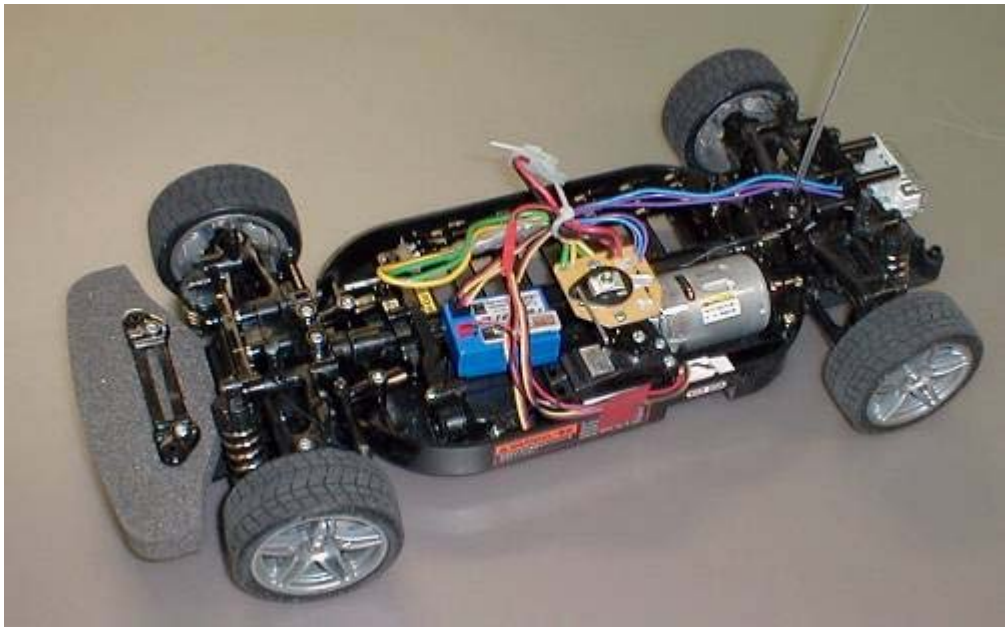
BACCALAUREAT 2006

SYSTEME DE RADIOPILOTAGE



SOMMAIRE

I- PRESENTATION DU SYSTEME DE RADIO PILOTAGE DE MODELISME

Le système support de l'étude est le modèle radio-commandé TAMIYA. C'est un modèle réduit au 1/10è de voiture de sport à quatre roues motrices et propulsion électrique.

MISE EN SITUATION :

Un véhicule à échelle réduite (1/10è) est piloté à distance sans liaison filaire.

La liaison se fait par ondes hertziennes à partir d'un boîtier d'émission (radiocommande).

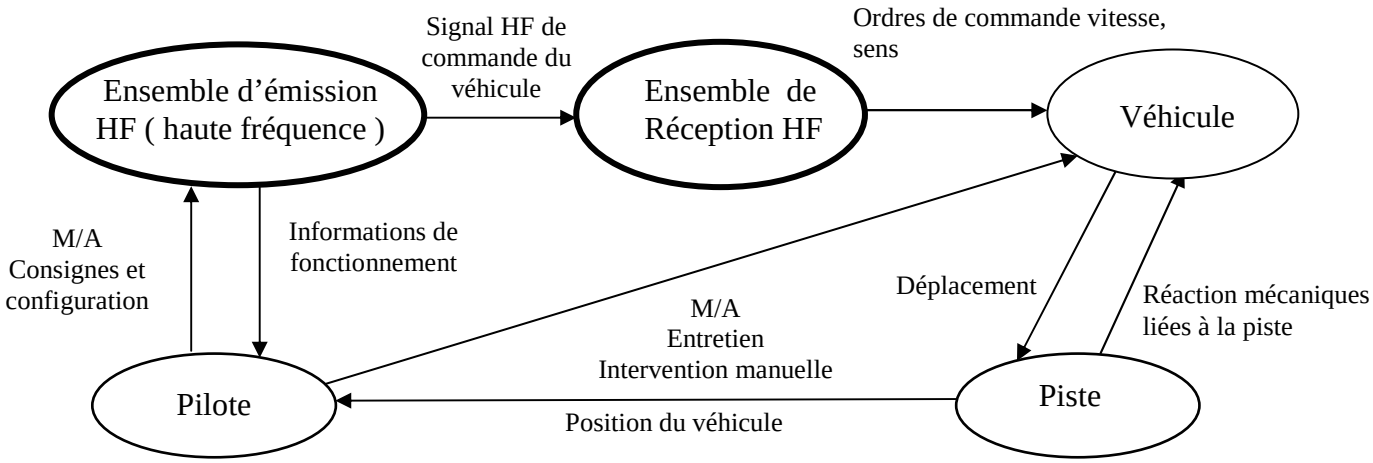
Celui-ci comprend les actionneurs nécessaires pour :

- Configurer les paramètres de fonctionnement et de transmission.
- Piloter le véhicule.

Pour le pilotage, on dispose de deux manettes :

- la manette de direction permettant de diriger le véhicule.
- la manette "vitesse-sens"permettant, suivant sa position par rapport au point de repos, de gérer les changements de sens et de vitesse.

DIAGRAMME SAGITTAL :



DEFINITION DES ELEMENTS DU SYSTEME :

- Pilote :

  Il agit sur l'ensemble d'émission pour :
  - le configurer,
  - puis, pour le pilotage du véhicule.

  De plus il doit assurer l'entretien du véhicule (réparations, changement des accumulateurs…) et les réglages et préparations mécaniques.

- Ensemble d'émission H. F. :

  C'est l'interface principale entre l'utilisateur et le véhicule. Il transforme les diverses commandes manuelles en un signal H.F. codé émis dans un rayon limité dans lequel doit se trouver la voiture pour permettre un pilotage optimum.

- Ensemble de réception H. F. :

  C'est l'interface entre l'ensemble d'émission et le véhicule. Il transforme le signal HF reçu en signaux électriques BF destinés aux actionneurs du véhicule.

- Véhicule :

  Il transforme les signaux BF en actions mécaniques, visuelle, sonore …

FONCTION D'USAGE DU SYSTEME:

Diriger un véhicule à distance sans liaison filaire avec l'utilisateur.

II – ETUDE FONCTIONNELLE DES OBJETS TECHNIQUES :.

OT1: ENSEMBLE D'EMISSION HF

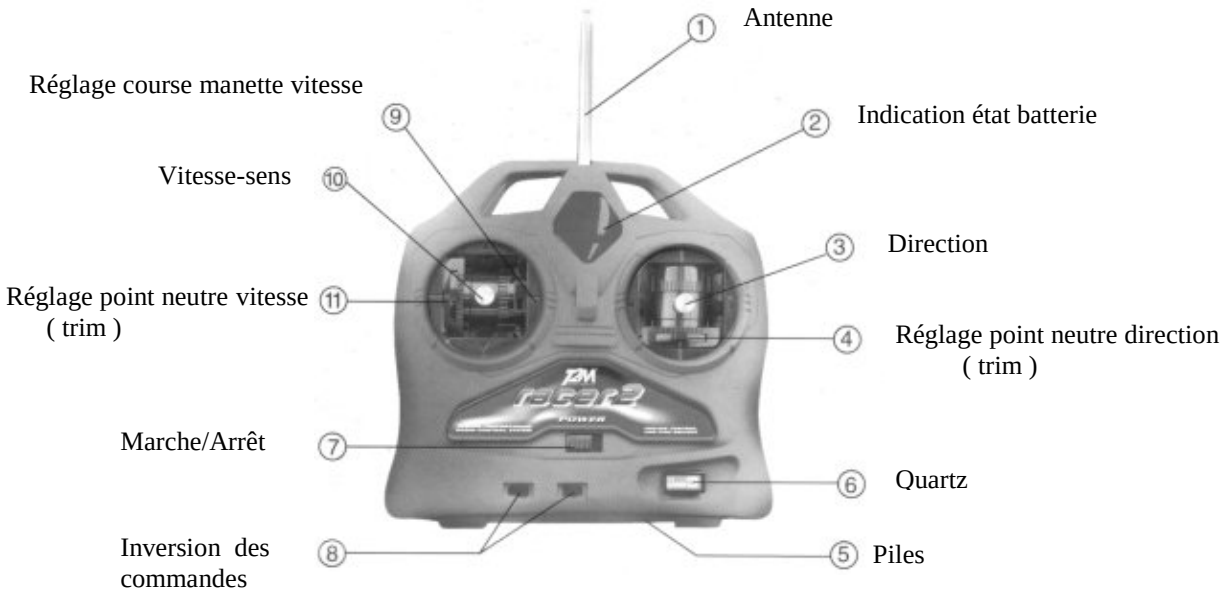
FONCTION D'USAGE :

- Convertir les différentes commandes manuelles (bouton poussoir, interrupteur manettes de direction et vitesse-sens), en signaux électriques.

- Générer et émettre un signal radio modulé (codé PPM) afin de diriger le véhicule à distance.

- Informer le pilote des paramètres de fonctionnement.

Exemple de modèle



OT2: ENSEMBLE DE RECEPTION HF

FONCTION D'USAGE :

- Sélectionner le signal radio modulé (codé PPM) émis par l'ensemble d'émission.

- Extraire du signal les ordres de commande: vitesse-sens, direction, allumage phares et avertisseur sonore.

ETUDE DES MILIEUX ASSOCIES

- Milieu technique:
  - Fonctionnement assuré par batterie autonome
  - Consommation de courant minimale
  - Plage de température de fonctionnement conseillée : de 0 à 50 °C.
  - L'ensemble émission-réception est compatible avec ceux du commerce
  - L'ensemble d'émission est capable de commander n'importe quel type de modèles réduits (avions compris).
- Milieu économique:
  - Le coût de fonctionnement correspond au remplacement des batteries et à leur recharge (chargeur).
- Milieu humain:
  - Leviers et manettes faciles à manœuvrer.
  - Mise en service et utilisation simple.
- Milieu physique:
  - La puissance d'émission ne doit pas exéder certaines valeurs (rayon d'action ou portée).
  - L'ensemble d'émission doit être aux normes des télécommunications (stabilité de la fréquence porteuse HF).
  - Le fonctionnement de l'ensemble d'émission ne doit pas interférer avec d'autre afin de ne pas perturber le fonctionnement des autres véhicules aux alentours (sélectivité des différents canaux radio).

CAHIER DES CHARGES

- Fonctionnalités de la radiocommande :

✓ Séquence à 4 voies : 2 proportionnelles utilisées pour les manettes gauche-droite et vitesse-sens, et 2 voies auxiliaires tout ou rien disponibles pour d'autres utilisations
✓ Fonctionnement intuitif
✓ Inversion possible du sens de commande des manches
✓ Réglage possible de la position neutre des manettes de commande

- Caractéristiques techniques de la radiocommande :

✓ Alimentation : par accumulateurs ou piles de 12V – consommation : environ 50 mA.
✓ Portée : minimum 100m.
✓ Signal de sortie PPM (Pulse Position Modulation) compatible avec tous le récepteurs FM et/ou AM existants.
Modulation PPM : La valeur lue sur les manches est immédiatement traduite en une durée, et c'est cette durée qui est transmise par support H. F.
✓ 2 types de réalisations sont proposés:
Modulation d'amplitude dans la bande des 26 MHz. Choix du canal par changement d'un quartz.
Modulation de fréquence dans la bande des 41 MHz. Choix du canal par programmation.

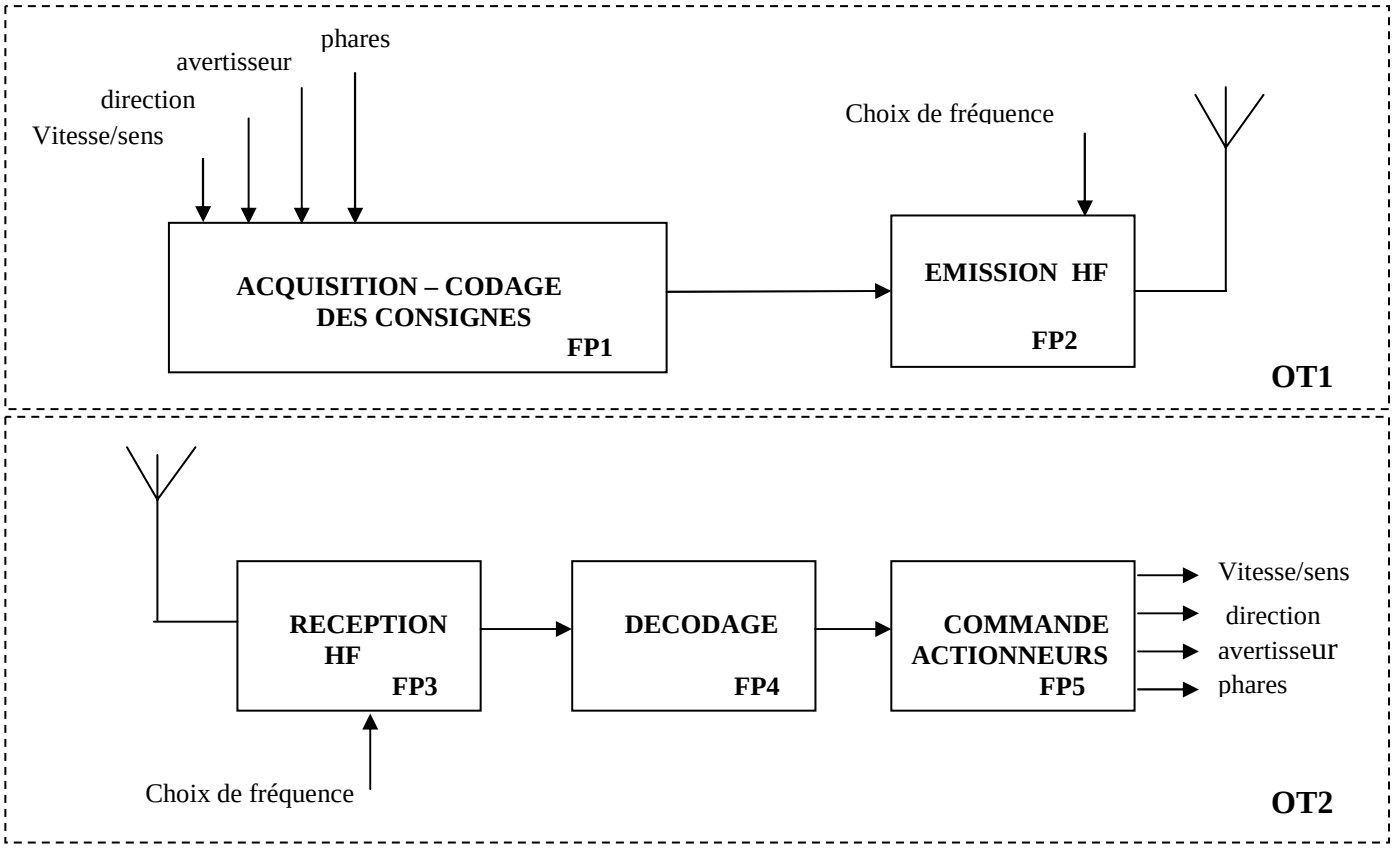
- Fonctionnalités de l'ensemble réception

✓ Encombrement et poids réduit
✓ Réception de 4 voies de commande

- Caractéristiques techniques de l'ensemble réception :

✓ Alimentation : par batterie de 7,2V utilisé pour la traction du véhicule.
✓ Insensibilité aux fréquences voisines
✓ Tension de sortie des signaux de commande de 5V
✓ Faible consommation d'environ 50 mA
✓ Signal d'entrée PPM (Pulse Position Modulation) compatible avec tous les emetteurs FM et/ou AM à codage PPM existants.
✓ 2 types de réalisations sont proposés:
Modulation d'amplitude dans la bande des 27 MHz. Choix du canal par changement de quartz.
Modulation de fréquence dans la bande des 41 MHz. Choix du canal par changement de quartz.

SCHEMA FONCTIONNEL DE PREMIER DEGRE :



DEFINITIONS DES FONCTIONS PRINCIPALES

FP1: ACQUISITIONS – CODAGE DES CONSIGNES
- Transforme des actions manuelles en signaux électriques images de ces actions.
- Génère une trame PPM série codée en durées images des signaux électriques de FP1 (voir annexe)

FP2: EMISSION HF
Transmet une onde hertzienne HF modulée par la trame PPM issue de FP1

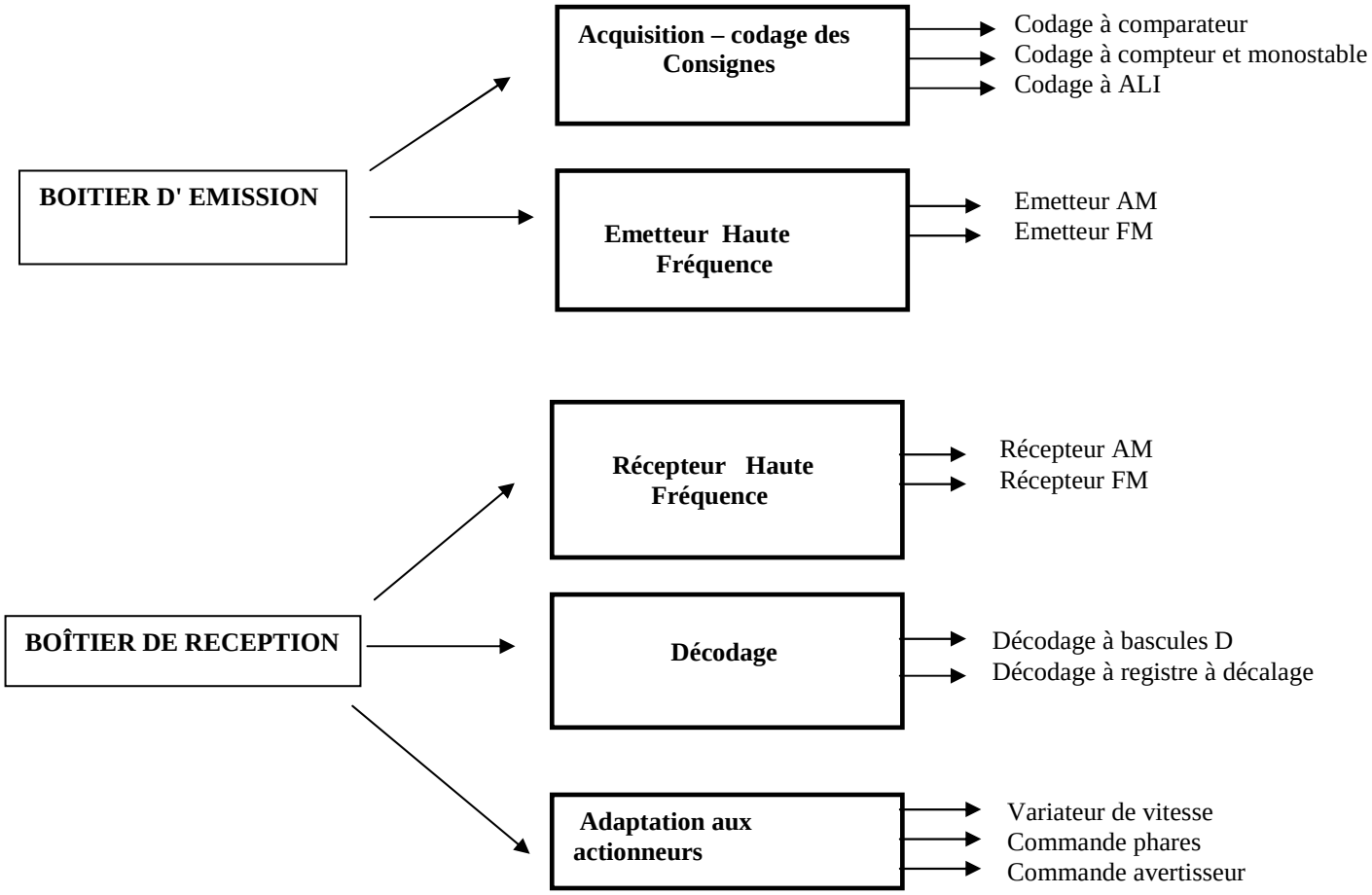
FP3: RECEPTION HF
Capte et démodule le signal HF pour récupérer la trame PPM émise.

FP4: DECODAGE
Sépare les informations série de la trame PPM pour les diriger vers l'actionneur concerné.

FP5: COMMANDE ACTIONNEURS
Transforme une information de durée en signaux propres à chaque actionneur.

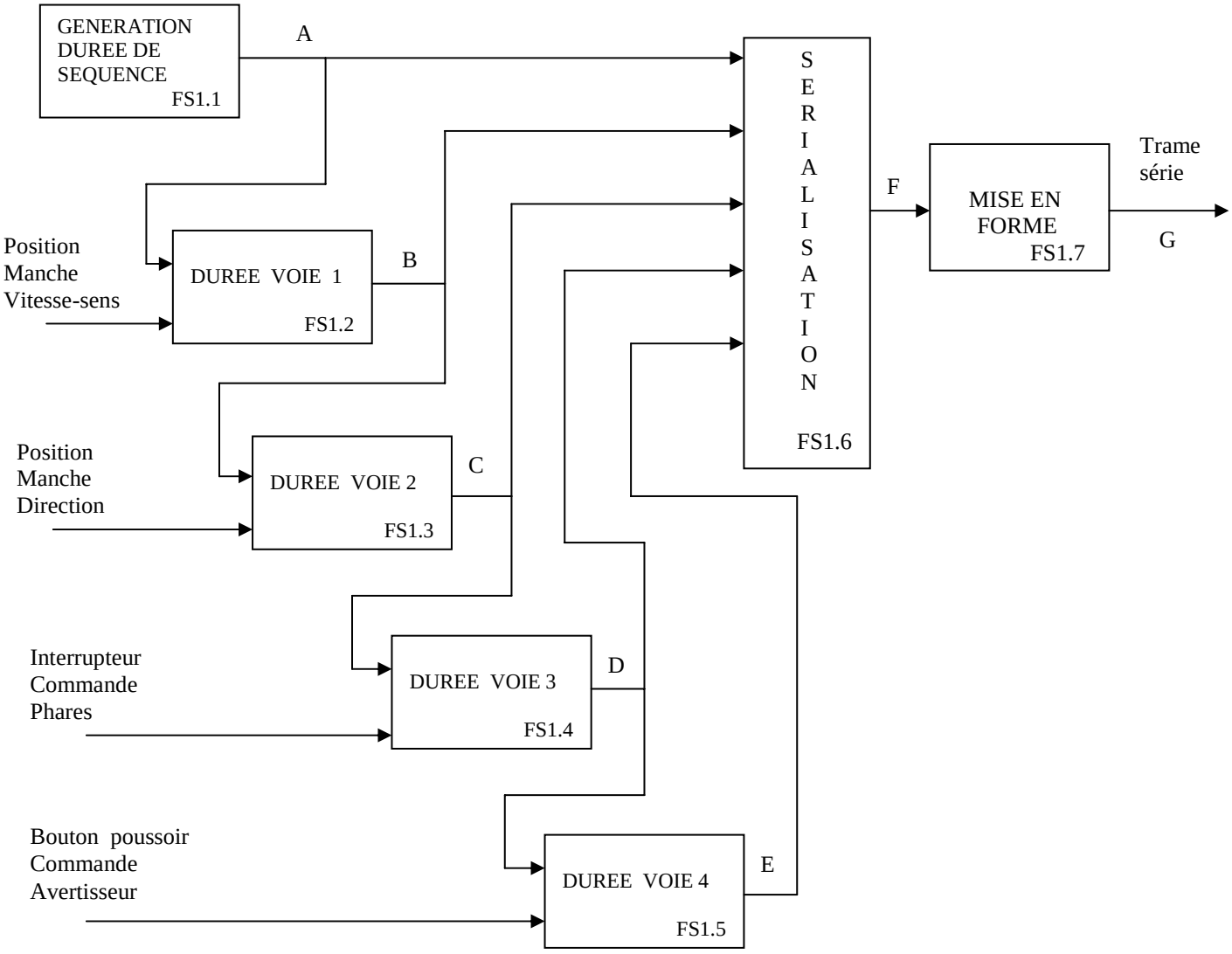
SCHEMA FONCTIONNEL DE SECOND DEGRE :

Différentes solutions technologiques sont envisagées conduisant chacune à un schéma fonctionnel du second degré légèrement différents selon le diagramme suivant :



FP1: ACQUISITIONS – CODAGE DES CONSIGNES

Solution 1: Codage à comparateur



FS1.1: GENERATION DE LA DUREE DE SEQUENCE

Génère des impulsions positives distantes de 20 ms (Ds)

FS1.2: DUREE VOIE 1

Déclenchée par FS1.1, génère une impulsion positive après une durée image de la position du manche vitesse-sens.
Manche en position extrême: 1ms ; 2ms
Manche en position médiane: 1,5 ms

Entrées : - Impulsion de déclenchement
- Position manche vitesse-sens

Sortie : Impulsion positive

FS1.3: DUREE VOIE 2

Déclenchée par FS1.2, génère une impulsion positive après une durée image de la position du manche direction.
Manche en position extrême: 1ms ; 2ms
Manche en position médiane: 1,5ms

Entrées : - Impulsion de déclenchement
- Position manche direction

Sortie : Impulsion positive

FS1.4: DUREE VOIE 3

Déclenchée par FS1.3, génère une impulsion positive après une durée image de l'état de l'interrupteur phares
Interrupteur OFF : 1 ms
Interrupteur ON : 2 ms

Entrées : - Impulsion de déclenchement
- Etat interrupteur Phares

Sortie : impulsion positive

FS1.5: DUREE VOIE 4

Déclenchée par FS1.4, génère une impulsion positive après une durée image de l'état du bouton poussoir avertisseur.
Bouton pousoir OFF : 1 ms
Bouton pousoir ON : 2 ms

Entrées : - Impulsion de déclenchement
- Etat bouton poussoir Avertisseur

Sortie : Impulsion positive

FS1.6: SERIALISATION

Mise en série des impulsions de voies

Entrée : Impulsions issues des différentes voies

Sortie : Pseudo-trame PPM

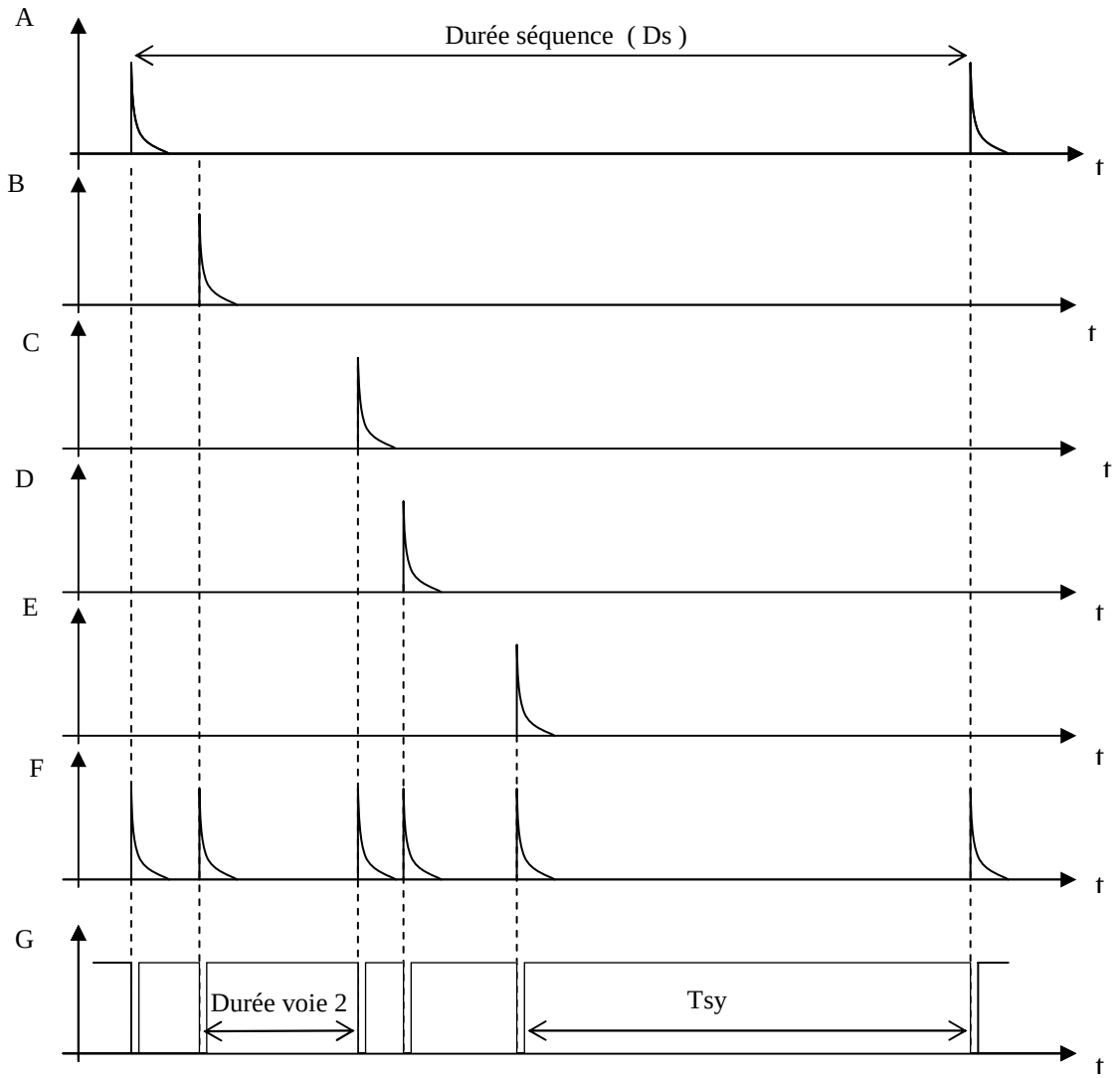
FS1.7: MISE EN FORME

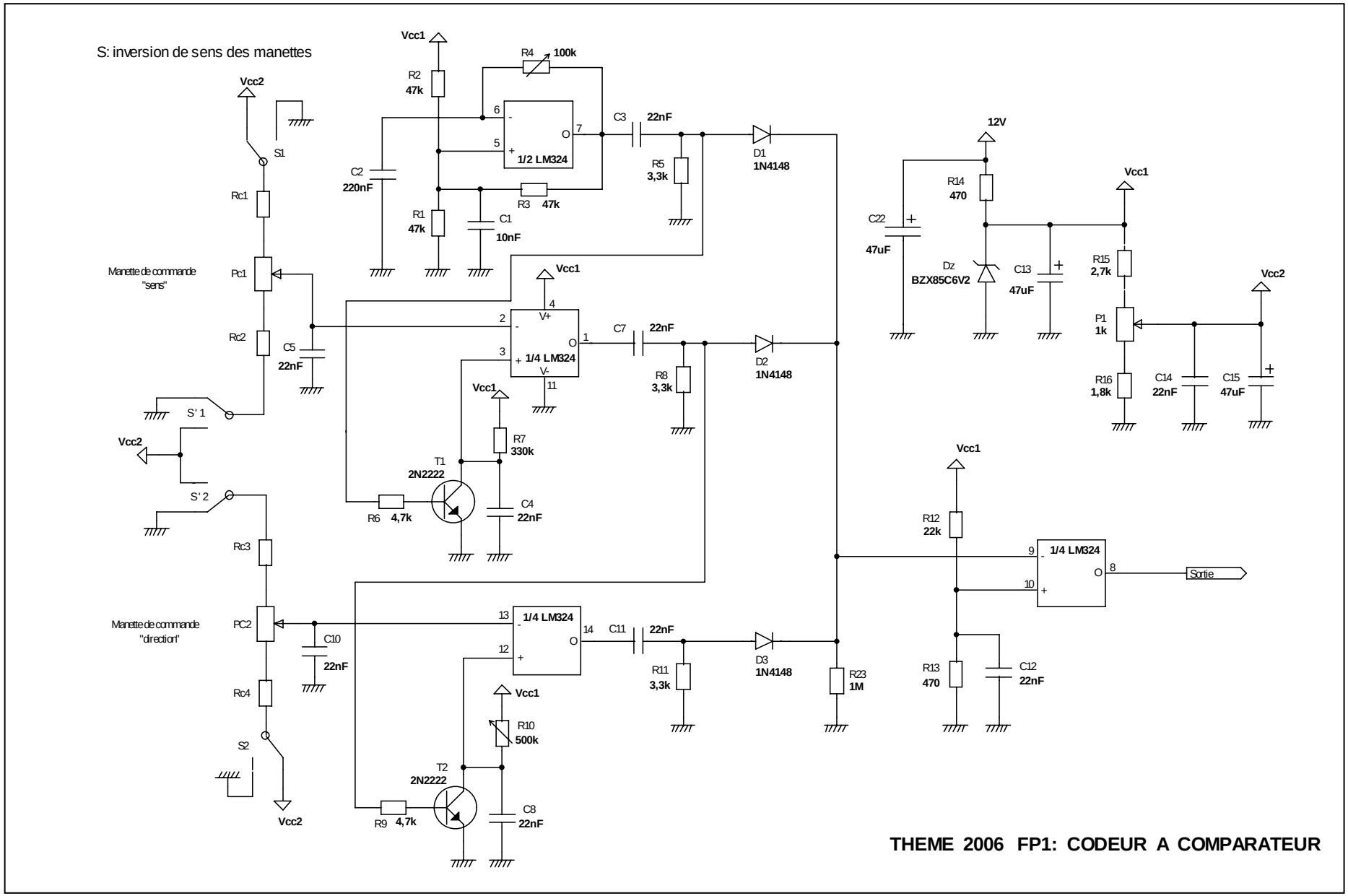
Restitue la forme habituelle de la trame PPM (durée inter-voie de 300µs, niveau haut pour la durée d'une voie).

Entrée : Pseudo-trame PPM

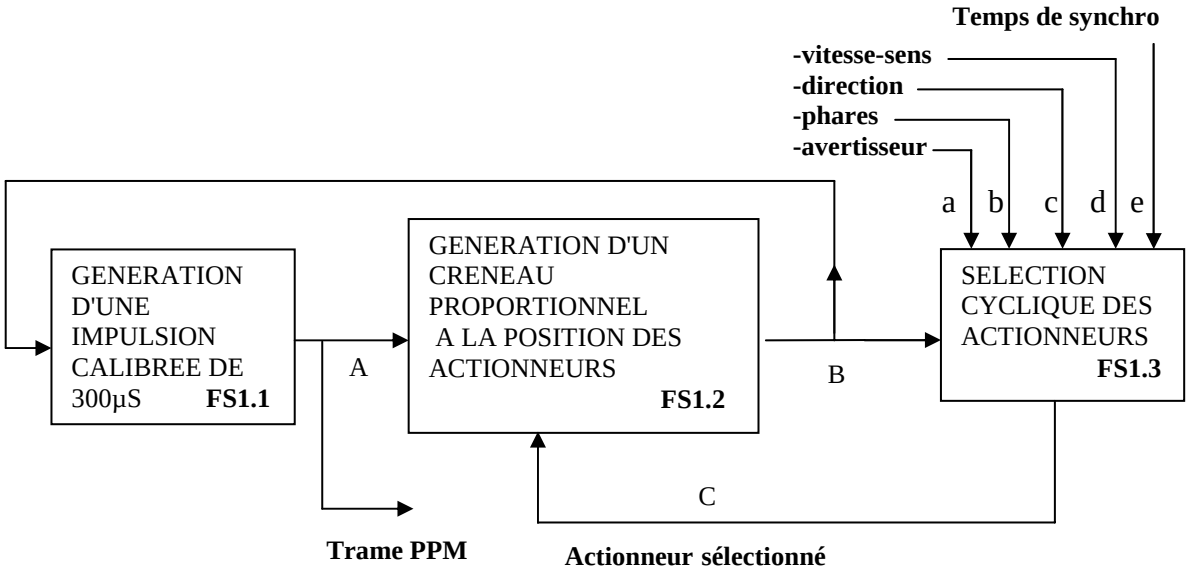
Sortie : Trame PPM

CHRONOGRAMMES FONCTIONNELS




S: inversion de sens des manettes
Vcc1
R4 100k
R2 47k
6
5
7
1/2 LM324
C3 22nF
D1 1N4148
C2 220nF
R5 3,3k
R3 47k
R1 47k
C1 10nF
Vcc2
S1
Rc1
Manette de commande "sens"
Pc1
Rc2
C5 22nF
Vcc1
4
2
3
1
11
1/4 LM324
V+
V-
C7 22nF
D2 1N4148
R8 3,3k
S' 1
Vcc2
S' 2
Vcc1
R7 330k
T1 2N2222
R6 4,7k
C4 22nF
Rc3
Manette de commande "direction"
PC2
C10 22nF
13
12
14
1/4 LM324
C11 22nF
D3 1N4148
R11 3,3k
R23 1M
Rc4
S2
Vcc2
Vcc1
R10 500k
T2 2N2222
R9 4,7k
C8 22nF
12V
R14 470
C22 47uF
Dz BZX85C6V2
C13 47uF
Vcc1
R15 2,7k
P1 1k
R16 1,8k
C14 22nF
C15 47uF
Vcc2
Vcc1
R12 22k
9
10
8
1/4 LM324
Sortie
R13 470
C12 22nF
THEME 2006 FP1: CODEUR A COMPARATEUR

Solution 2: Codage à compteur et monostable



FS1.1:GENERATION D'UNE IMPULSION CALIBREE DE 300µS

Génère ,après déclenchement par FS1.2, l'impulsion inter-voie de 300µs

Entrée : Impulsion de déclenchement

Sortie : Impulsions calibrées formant la trame PPM

FS1.2:GENERATION D'UN CRENEAU PROPORTIONNEL A LA POSITION DES ACTIONNEURS

Génère ,après déclenchement par le front montant de FS1.1, le créneau de durée de voie sélectionnée.

Entrées : - Impulsion de déclenchement
- Position des actionneurs

Sortie : Créneau calibré en fonction de la position des manches

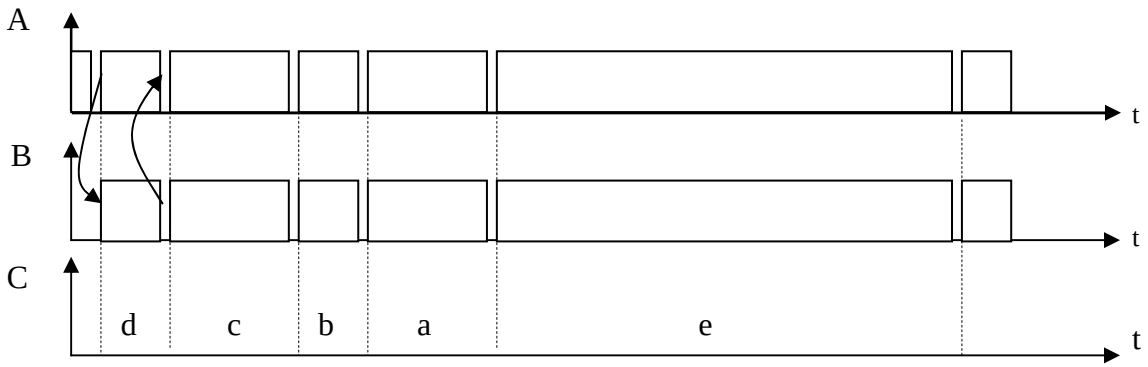
FS1.3:SELECTION CYCLIQUE DES ACTIONNEURS

Sélectionne ,après déclenchement par le front montant de FS1.2, un actionneur parmi 4 ou le temps de synchronisation

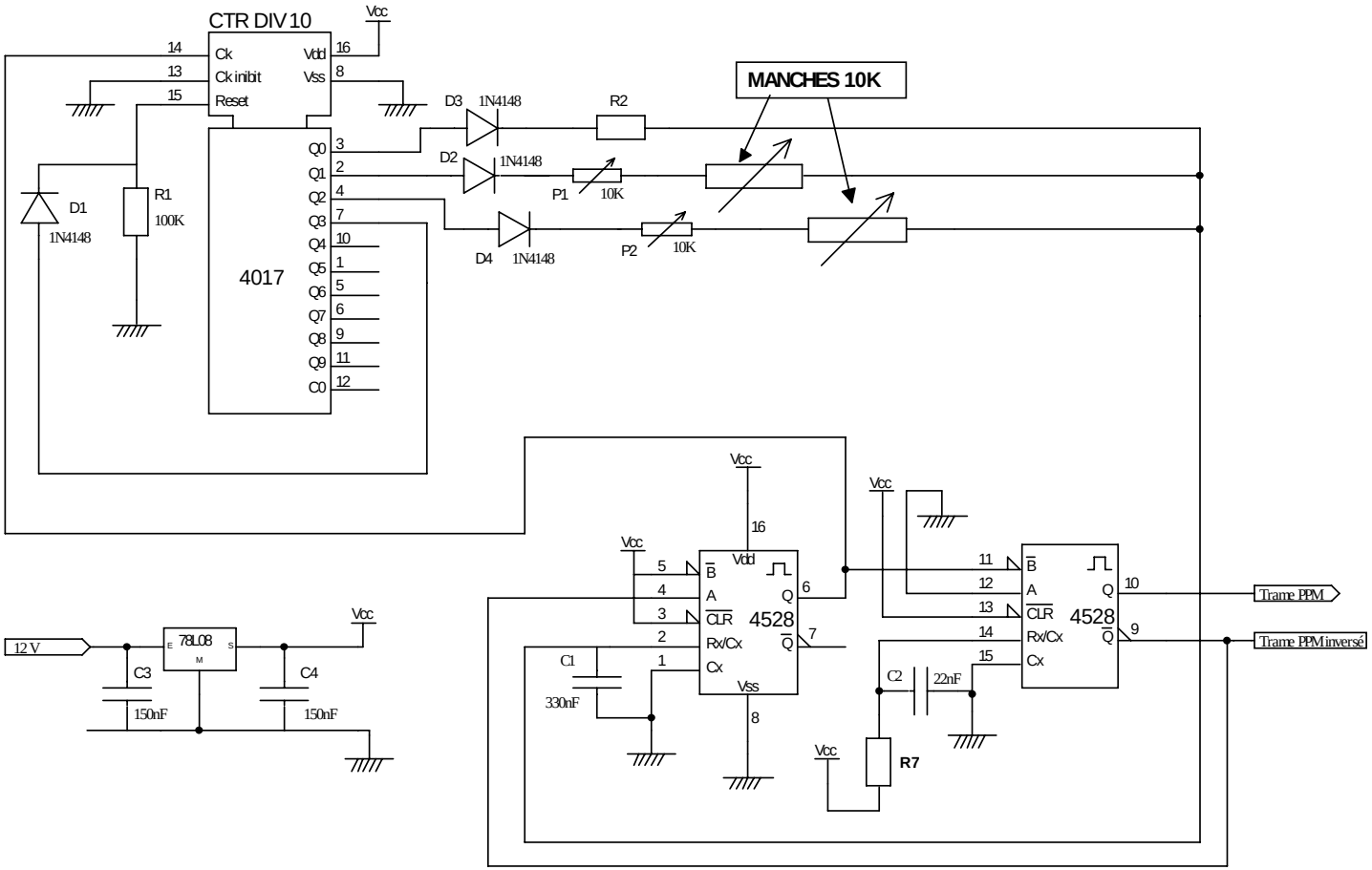
Entrées : - Impulsion de déclenchement
- Actionneurs et Tsy

Sortie : Niveau validant un actionneur parmi 4 ou Tsy

CHRONOGRAMMES FONCTIONNELS

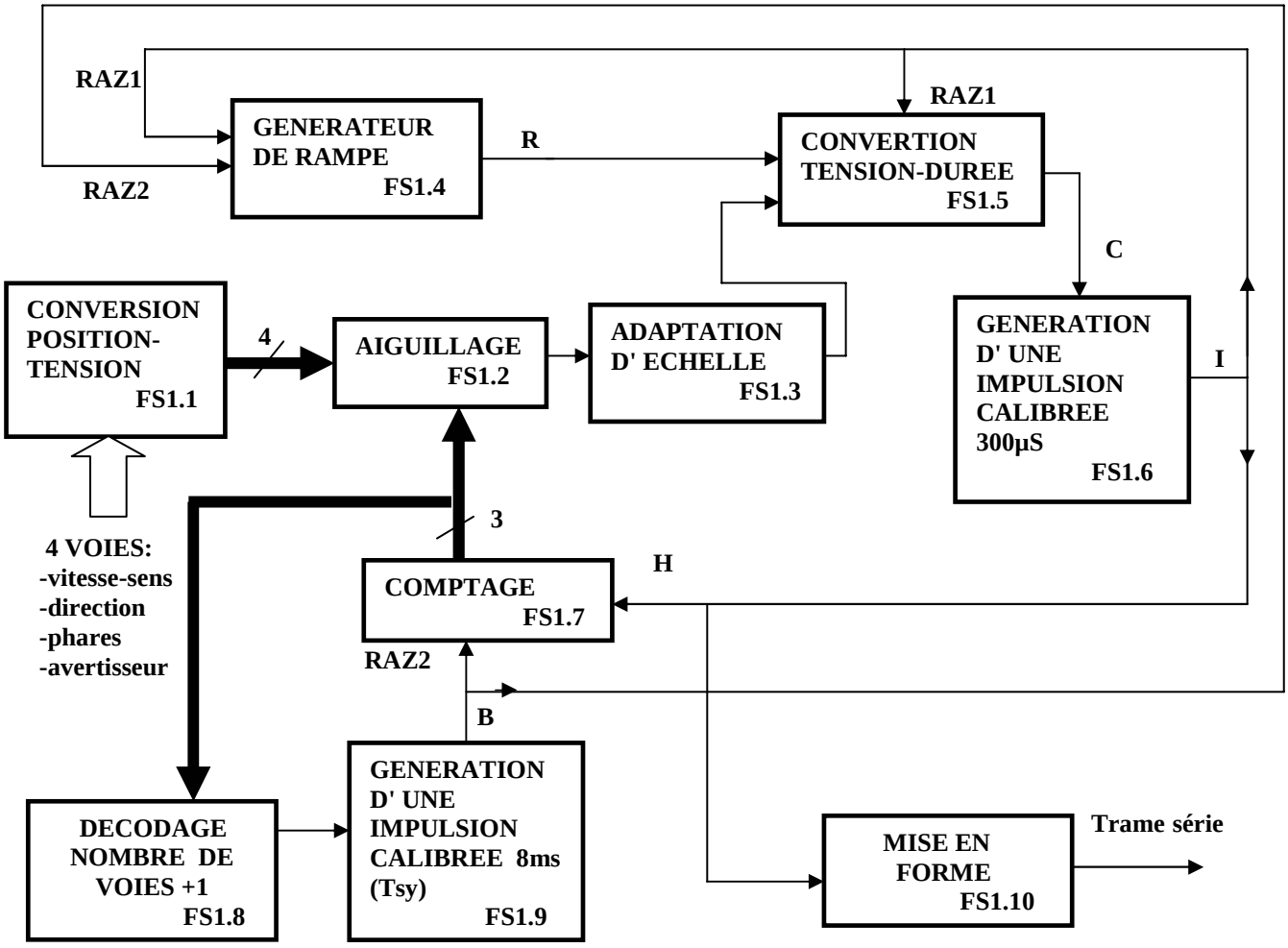


SCHEMA STRUCTUREL



CODEUR A COMPTEUR ET MONOSTABLE

Solution 3: Codage à ALI



FS1.1: CONVERSION POSITION-TENSION

Des potentiomètres couplés aux manches de commande fournissent des tensions analogiques fonctions de la position du manche considéré, et dont les valeurs extrèmes dépendent des caractéristiques mécaniques des manches (position de repos, butées, etc).
Des boutons poussoirs fournissent deux niveaux de tension (ON-OFF)

Entrées : - Position des manches
- Etat des boutons poussoirs (phares et avertisseur)

Sorties : Tensions analogiques comprises entre 0 et 10V

FS1.2: AIGUILLAGE

Sélectionne cycliquement une voie parmi 4 en fonction de l'état du compteur.

Entrées: - 4 tensions analogiques comprises entre 0 et 10V.
- nombre binaire variant périodiquement de 000 à nombre de voies+1

Sortie : Tension analogique image successive des voies

FS1.3: ADAPTATION D' ECHELLE

Permet de régler les valeurs de positions extrèmes des manches de commande autour d'une valeur médiane fixe.

Entrée: Tension analogique image successive des voies

Sortie : Tension analogique variant de 0 volts (position extrème du manche) à 10 volts (autre position extrème du manche), centrée sur 5 volts (position de repos du manche).

FS1.4: GENERATEUR DE RAMPE

Délivre une tension variant linéairement en fonction du temps

Entrées: RAZ1 et RAZ2: mise à zéro de la tension de sortie

Sortie : Tension variant linéairement avec une pente de 5V/1,5ms

FS1.5: CONVERSION TENSION - DUREE

Délivre une tension fixe dont la durée est proportionnelle à la tension issue de FS1.3

Entrées: - RAZ1 : mise à 0V de la sortie
- Tension variant linéairement avec une pente de 5V/1,5ms
- Tension issu de FS1.3 image des commandes.

Sorties : - Niveau haut de durée image de la position des organes de commande
- Manche en position extrême: 0V ⟶ 1ms
  10V ⟶ 2ms
- Manche en position médiane: 5V ⟶ 1,5ms

- Bouton pousoir OFF : 1 ms
- Bouton pousoir ON : 2 ms

FS1.6: GENERATION D' IMPULSION CALIBREE DE 300µs

Génère à la fin de l'analyse de chaque voie une impulsion de 300µs permettant la séparation inter-voie et le lancement de l'analyse de la voie suivante.
L'ensemble des impulsions constitue la trame PPM

Entrée : Front descendant de FS1.5

Sortie : Impulsion positive 10V de durée 300µs

FS1.7: COMPTAGE

En contrôlant la fonction FS1.2 (aiguillage), permet la sélection cyclique des voies à analyser.

Entrées : - Impulsion positive 10V de durée 300µs
- RAZ2 , remise à zéro

Sortie : Nombre binaire variant périodiquement de 000 à à nombre de voies+1

FS1.8: DECODAGE NOMBRE DE VOIES+1

Permet le lancement de l'impulsion inter-trame Tsy.

Entrée : Nombre binaire variant périodiquement de 000 à nombre de voies+1

Sortie : Impulsion de 10V pour une entrée égale à nombre de voies+1

FS1.9: GENERATION D' UNE IMPULSION CALIBREE DE 8ms

Génère le temps inter-trame (temps de synchronisation), remet à zéro le compteur dés le lancement de Tsy et maintient à zéro le générateur de rampe pendant Tsy

Entrée : Impulsion de 10V

Sortie : Durée calibrée correspondant à Tsy

FS1.10: MISE EN FORME

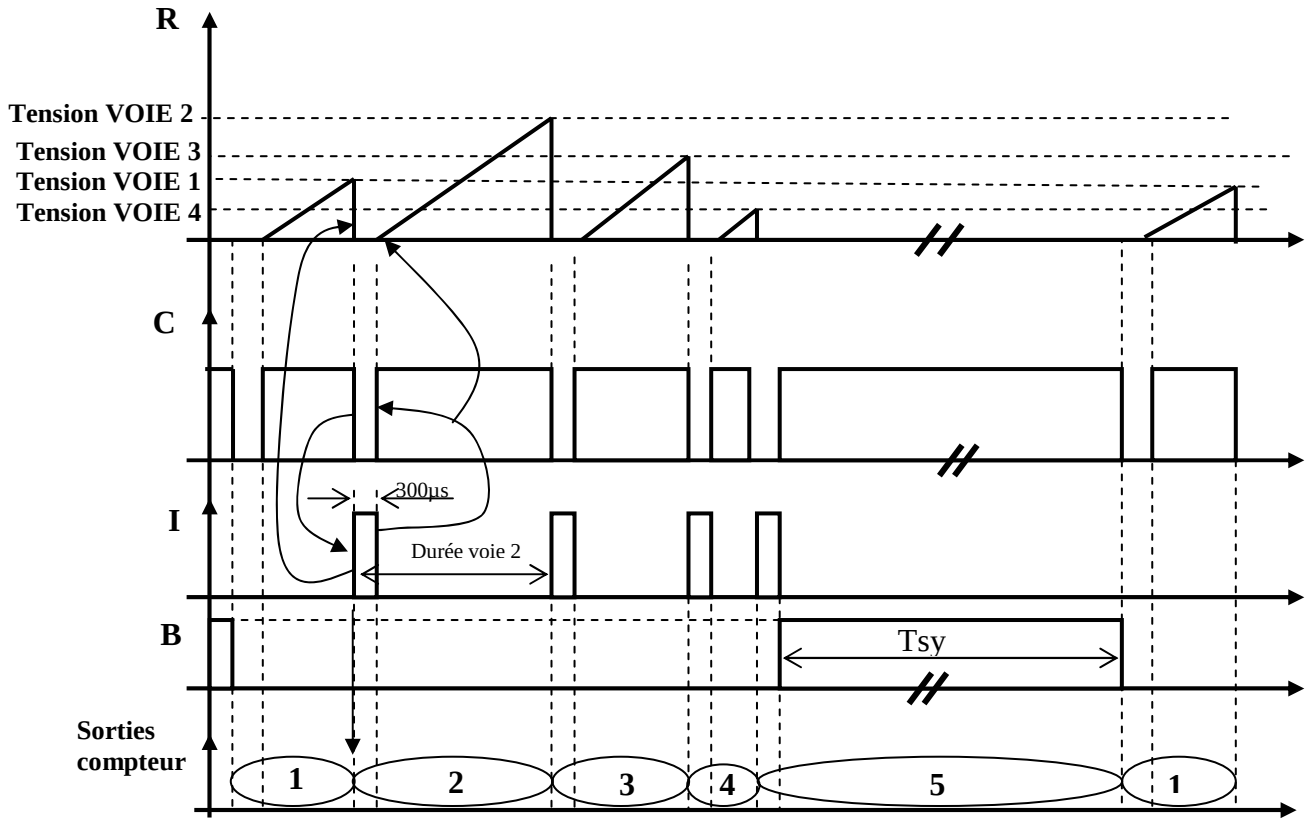
Rend les fronts de la trame PPM trapézoïdaux pour limiter l'émission de fréquence parasites.

Entrée : Impulsions à fronts raides

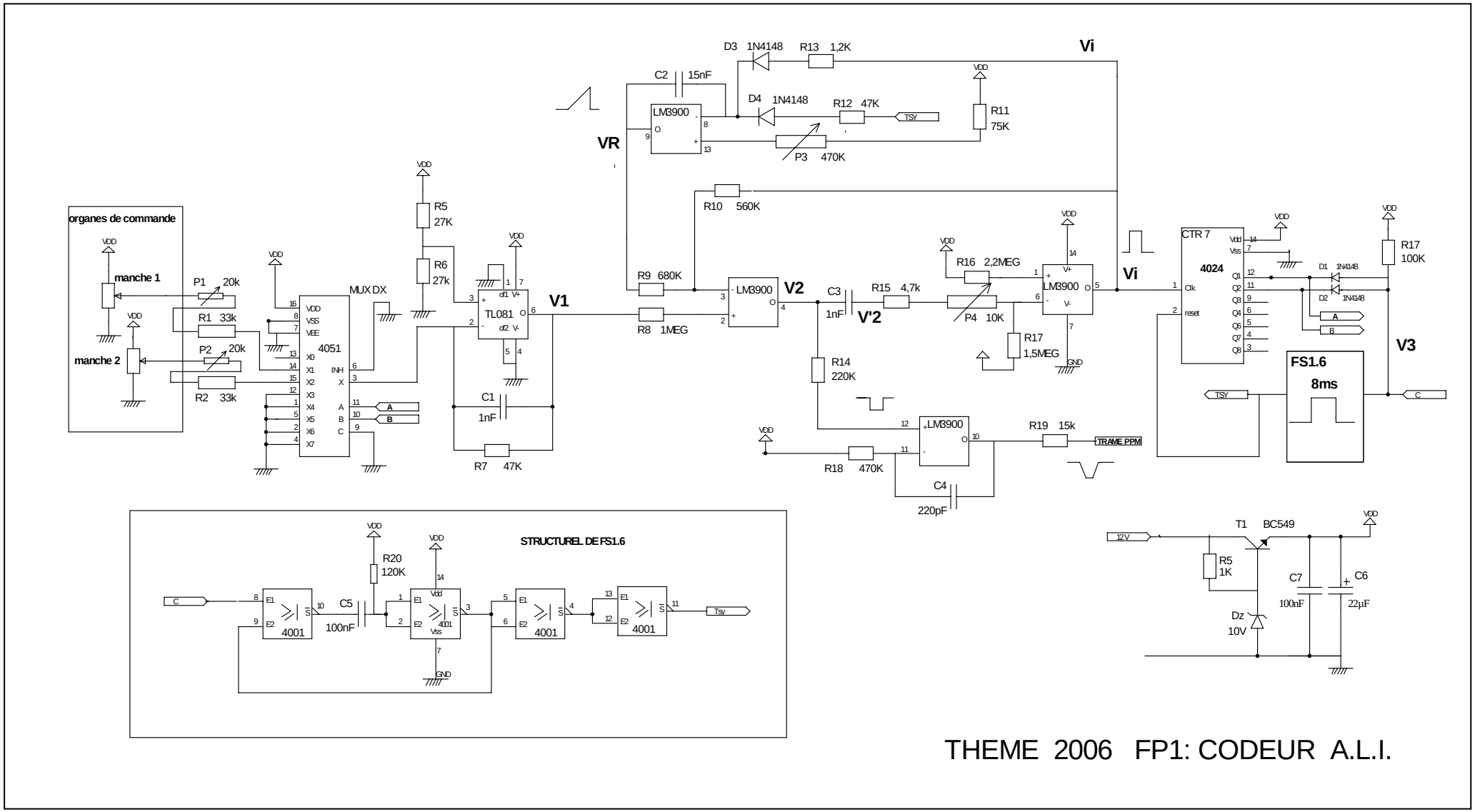
Sortie : Impulsions à fronts trapézoïdaux

CHRONOGRAMMES FONCTIONNELS POUR 4 VOIES

(NB: le structurel est légèrement différent)



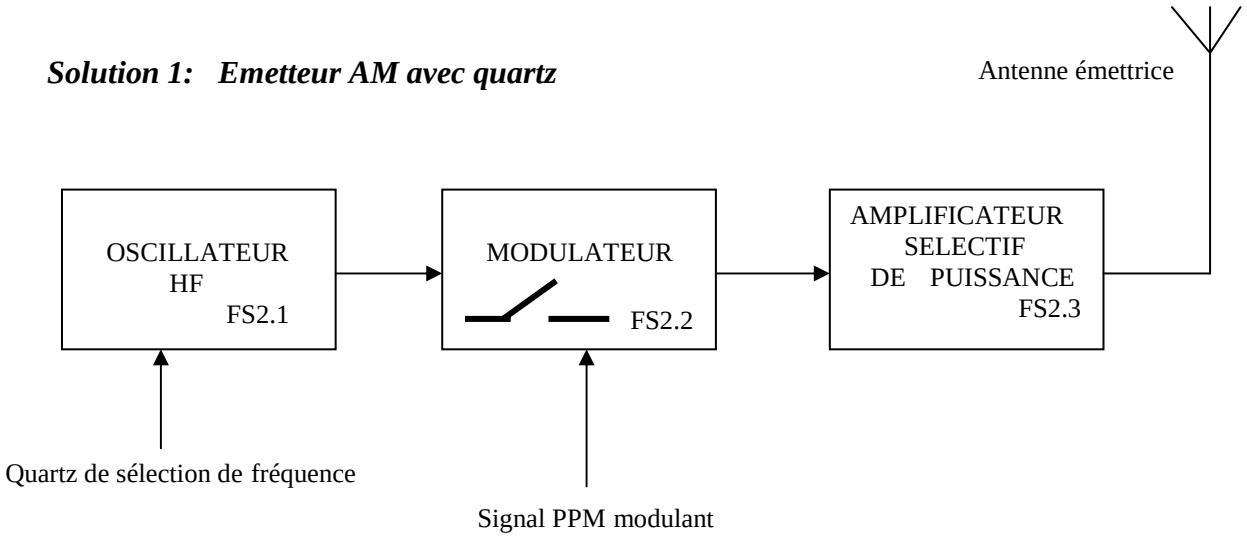
SCHEMA STRUCTUREL



THEME 2006 FP1: CODEUR A.L.I.

FP2: EMISSION HAUTE FREQUENCE

Solution 1: Emetteur AM avec quartz



FS2.1: OSCILLATEUR HF

Génère la fréquence porteuse en fonction du choix du quartz

Entrée : Quartz de sélection de fréquence

Sortie : Signal sinusoïdal haute fréquence

FS2.2: MODULATEUR

Autorise ou stoppe (module) l'émission du signal HF sous contrôle du signal PPM.

Entrée : Signal sinusoïdal haute fréquence

Sortie : Signal sinusoïdal modulé en tout ou rien

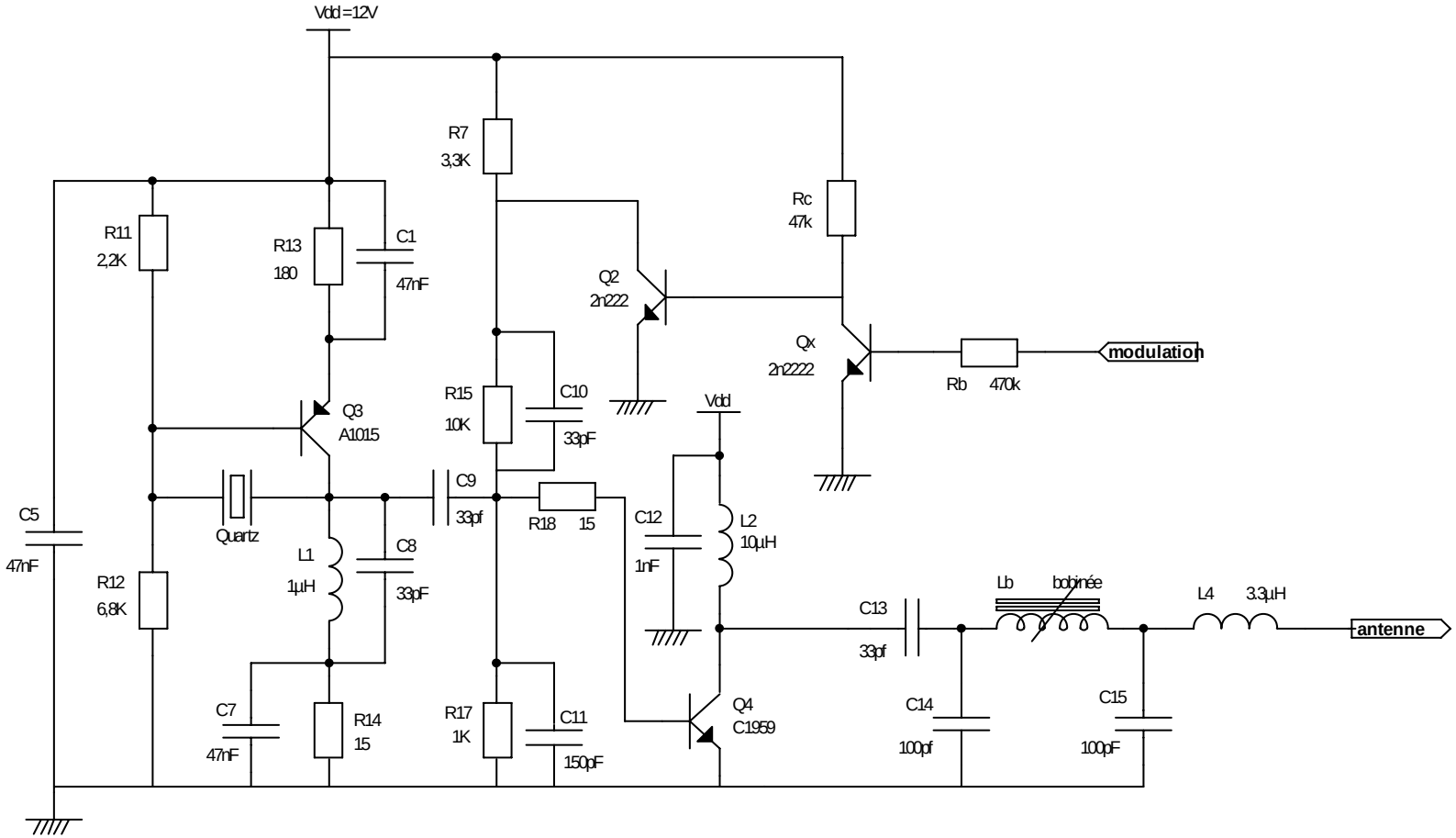
FS2.3: AMPLIFICATEUR SELECTIF DE PUISSANCE

Amplifie dans une bande étroite de fréquence

Entrée : Signal sinusoïdal modulé en tout ou rien

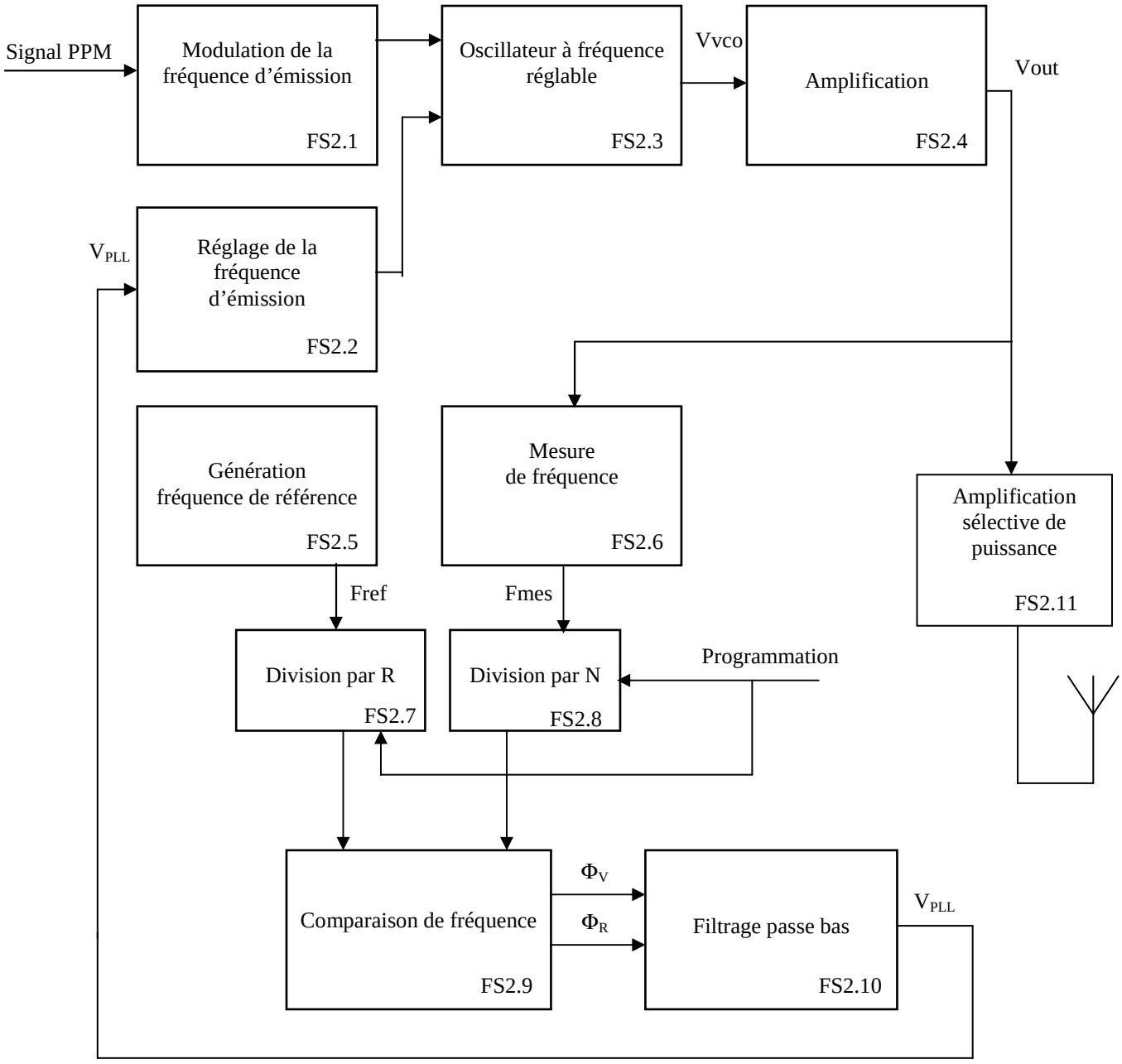
Sortie : Signal sinusoïdal modulé en tout ou rien amplifié en puissance et filtré

SCHEMA STRUCTUREL



THEME 2006 FP2 : Emetteur AM

Solution 2: Emetteur FM à fréquence d'émission programmable
(synthèse de fréquence)



FS2.1 : MODULATION DE LA FREQUENCE D'EMISSION

Génère une tension de consigne permettant de moduler la fréquence de l'oscillateur FS2.3 autour d'une fréquence centrale

Entrée : Signal PPM, train d'impulsions de durées variables (valeur minimale 1 ms, valeur maximale 2 ms, valeur de repos 1,5 ms).

Sortie : Tension modulante

FS2.2 : REGLAGE DE LA FREQUENCE D'EMISSION

Génère une tension permettant de stabiliser la fréquence centrale de l'oscillateur FS2.3

Entrée : Tension analogique V_{PLL} , image de l'écart entre la fréquence réellement émise et la fréquence de consigne programmée.

Sortie : Tension de réglage

FS2.3 : OSCILLATEUR A FREQUENCE VARIABLE

Génère un signal sinusoïdal de fréquence asservie par FS2.2 et modulé par FS2.1

Entrée : Tension modulante
Tension de réglage

Sortie : Vvco, signal sinusoïdal de fréquence Fvco variable autour de la fréquence de milieu de bande définie par programmation.

FS2.4 : AMPLIFICATION

Amplifie le signal Fvco.

Entrée : Vvco, signal sinusoïdal de fréquence Fvco variable autour de la fréquence de milieu de bande définie par programmation..

Sortie : Vout, signal sinusoïdal amplifié de fréquence Fout = Fvco

FS2.5 : GENERATION FREQUENCE DE REFERENCE

Génère un signal sinusoïdal de référence, d'amplitude 5V crête à crête, de fréquence fixe 10245 kHz , pour asservissement de la fréquence d'émission.

FS2.6 : MESURE DE FREQUENCE

Donne une image de la fréquence d'émission par couplage magnétique.

Entrée : Information de fréquence Fout par couplage magnétique

Sortie : Fmes, signal sinusoïdal d'amplitude ≥ 500mV, de fréquence Fmes = Fout = Fvco.

FS2.7 et FS2.8: DIVISION DE FREQUENCE

Fref est divisée par R et Fmes par N de tel sorte que si Fmes = Fprogrammée alors
Fref/R = Fmes/N = 5 KHz

Entrée : Fmes, Fref et N, R (par programmation)

Sortie : Ferf/R et Fmes/N.

FS2.9: COMPARAISON DE FREQUENCES

Compare Fref/R et Fref/N et génère un signal image de l'écart entre Fref et Fmes.

Entrées : Fmes/N,
Fref/R, signal sinusoïdal de fréquence Fref /R= 10 245 kHz./R

Sorties : Φ_V et Φ_R , signaux logiques de valeurs 0 ou 5 volts, présentant des impulsions dont la largeur est fonction de l'écart de phase entre les signaux d'entrée mis en forme, de fréquences respectives Fmes/N et Fref/R. Les valeurs N et R sont choisies dans le programme de façon à obtenir dans les deux cas une fréquence de 5 kHz, ce qui permet la programmation de la fréquence d'émission par pas de 5 kHz.

FS2.10 : FILTRAGE PASSE-BAS

Permet d'obtenir la valeur moyenne de l'écart de phase entre la fréquence d'émission et la fréquence programmée, afin de régler la fréquence d'émission de façon stable, sans perturber la modulation de fréquence.

Entrées : Φ_V et Φ_R , signaux logiques de valeurs 0 ou 5 volts, présentant des impulsions dont la largeur est fonction de l'écart de phase entre les signaux d'entrée mis en forme, de fréquences respectives Fmes/N et Fref/R.

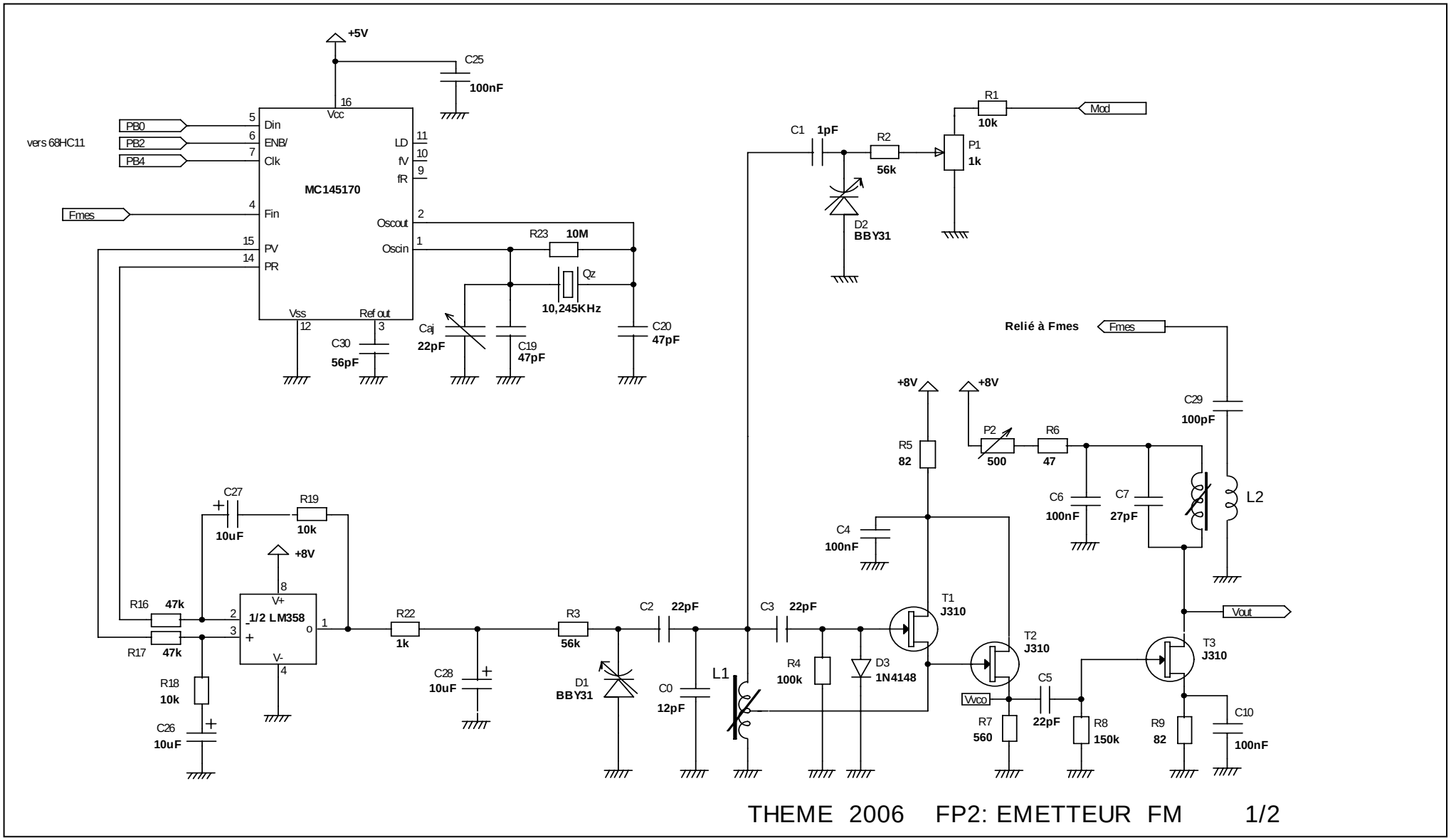
Sortie : Tension analogique V_{PLL} , image de l'écart moyen entre fréquence d'émission et fréquence programmée, variable de 0 à 8 volts.

FS2.11 : AMPLIFICATION SELECTIVE DE PUISSANCE

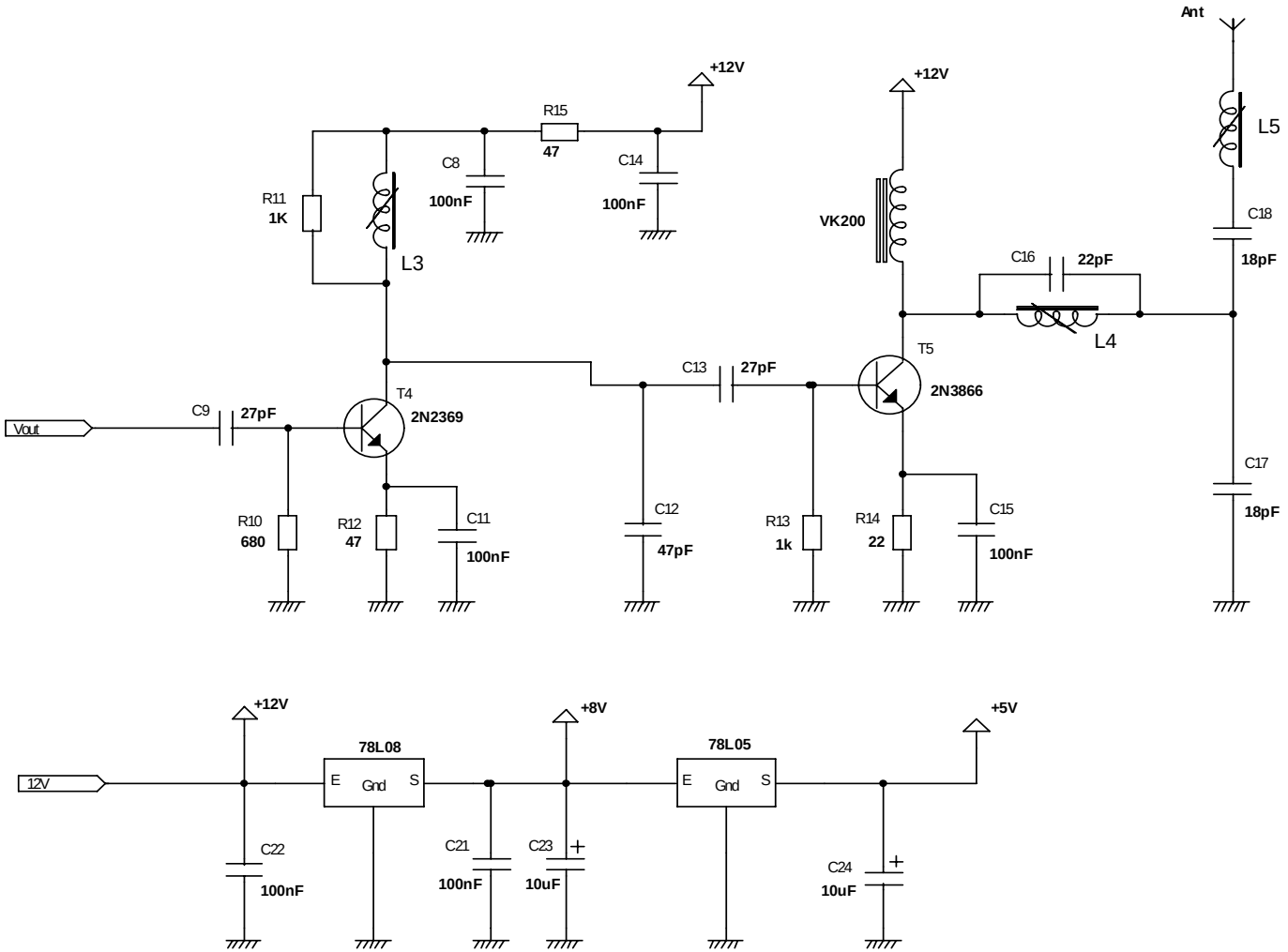
Amplifie dans une bande étroite de fréquence

Entrée : Signal sinusoïdal modulé Vout
Sortie : Signal sinusoïdal modulé amplifié en puissance et filtré.

SCHEMA STRUCTUREL



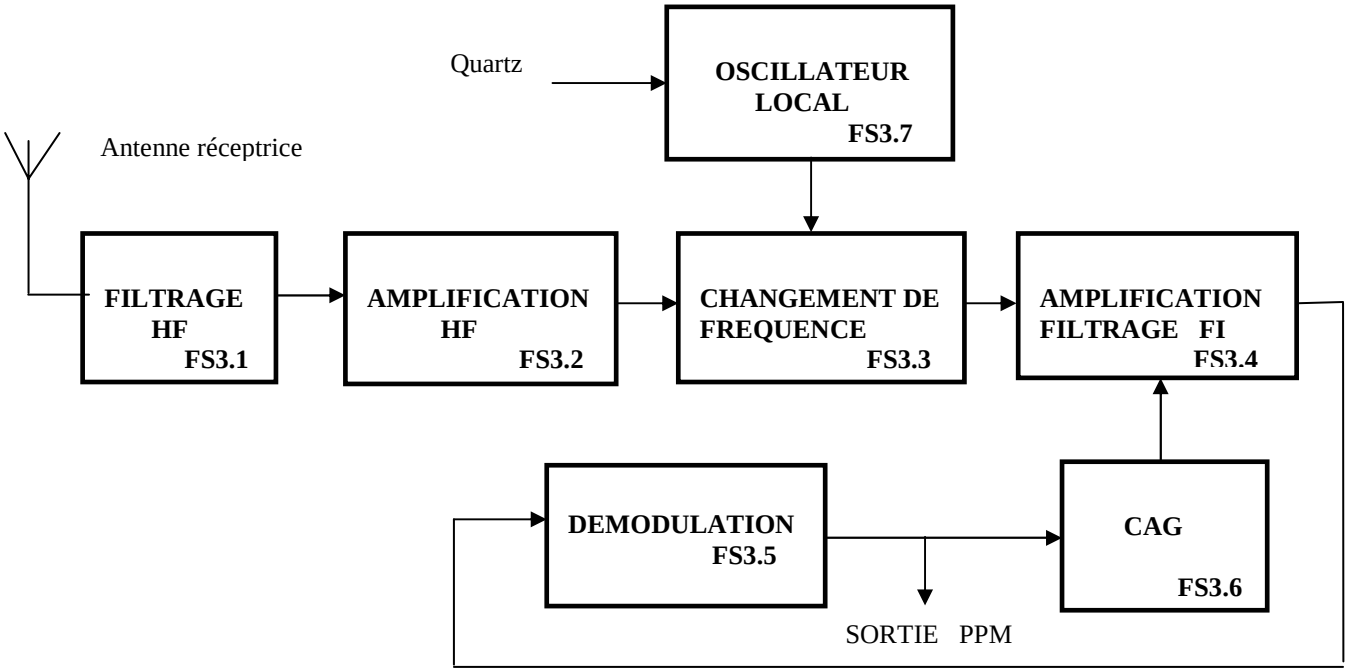
SCHEMA STRUCTUREL



THEME 2006 FP2: EMETTEUR FM 2/2

FP3: RECEPTION HAUTE FREQUENCE

Solution 1: Réception AM à quartz



FS3.1: FILTRAGE HF

Permet de sélectionner des signaux émis sur la bande de fréquences 26MHz attribuée aux modèles réduits.

Entrée : Signaux radio-fréquences

Sortie : Signaux radio-fréquences attribués aux modèles réduits bande 26 MHz

FS3.2: AMPLIFICATION HF

Amplifie les signaux radio-fréquences

Entrée : Signaux radio-fréquences attribués aux modèles réduits

Sortie : Signaux radio-fréquences amplifiés

FS3.3: CHANGEMENT DE FREQUENCE

Pourquoi changer de fréquence?

La sélectivité des récepteurs ne peut pas s'obtenir dans les étages d'entrée accordés sur la fréquence reçue. Ces étages sont du type LC à bande passante bien trop large. La sélectivité est donc obtenue après changement de fréquence qui fait passer le signal HF à 455 kHz (fréquence intermédiaire = FI).
Sur cette fréquence basse, la sélectivité des bobines (1/50 F) est suffisante.

Entrées : - Signaux radio-fréquences amplifiés
- Quartz de fréquence telle que :
(fréquence à selectionnée) – (fréquence quartz) = 455 KHz = FI

Sortie : Signal de fréquence 455KHz modulé par l'emetteur sélectionné.

FS3.4: AMPLIFICATION ET FILTRAGE FI

Filtrage bande étroite et amplification

Entrée : Signal de fréquence 455KHz modulé par l'émetteur sélectionné.

Sortie : Signal de fréquence 455KHz modulé par l'émetteur sélectionné filtré et amplifié

FS3.5: DEMODULATION

Supprime la fréquence intermédiaire et restitue la trame PPM

Entrée : Signal de fréquence 455KHz modulé par l'émetteur sélectionné filtré et amplifié

Sortie : Trame PPM

FS3.6: CAG (CONTROLE AUTOMATIQUE DE GAIN)

Modifie automatiquement le gain de l'amplificateur FI en fonction du niveau de réception

Entrée : signal PPM

Sortie : signal électrique de commande de gain

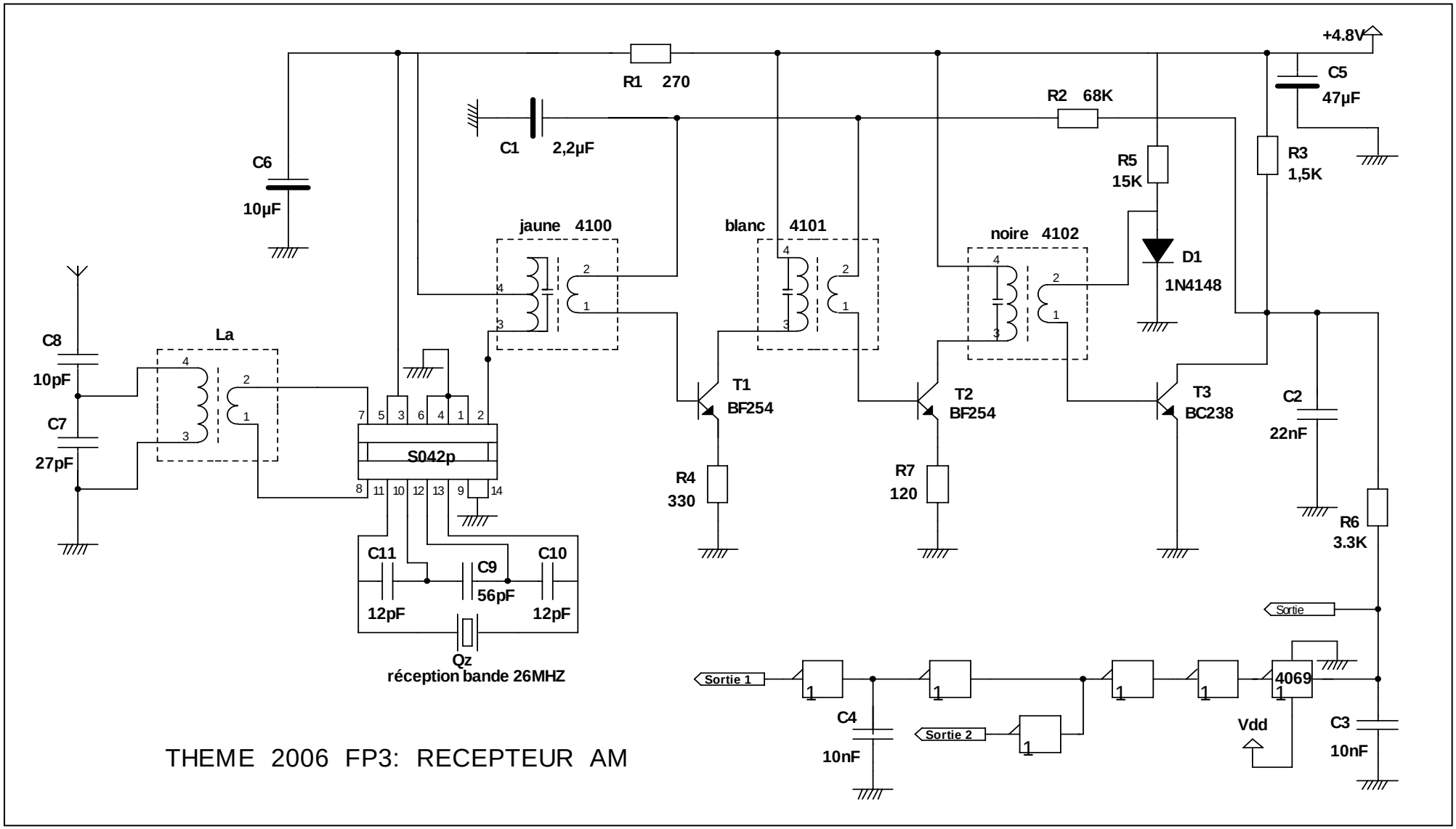
FS3.7: OSCILLATEUR LOCAL

Génère une fréquence très stable égale à celle de la fréquence émise moins 455 KHz

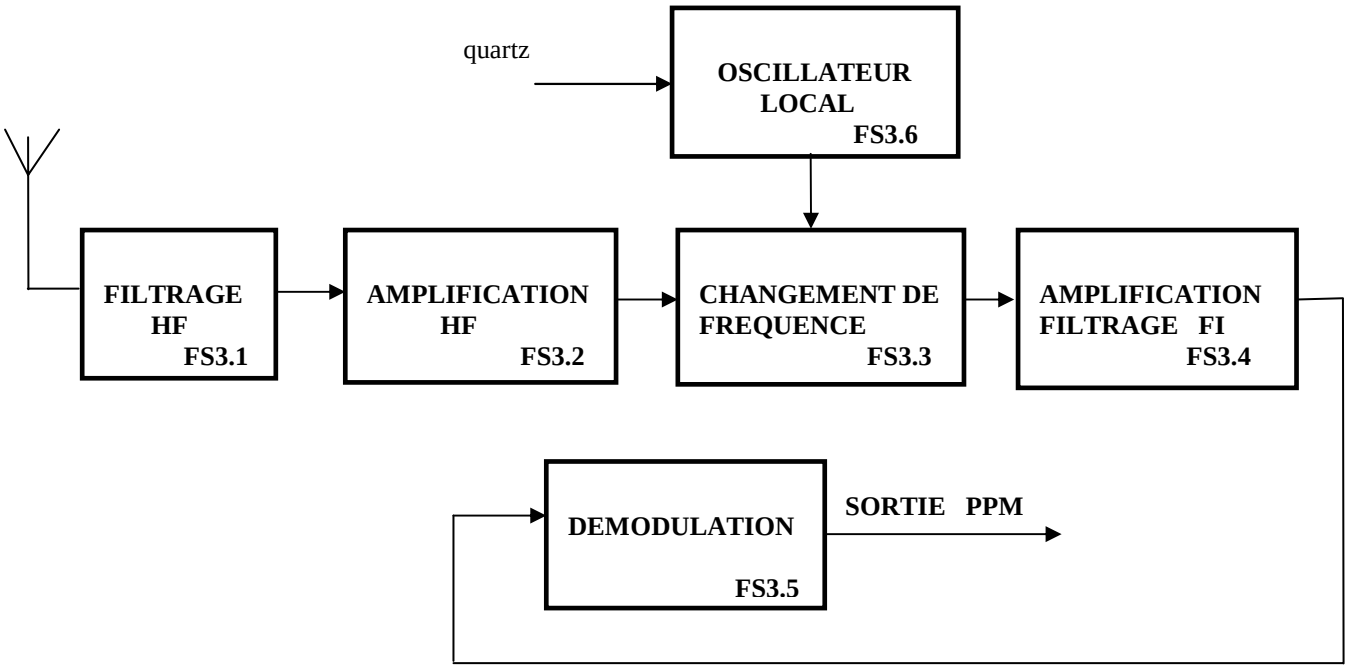
Entrée : Quartz de réception

Sortie : Fréquence stable du quartz de réception

SCHEMA STRUCTUREL



Solution 2: Réception FM à quartz



FS3.1: FILTRAGE HF

Permet de sélectionner des signaux émis sur la bande de fréquences 41MHz attribuée aux modèles réduits.

Entrée : Signaux radio-fréquences

Sortie : Signaux radio-fréquences attribués aux modèles réduits bande 41MHz

FS3.2: AMPLIFICATION HF

Amplifie les signaux radio-fréquences

Entrée : Signaux radio-fréquences attribués aux modèles réduits

Sortie : Signaux radio-fréquences amplifiés

FS3.3: CHANGEMENT DE FREQUENCE

Pourquoi changer de fréquence?

La sélectivité des récepteurs ne peut pas s'obtenir dans les étages d'entrée accordés sur la fréquence reçue. Ces étages sont du type LC à bande passante bien trop large. La sélectivité est donc obtenue après changement de fréquence qui fait passer le signal HF à 455 kHz (fréquence intermédiaire = FI). Sur cette fréquence basse, la sélectivité des bobines (1/50 F) est suffisante.

Entrées : Signaux radio-fréquences amplifiés
Fréquence oscillateur local
(fréquence à selectionnée) - (fréquence oscillateur local) = 455 KHz = FI

Sortie : Signal de fréquence 455KHz modulé par l'emetteur sélectionné.

FS3.4: AMPLIFICATION ET FILTRAGE FI

Filtrage bande étroite et amplification

Entrée : Signal de fréquence 455KHz modulé par l'émetteur sélectionné.

Sortie : Signal de fréquence 455KHz modulé par l'émetteur sélectionné filtré et amplifié

FS3.5: DEMODULATION

Supprime la fréquence intermédiaire et restitue la trame PPM

Entrée : Signal de fréquence 455KHz modulé par l'emetteur sélectionné filtré et amplifié

Sortie : Trame PPM

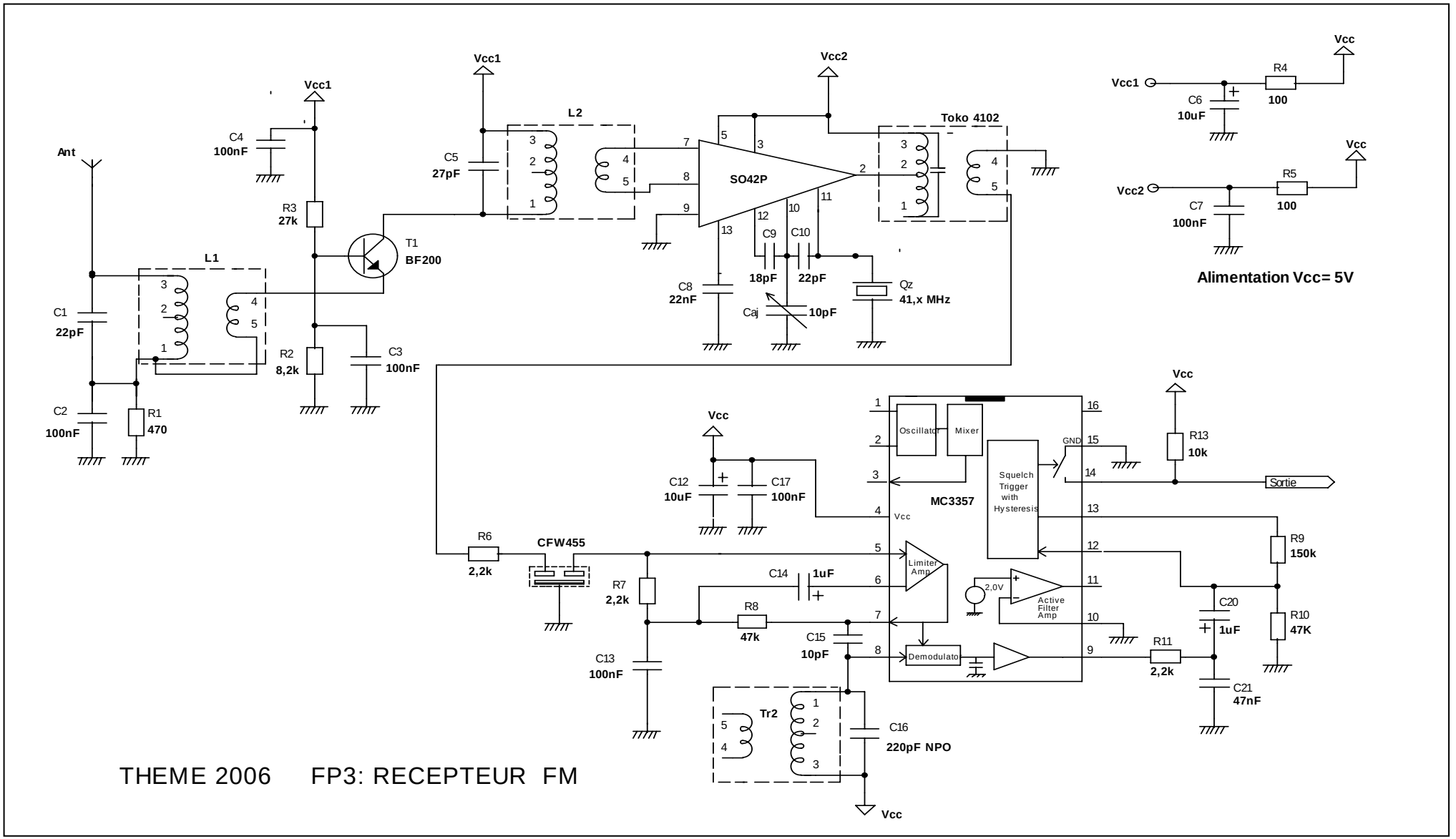
FS3.6: OSCILLATEUR LOCAL

Génère une fréquence très stable égale à celle de la fréquence émise moins 455 KHz

Entrée : Quartz de réception

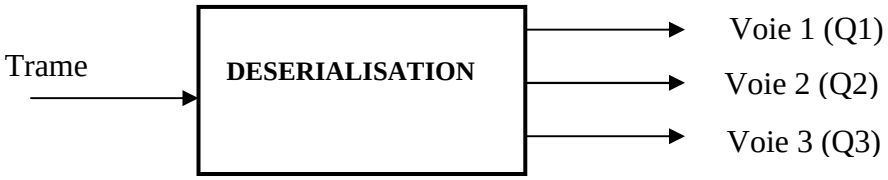
Sortie : Fréquence stable du quartz de réception

SCHEMA STRUCTUREL

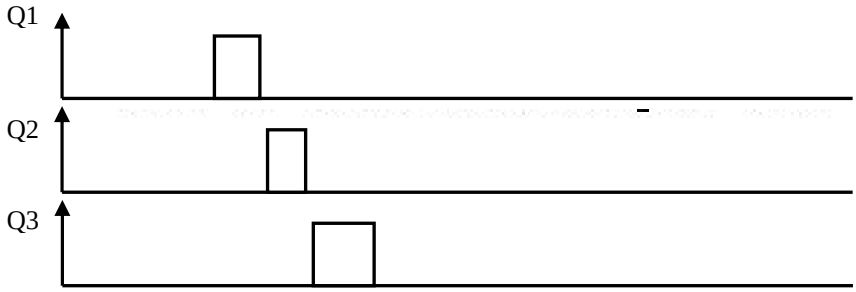


FP4: DECODAGE

Les deux solutions technologiques conduisent au même schéma fonctionnel.

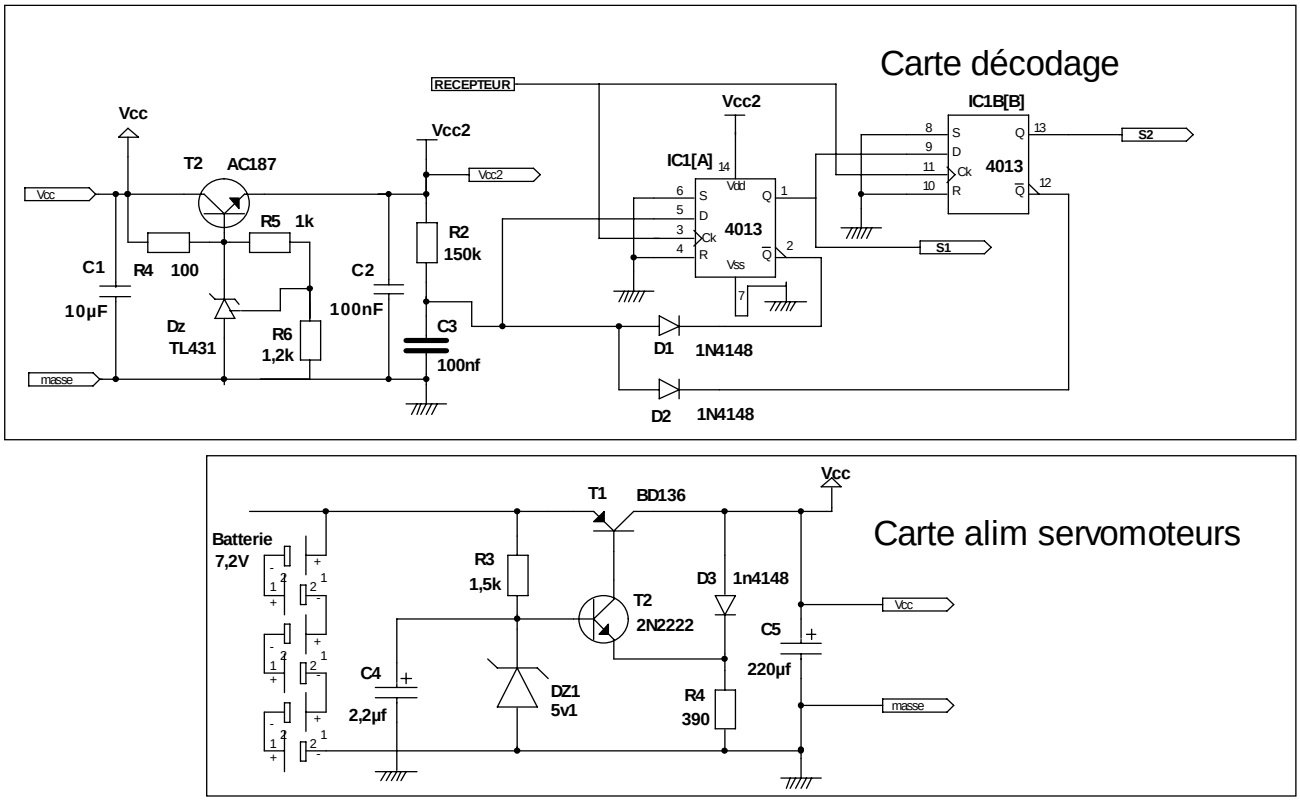


Trame PPM

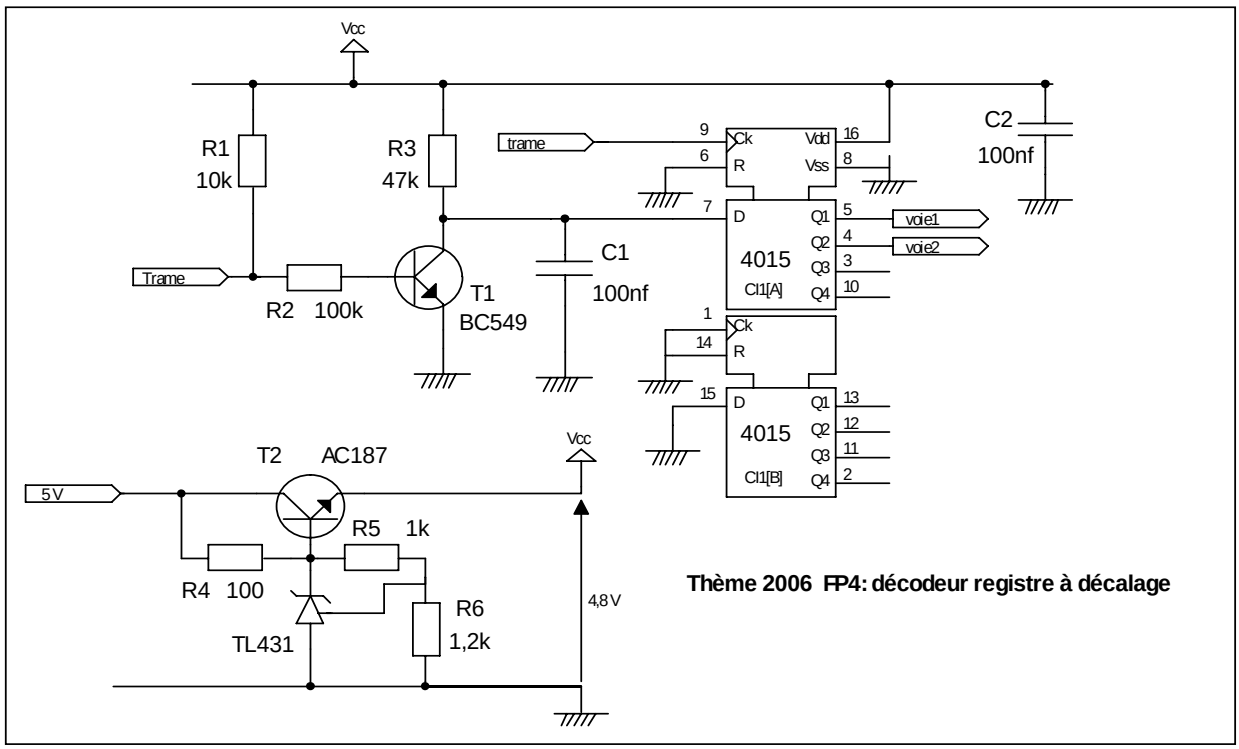


SCHEMA STRUCTUREL

Décodage à bascules D

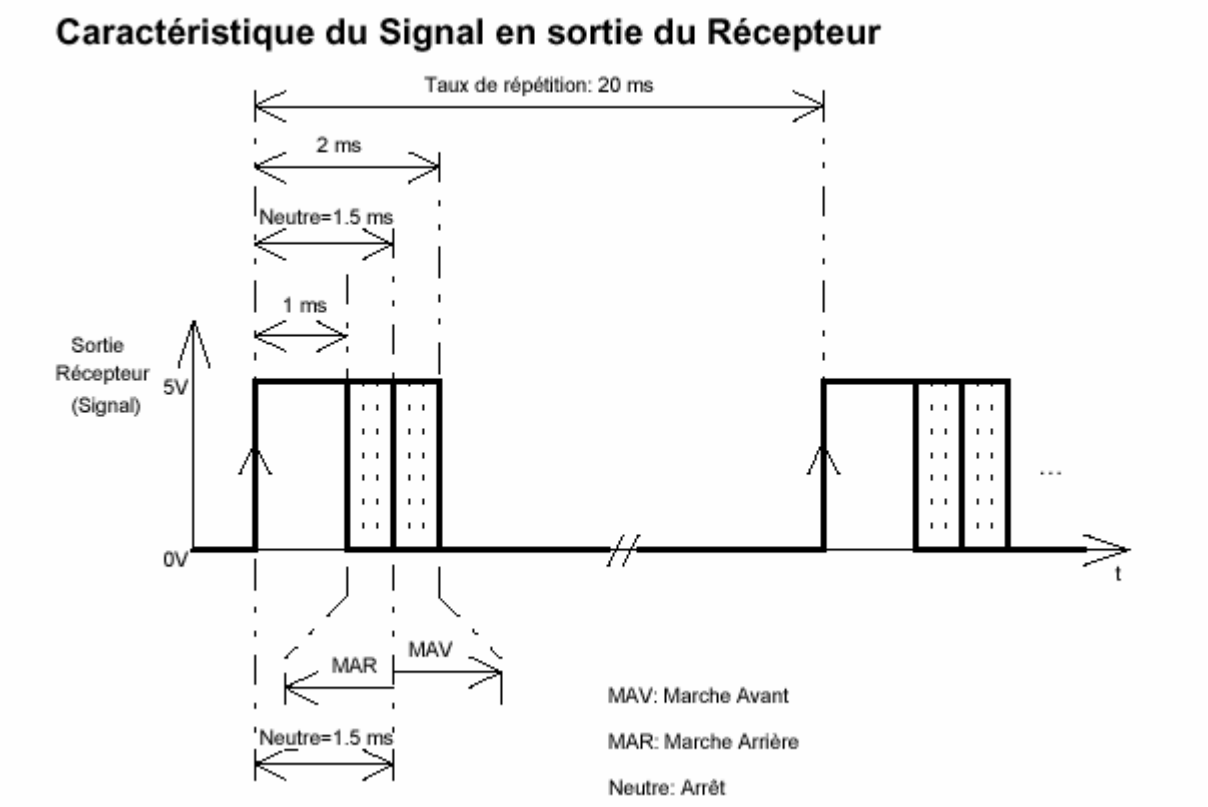


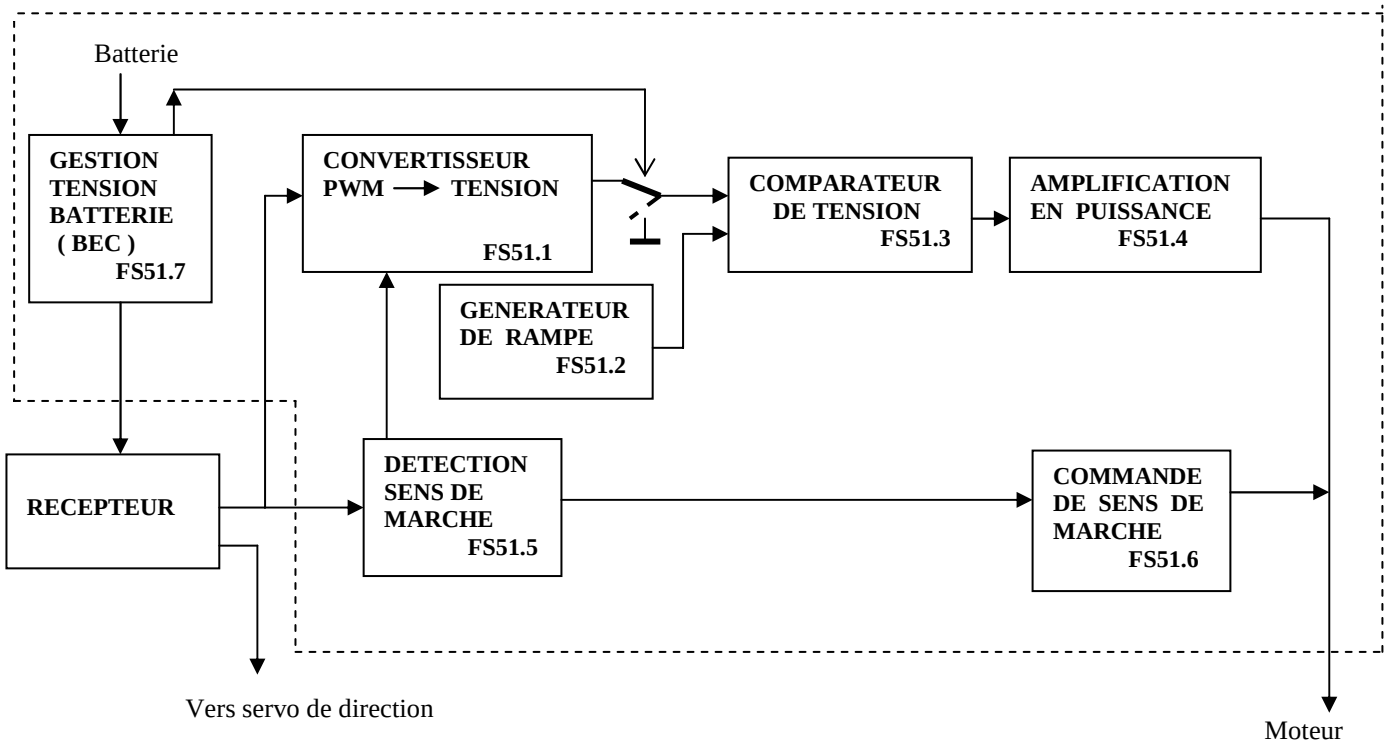
Décodage à registres à décalage.



FP5: ADAPTATION AUX ACTIONNEURS

FP51 : ADAPTATION AU MOTEUR DE PROPULSION
Variateur de vitesse





FS51.1: CONVERTISSEUR PWM ⟶ TENSION

Convertit la différence entre la durée de voie et la durée de neutre (1,5 ms) en une tension continue proportionnelle à la valeur absolue de cette différence.

Entrées : Durée de la voie vitesse se répétant toutes les 20 ms (Ds)
Durée du neutre

Sortie : Tension continue proportionnelle.

FS51.2: GENERATEUR DE RAMPE

Génère un signal triangulaire

Sortie : signal triangulaire de fréquence 1 KHz

FS51.3: COMPARATEUR DE TENSION

Par comparaison entre le signal triangulaire et le signal continue de FS51.1, génère un signal PWM (MLI) image de la vitesse souhaitée.

Entrées : Signal triangulaire de fréquence 1 KHz
Tension continue proportionnelle.

Sortie : Signal PWM commandant le régime moteur de 0 à 100%

FS51.4: AMPLIFICATEUR DE PUISSANCE

Amplifie le signal PWM pour l'adapter à la puissance du moteur

Entrée : Signal PWM

Sortie : Signal PWM amplifié

FS51.5: DETECTION SENS DE MARCHE

Par comparaison entre la durée de voie et le neutre, génère un niveau logique correspondant à un sens de marche du moteur

Entrée : Durée de la voie vitesse

Sortie : Niveau logique de sens

FS51.6: COMMANDE DE SENS DE MARCHE

Transforme le niveau logique de sens en ordre d'inversion de rotation.

Entrée : Niveau logique de sens

Sortie : Inversion du sens de rotation

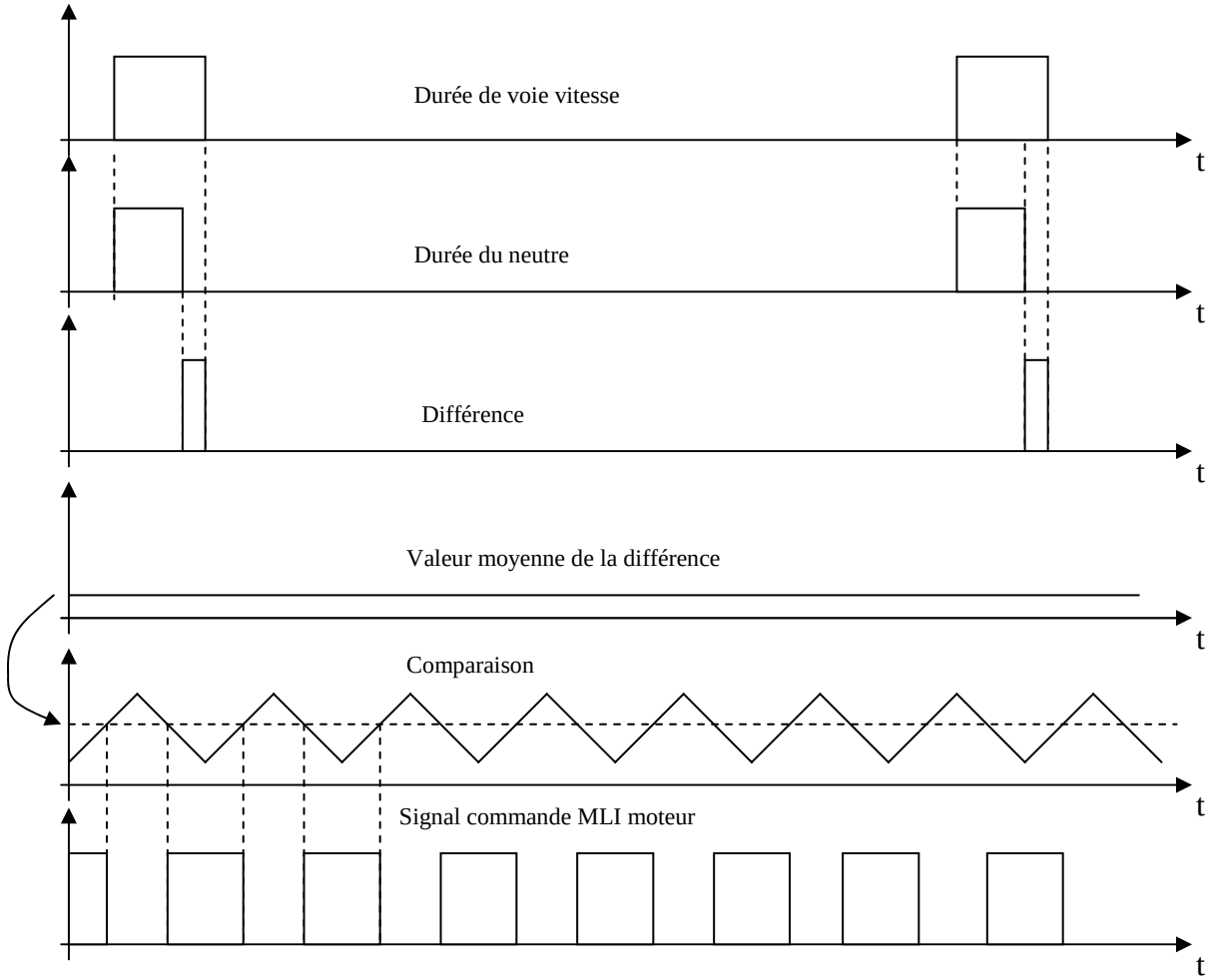
FS51.7: GESTION TENSION BATTERIE (BEC)

En cas de baisse de la tension batterie, coupe la commande de puissance tout en maintenant alimenté le récepteur.

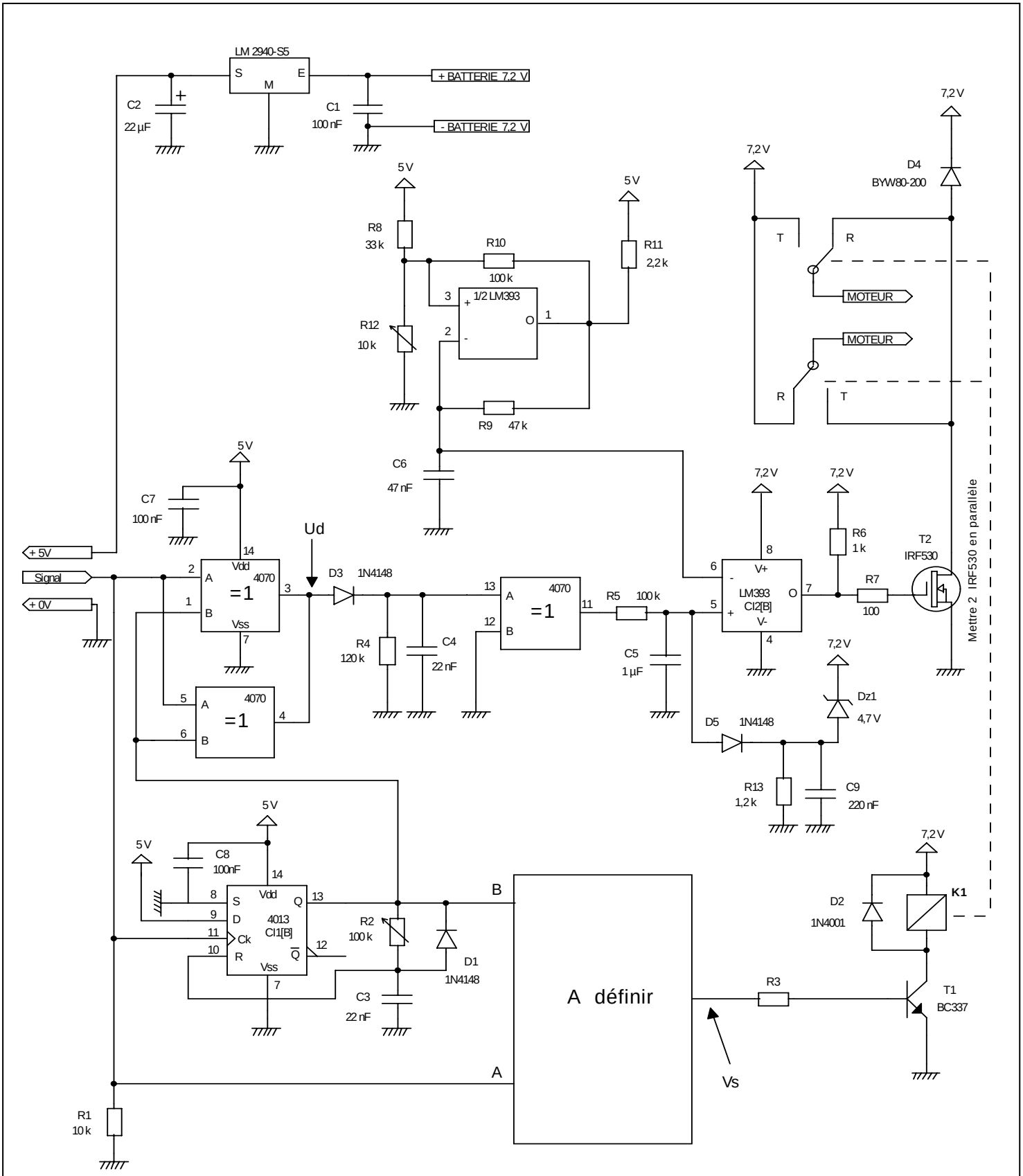
Entrée : Tension de batterie

Sortie : Annulation de la tension issu de la fonction FS51.1

CHRONOGRAMMES FONCTIONNELS DE PRINCIPE
(Structurel légèrement différent)



SCHEMA STRUCTUREL

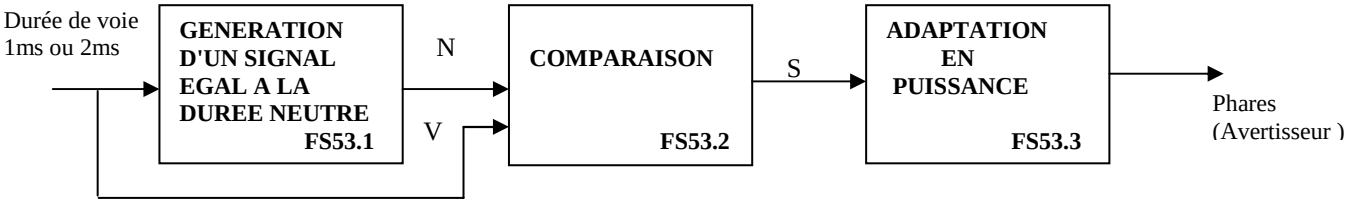


Thème 2006 FP51: Variateur de vitesse

FP52 : ADAPTATION A LA COMMANDE DE DIRECTION

Elle est assurée par un dispositif interne au servomoteur de direction

FP53 : ADAPTATION A LA COMMANDE DES PHARES OU DE L' AVERTISSEUR



FS53.1: GENERATION D'UN SIGNAL DE DUREE 1,5 ms

Génère un signal de durée égal à la durée du neutre en synchronisme avec le signal de voie.

Entrées : Durée de voie
1ms : Dévalider phares ou Avertisseur
2 ms: Valider phares ou Avertisseur

Sortie : Signal de durée de 1,5ms synchronisé avec la durée de voie

FS53.2: COMPARAISON

Compare la durée de neutre avec la durée de voie et affecte un niveau logique à la sortie S.
Durée N > Durée V ⟶ S = 0
Durée N < Durée V ⟶ S = 1

Entrées : Durée de voie
Durée de neutre

Sortie : Niveau logique résultat de la comparaison

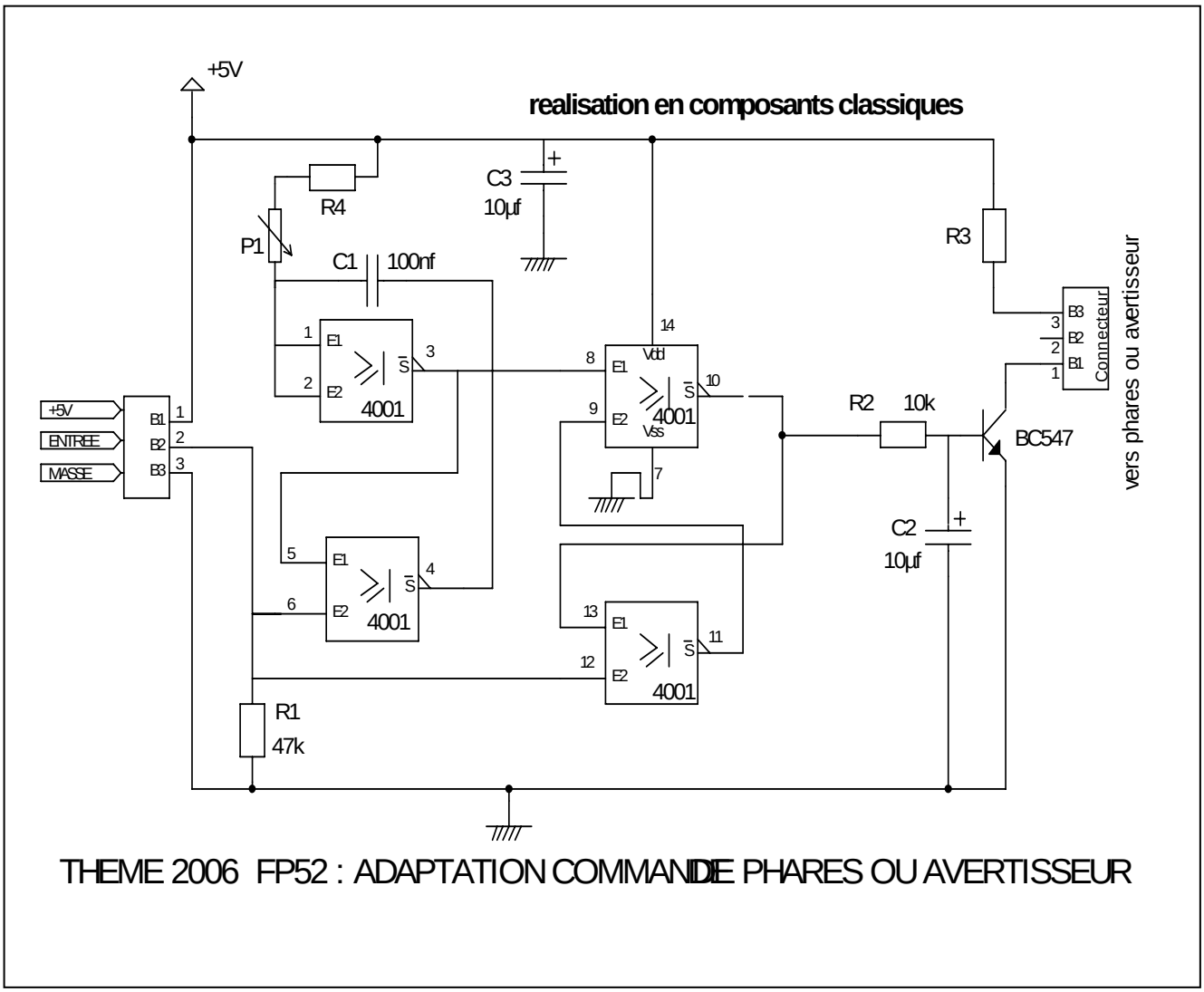
FS53.3: ADAPTATION EN PUISSANCE

Active ou désactive les phares (ou avertisseur) selon l'état de S.

Entrée : Niveau logique résultat de la comparaison

Sortie : Phares (ou avertisseur)

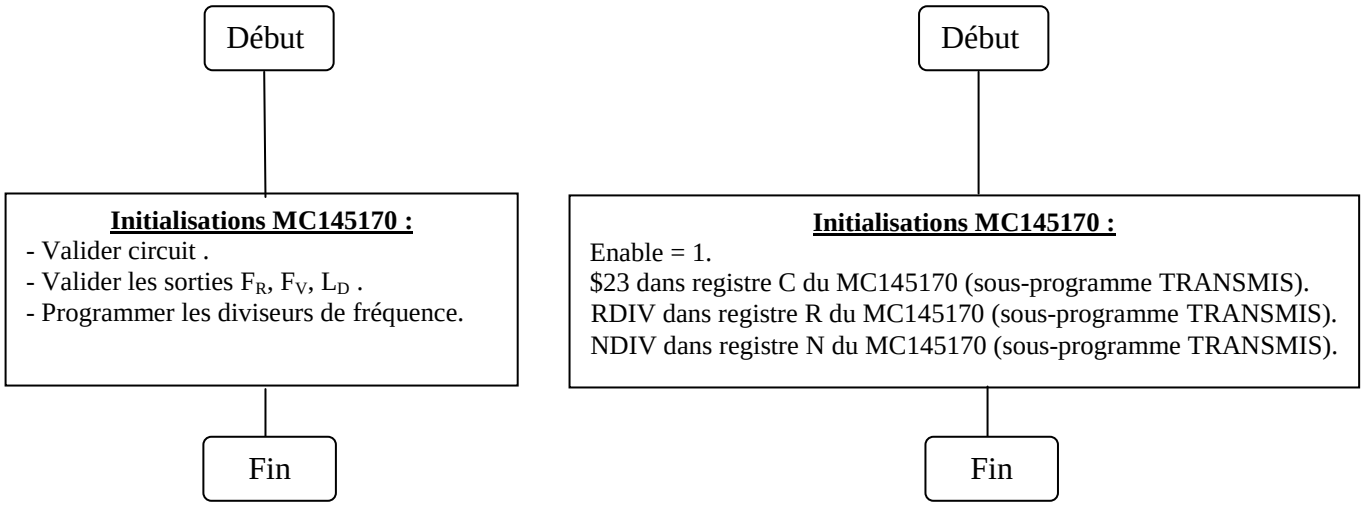
SCHEMA STRUCTUREL



THEME 2006 FP52 : ADAPTATION COMMANDE PHARES OU AVERTISSEUR

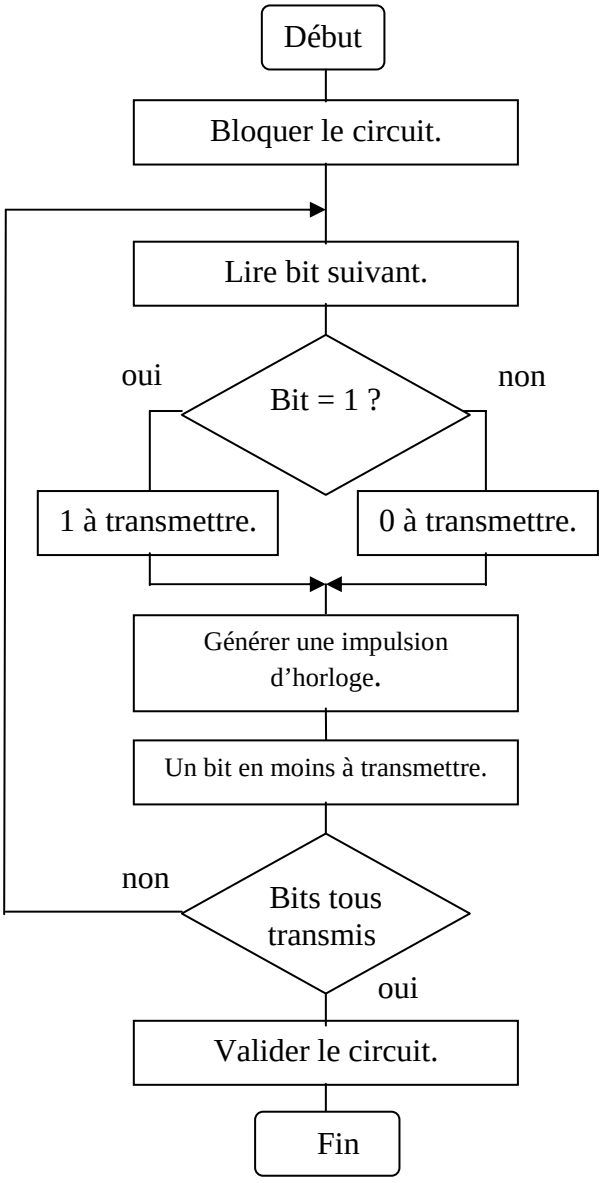
ALGORIGRAMMES:

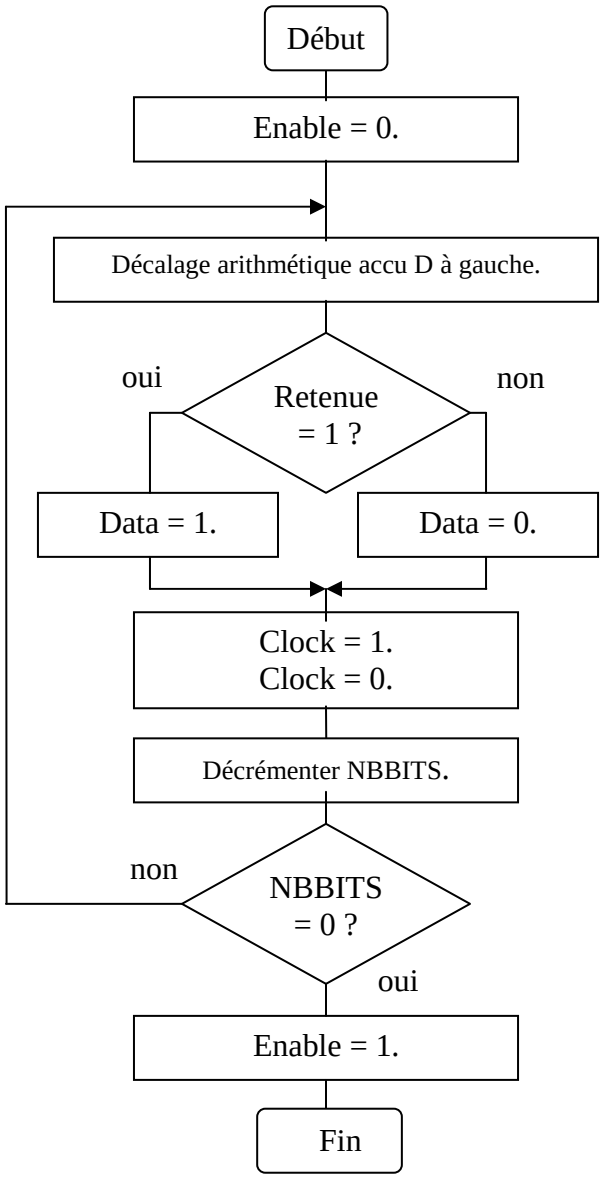
Programmation d'initialisation de la PLL



Programme de transmission des données au MC145170

Entrées : Accumulateur D, contient les données à transmettre, premier bit en position MSB ;
NBBITS, contient le nombre de bits à transmettre.





Remarque 1 : Tous les temps de propagation du MC145170 sont inférieurs à un cycle du 68HC11, ce qui explique que ce sous-programme ne comporte pas de temporisation.

Remarque 2 : Le choix du registre du MC145170 à programmer est effectué par le nombre d'impulsions d'horloge (8 pour le registre C, 15 pour R, 16 pour N).

Remarque 3 : RDIV = 10245/5 = 2049 donne F_R = 5 kHz. NDIV = FEMIS/5 permet de régler, quelle que soit FEMIS multiple de 5, F_V à 5 kHz pour vérrouiller la PLL avec $F_R = F_V$.

- Programme

```
* Configuration PLL

*                            Date : 10/06/2006

* Thème de baccalauréat 2006

* Permet la programmation en série du circuit MC145170
* de synthèse de fréquence.
*****************************************************************
*****************************************************************
* Description des Entrées/Sorties utilisées :
* Sorties :
* PB4, fournit le signal Clock pour la programmation du MC145170.
* PB2, fournit le signal Enable pour la programmation du MC145170.
* PB0, fournit le signal Data pour la programmation du MC145170.
*****************************************************************
```

PROGRAMME A DEFINIR PENDANT LE TP TOURNANT

IV -Travail demandé

CONSTITUTION DES GROUPES DE TRAVAIL :

L'étude du système radiopilotage de modélisme est répartie entre 6 groupes de travail (binôme). La coopération entre deux groupes de travail permet la réalisation d'un ensemble radiopiloté complet. Il existe 3 ensembles de technologies différentes. La coopération entre les différents groupes de travail est la suivante :

- Groupe 1 avec groupe 2 (Ensemble 1)
- Groupe 3 avec groupe 4 (Ensemble 2)
- Groupe 5 avec groupe 6 (Ensemble 3)

Groupe 1 : Emetteur FM à PLL (FP2 solution 2)
Codeur à monostable (FP1 solution 2)

Groupe 2 : Récepteur FM (FP3 solution 2)
Décodeur à registre à décalage (FP4 solution 2)
Adaptation aux actionneurs (FP53 : phares, avertisseur)

Groupe 3 : Emetteur AM à quartz (FP2 solution technologique 1)
Codeur à ALI (FP1 solution 3)

Groupe 4 : Récepteur AM à quartz (FP3 solution 1)
Décodage par bascule D (FP4 solution 1)
Adaptation aux actionneurs (FP53 : phares, avertisseur)

Groupe 5 : Emetteur AM à quartz (FP2 solution 1)
Codeur à comparateur (FP1 solution 1)
Décodeur à registre à décalage (FP4 solution 2)

Groupe 6: Récepteur AM à quartz (FP3 solution 1)
Adaptation aux actionneurs (FP51: variateur de vitesse)

REMARQUE IMPORTANTE RELATIVE A TOUS LES GROUPES

Les questions posées ne sont pas exhaustives. Elles sont un guide pour vous aider dans la compréhension de votre système et la rédaction de votre dossier.
Ce dernier ne devra donc pas se présenter comme une suite chronologique de réponses à ces questions

TRAVAIL COMMUN A TOUS LES GROUPES

- Etude, programmation et réglage de l'émetteur FM (partie PLL) selon TP tournant.

.

TRAVAIL GROUPE 1 :

- Connaissance fonctionnelle jusqu'au 1er degré de votre ensemble (2 groupes)
- Etude qualitative de vos fonctions
- Etude quantitative de vos fonctions (sauf émetteur et récepteur)
- Réalisations des maquettes
- ***Validation expérimentale : Test et relevés "commentés" de mesures (oscillogrammes etc. …..)***

- Assemblage de l'ensemble auquel vous appartenez (2 groupes) permettant un contrôle aisé par le jury.
- Rédaction d'un rapport comprenant les parties précédentes.
- Préparer un exposé oral en tenant compte de la grille d'évaluation qui vous sera présentée.

Conseil : La présentation fonctionnelle jusqu'au 1er degré ne doit pas excéder 5 mn pour l'épreuve orale.

Etude fonctionnelle:
Emetteur et codeur : Entourer les fonctions secondaires sur le structurel
Etude structurelle:
Qualitative:
Expliciter le rôle de chaque composant: 4528 (1 et 2) 4017, P1, P2, R2 et diodes.
Tracer les chronogrammes aux points :
broche 6 de 4528
broche 10 de 4528
Q0 de 4017
Q1 de 4017 (manche au max)
Q2 de 4017 (manche au mini)
Q3 de 4017

Qantitative:
Relever pour un montage monostable à base de 4528 la courbe tw=f(R) pour C=330nF et tw variant entre 0.6 et 2.3 ms.
En déduire R pour tw=1 ms , 1,5ms et 2 ms
Pour des manches de 10K, vérifier que les résistances ajustables choisies permettent d'atteindre ces valeurs.
En déduire une procédure de réglage de l'ensemble (P1 + manche ou P2 + manche)
Par extrapolation de la courbe, déduire R2 pour que Tsy = 8ms

Compléter (ou modifié) le schéma du codeur à monostable pour rajouter 2 voies tout ou rien (logiques) selon le principe suivant:

voie active: créneau de durée 2 ms

voie inactive: créneau de durée 1 ms

REALISATION ET ESSAIS

- Réalisation de l'émetteur FM à PLL (le typon est donné) et de ses bobines
- Réglages à l'aide du programme conçu pendant le TP tournant.
- Réaliser le typon du codeur, fabriquer la carte et procéder aux réglages
- Faire un ou plusieurs relevés expérimentaux (**oscillogrammes**) permettant de valider le fonctionnement

En collaboration avec le groupe 2 , assembler le système de pilotage radiocommandé.

TRAVAIL GROUPE 2 :

- Connaissance fonctionnelle jusqu'au 1er degré de votre ensemble (2 groupes)
- Etude qualitative de vos fonctions
- Etude quantitative de vos fonctions (sauf émetteur et récepteur)
- Réalisations des maquettes
- ***Validation expérimentale : Test et relevés "commentés" de mesures (oscillogrammes etc. …..)***

- Assemblage de l'ensemble auquel vous appartenez (2 groupes) permettant un contrôle aisé par le jury.
- Rédaction d'un rapport comprenant les parties précédentes.
- Préparer un exposé oral en tenant compte de la grille d'évaluation qui vous sera présentée.

Conseil : La présentation fonctionnelle jusqu'au 1er degré ne doit pas excéder 5 mn pour l'épreuve orale.

Etude fonctionnelle:

Récepteur FM, décodeur, adaptation aux actionneurs : Entourer les fonctions secondaires sur le structurel

Etude structurelle:

Récepteur:

Qualitative:

Expliciter le principe de la démodulation FM utilisé par le MC3357.

En fonction de la fréquence d'émission, choisir et justifier le choix de la fréquence du quartz associé au SO42P.

Décodeur:

Qualitative:

Expliciter le rôle de chaque composants constituant le décodeur et l'alimentation.

Expliquer le principe de la stabilisation de l'alimentation.

Pour une suite de deux trames de 2 voies représenter les chronogrammes de :

- Collecteur de bc549
- Q1 du 4015
- Q2 du 4015
- Q3 du 4015
- Q4 du 4015

Quantitative:

Justifier la valeur de tous les composants du décodeur et de l'alimentation.

Compléter (ou modifier) le schéma du décodeur à registre à décalage pour disposer de 2 voies supplémentaires.

Adaptation aux actionneurs :

Qualitative:

Pour une suite de 3 signaux de voie de 1 ms puis de 3 signaux de voie de 2 ms arrivant sur Entrée, représenter les chronogrammes de:

- broche 6 du 4001
- broche 4 du 4001
- broches 1-2 du 4001
- broche 3 du 4001
- broche 10 du 4001
- broche 11 du 4001
- Base du BC547 (sortie de R2)

Quantitative

Calculer (R4 + P1) et les choisir

Calculer R3 pour l'actionneur choisi (2 DEL ou un buzzer) et vérifier que le BC547 est bien saturé.

REALISATION ET ESSAIS

- Réalisation du récepteur FM (le typon est donné) et de ses bobines
- Réglages en utilisant l'émetteur du TP et le programme modulation.
- Réalisation du typon du décodeur 4 voies, fabrication de la carte et essai
- Réalisation du typon adaptation aux actionneurs, fabrication de 2 cartes et essai
- Faire un ou plusieurs relevés expérimentaux (**oscillogrammes**) permettant de valider le fonctionnement de vos ensembles.

En collaboration avec le groupe 1, assembler le système de pilotage radiocommandé.

TRAVAIL GROUPE 3 :

- Connaissance fonctionnelle jusqu'au 1er degré de votre ensemble (2 groupes)
- Etude qualitative de vos fonctions
- Etude quantitative de vos fonctions (sauf émetteur et récepteur)
- Réalisations des maquettes
- ***Validation expérimentale : Test et relevés "commentés" de mesures (oscillogrammes etc. …)***

- Assemblage de l'ensemble auquel vous appartenez (2 groupes) permettant un contrôle aisé par le jury.
- Rédaction d'un rapport comprenant les parties précédentes.
- Préparer un exposé oral en tenant compte de la grille d'évaluation qui vous sera présentée.

Conseil : La présentation fonctionnelle jusqu'au 1er degré ne doit pas excéder 5 mn. pour l'épreuve orale.

Etude fonctionnelle:

Emetteur AM et codeur : Entourer les fonctions secondaires sur le structurel.

Etude structurelle:

FS1.1, FS1.2 et FS1.3:

Tracer Vs= f(AB) pour le manche vitesse en position extrême haute et le manche direction en position extrême basse avec P1= P2 = 7 K .
(AB prenant les valeurs 00,01,10, 00)
Commenter et conclure.

FS1.4: Générateur de rampe

Par étude théorique,ou sur labdec,ou en simulation,
tracer ou relever VR = f(t) pour Vi=0 et VTsy=0
Quel est l'effet de P3 sur VR
Tracer ou relever VR = f(t) pour Vi=Vcc et VTsy=0
Tracer ou relever VR = f(t) pour Vi=0 et VTsy=Vcc
Commenter et conclure.

FS1.5: Conversion Tension-durée

Par étude théorique, sur labdec ou en simulation,
tracer ou relever V2 = f(VR) pour V1=7V et Vi=0
Tracer ou relever V2 = f(VR) pour V1=7V et Vi=Vcc
Tracer en concordance de phase, V2, VR et V1 pour manche 1 en position neutre et manche 2 en position mini. On respectera les durées théoriques.
Commenter et conclure.

FS1.6: Génération d'une impulsion calibrée de 300µs

Par étude théorique,ou sur labdec,ou en simulation
V2 étant à Vcc, tracer ou relever Vi et V- du LM3900 pour un passage à 0 de V2 pendant un temps supérieur ou égal à 5 RC.
Quel est l'effet de P4 sur V2
Commenter et conclure.

FS1.7, FS1.8 et FS1.9

Par étude théorique,
Tracer en concordance de temps,CLK, Q1, Q2, V3 et Reset du 4024 .
Quel est le rôle des diodes.
Commenter et conclure.

Etude de FP1 complet:

Tracer en concordance de temps V1, VR, V2, Vi, Vsortie, V3, VTsy pour manche vitesse en position extrême haute (Vcc) et manche direction en position extrême basse (0V). On s'efforcera de respecter les valeurs temporelles.
Définir une procédure de réglage des différentes résistances ajustables.
Calculer R20 pour obtenir le Tsy désiré.
Calculer la valeur théorique de P4 pour obtenir le temps d'inter-voie désiré.

REALISATION ET ESSAIS

- Réalisation de l'émetteur AM (le typon est donné) et de sa bobine.
- Réglages

- Compléter (ou modifié) le schéma du codeur à ALI pour rajouter 2 voies tout ou rien (logiques) selon le principe suivant:
  voie active: créneau de durée 2 ms
  voie inactive: créneau de durée 1 ms
- Réaliser le typon et fabriquer la carte
- Faire un ou plusieurs relevés expérimentaux (**oscillogrammes**) permettant de valider le fonctionnement de vos ensembles.
- En collaboration avec le groupe 4, assembler le système de pilotage radiocommandé.

TRAVAIL GROUPE 4 :

- Connaissance fonctionnelle jusqu'au 1er degré de votre ensemble (2 groupes)
- Etude qualitative de vos fonctions
- Etude quantitative de vos fonctions (sauf émetteur et récepteur)
- Réalisations des maquettes
- ***Validation expérimentale : Test et relevés "commentés" de mesures (oscillogrammes etc. …..)***

- Assemblage de l'ensemble auquel vous appartenez (2 groupes) permettant un contrôle aisé par le jury.
- Rédaction d'un rapport comprenant les parties précédentes.
- Préparer un exposé oral en tenant compte de la grille d'évaluation qui vous sera présentée.
  Conseil : La présentation fonctionnelle jusqu'au 1er degré ne doit pas excéder 5 mn. pour l'épreuve orale.

Etude fonctionnelle:
Récepteur AM, décodeur, adaptation aux actionneurs : Entourer les fonctions secondaires sur le structurel

Etude structurelle:

Récepteur AM:

Qualitative:

Expliciter le principe de la démodulation AM utilisée.
En fonction de la fréquence d'emission, choisir et justifier le choix de la fréquence du quartz associé au SO42P.

Décodeur:

Qualitative:

Expliciter le rôle de chaque composants constituant le décodeur et l'alimentation.
Pour une suite de deux trames de 2 voies représenter les chronogrammes de:

- broche 1 du 4013
- broche 2 du 4013
- broche 13 du 4013
- broche 12 du 4013
- Tension aux bornes de C3

Quantitatif:
Justifier les valeurs de R2 et C3.
Expliciter le principe de la stabilisation de l'alimentation du décodeur.

Carte alimentation servomoteur :

Déterminer la valeur précise de Vcc.

Expliciter le principe de la régulation.

REALISATION ET ESSAIS

- Réalisation du récepteur AM (le typon est donné).
- Réglages
- Compléter (ou modifié) le schéma du décodeur à bascules D pour disposer de 2 voies supplémentaires
- Réaliser le typon et fabriquer la carte
- Réaliser le typon des cartes phares et avertisseur et les fabriquer.
- Réaliser le typon de la carte alimentation servomoteur en 2 exemplaires. (pour le groupe 1 et 2)

TRAVAIL GROUPE 5 :

- Connaissance fonctionnelle jusqu'au 1er degré de votre ensemble (2 groupes)
- Etude qualitative de vos fonctions
- Etude quantitative de vos fonctions (sauf émetteur et récepteur)
- Réalisations des maquettes
- ***Validation expérimentale : Test et relevés "commentés" de mesures (oscillogrammes etc. …..)***

- Assemblage de l'ensemble auquel vous appartenez (2 groupes) permettant un contrôle aisé par le jury.
- Rédaction d'un rapport comprenant les parties précédentes.
- Préparer un exposé oral en tenant compte de la grille d'évaluation qui vous sera présentée.

Conseil : La présentation fonctionnelle jusqu'au 1er degré ne doit pas excéder 5 mn. pour l'épreuve orale.

Etude fonctionnelle:

Emetteur AM, codeur à comparateur, décodeur avec registre à décalage : Entourer les fonctions secondaires sur le structurel.

Etude structurelle:

Codeur à comparateur:

Qualitative:

Expliquer le principe de fonctionnement de l'alimentation.

Calculer la constante de temps de circuit R7 et C4

Exprimer Uc_5 en fonction de Vcc_2 pour manette de commande sens en position haute (pour les valeurs du schéma)

Exprimer Uc_{10} en fonction de Vcc2 pour manette de commande direction en position repos.

Sachant que la sortie patte 7 du LM324 délivre un signal rectangulaire de période 20ms et considérant R10 = R7, tracer en respectant sommairement les échelles de temps et de tension:

- broche 7 du LM324
- U_{R5}
- U_{c4} et U_{c5} pour manette sens en position haute
- Broche 1 du LM324
- U_{R8}
- U_{C8} et U_{c10} pour manette direction position repos
- Broche 14 du LM324
- U_{R11}
- U_{R23} et U_{R13}
- Broche 8 du LM324

Quantitative:
Sachant que lorsqu'une manette est au repos, la durée de voie doit être de 1,5ms,
Déterminer graphiquement ou par calcul la valeur de U_{C5}
En déduire la valeur de Vcc_2 et le rôle de P1.
En fonction de la valeur du potentiomètre de vos manettes et de la course de ces dernières, dimensionner Rc1, Rc2, Rc3 et Rc4 de façon à ce que les positions extrêmes des manettes conduisent à une durée de voie >= à 2ms et <=1ms
Justifier le choix d'une résistance ajustable pour R10.
Justifier les valeurs des composants du montage astable (FS1.1).

Décodeur:

Qualitative:
Expliciter le rôle de chaque composants constituant le décodeur et l'alimentation.
Expliquer le principe de la stabilisation de l'alimentation.
Pour une suite de deux trames de 2 voies représenter les chronogrammes

- Collecteur de BC549
- Q1 du 4015
- Q2 du 4015
- Q3 du 4015
- Q4 du 4015
-

Quantitative:
Justifier la valeur de tous les composants du décodeur et de l'alimentation.
Compléter (ou modifier) le schéma du décodeur à registre à décalage pour disposer de 2 voies supplémentaires.

REALISATION ET ESSAIS

- Réalisation de l'émetteur AM (le typon est donné) et de sa bobine.
- Réglages
- Compléter (ou modifier) le schéma du codeur à comparateur pour rajouter 2 voies tout ou rien (logiques) selon le principe suivant:
  voie active: créneau de durée 2 ms
  voie inactive: créneau de durée 1 ms
- Réaliser le typon et fabriquer la carte

- Compléter (ou modifié) le schéma du décodeur à registre à décalage pour disposer de 2 voies supplémentaires
- Réaliser le typon et fabriquer la carte

TRAVAIL GROUPE 6 :

- Connaissance fonctionnelle jusqu'au 1er degré de votre ensemble (2 groupes)
- Etude qualitative de vos fonctions
- Etude quantitative de vos fonctions (sauf émetteur et récepteur)
- Réalisations des maquettes
- ***Validation expérimentale : Test et relevés "commentés" de mesures (oscillogrammes etc. …..)***

- Assemblage de l'ensemble auquel vous appartenez (2 groupes) permettant un contrôle aisé par le jury.
- Rédaction d'un rapport comprenant les parties précédentes.
- Préparer un exposé oral en tenant compte de la grille d'évaluation qui vous sera présentée.

Conseil : La présentation fonctionnelle jusqu'au 1er degré ne doit pas excéder 5 mn. pour l'épreuve orale.

Etude fonctionnelle:

Récepteur AM, décodeur, adaptation aux actionneurs : Entourer les fonctions secondaires sur le structurel

Etude structurelle:

Récepteur AM:

Qualitative:

Expliciter le principe de la démodulation AM utilisée.

En fonction de la fréquence d'émission, choisir et justifier le choix de la fréquence du quartz associé au SO42P.

Adaptation aux actionneurs: Variateur de vitesse

Etude qualitative:

FS51.1, FS51.2 et FS51.3

Pour un signal d'entrée de 1ms puis de 2ms, tracer Ud.

Sur labdec ou en simulation, pour un signal d'entrée de 1ms puis 2ms, relever les signaux Vc4 et Vc5.

En déduire: - le rôle de la structure composé de D3, R4 et C4.
- les seuils de basculement de FS51.2.

Pour un signal d'entrée de 1,2ms puis de 1,8ms, tracer les chronogrammes, en régime établi de:

- signal d'entrée
- broche 13 de 4013
- broche 3 de 4070
- broches 5 et 6 de LM393
- broche 7 de LM393

FS51.4, FS51.6

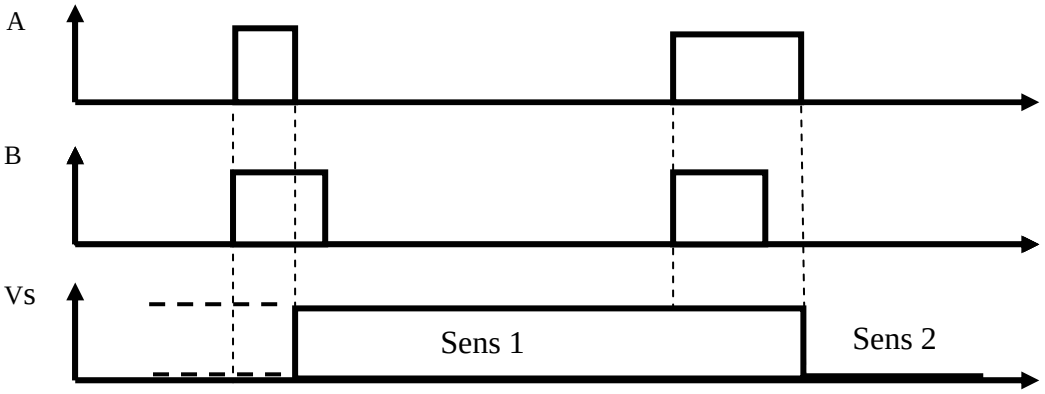
Les contacts du relais étant représentés au repos tracer le chemin du courant de puissance pour Vs = Vcc et Vs = 0.

En déduire la position de la diode par rapport au moteur ainsi que son rôle.

Etude quantitative:

FS51.5:

Trouver le schéma structurel permettant de satisfaire aux chronogrammes de fonctionnement suivant:



Justifier la valeur des composants de FS51.2

Calculer R3 pour le relais en votre possession

Calculer la valeur théorique de R2 et justifier le choix du potentiomètre.

Rédiger une procédure d'essai et réglage de la carte

REALISATION ET ESSAIS

- Réalisation du récepteur AM (le typon est donné).
- Réglages
- Réalisation du typon et fabrication de la carte du variateur de vitesse.

PROPOSITION DE PLAN POUR VOTRE RAPPORT :

Le rapport devra comporter environ 30 pages hors annexe. En annexe, ne pourront figurer que les documents constructeurs indispensables à la compréhension du rapport. Il devra comporter un sommaire et les pages devront être numérotées. Le dossier peut être manuscrit.

Le rapport pourra suivre le plan suivant:

La partie présentation n'apparaît pas dans le dossier mais doit être parfaitement connue pour l'épreuve orale.

1. Etude fonctionnelle de 1er degré des objets techniques.
- Schémas fonctionnels de 1er degré.
- Explications des fonctions principales.
- Définitions des liaisons.

2. Explications à propos des fonctions étudiées.
- Position et justification de la présence des fonctions au sein du système ;
- Schéma fonctionnel de 2nd degré des fonctions principales ;
- Schémas structurels avec repérage des fonctions secondaires ;
- Définitions des liaisons ;
- Etude détaillée de chaque fonction secondaire qui peut comporter par exemple :
- Schéma structurel de la fonction secondaire ;

- Explications du fonctionnement de la fonction secondaire ;
- Calcul ou justification des composants ;
- Définitions des points tests ;
- Chronogrammes théoriques et/ou oscillogrammes ;
- Algorithme de fonctionnement ;
- Programme de test ;
- Etc…
- Méthode de mise en œuvre des cartes ;
- Relevés des mesures.

3. Algorithme et programmation éventuels des cartes étudiées.

4. Documents de fabrication.
- Schémas structurels (réalisés par le binôme) et nomenclatures.
- Typons avec identification des faces et schémas d'implantation.
- Plan de câblage (définition de la connectique).

5. Annexe : Documentations des fabricants de composants.

V- DOCUMENTS ANNEXES

CONSEIL A SUIVRE POUR LA REALISATION DE VOS CARTES

La dimension des cartes de l'ensemble réception devra permettre leur implantation sur la voiture modèle réduit.

Soyez attentif à la liste du matériel dont le typon n'est pas donné, certains composants sont de type CMS.

Mettre le maximum de pistes sur une face, l'autre face étant réservée pour le plan de masse.

Pour l'ensemble émetteur - codeur et l'ensemble récepteur – décodeur, relier les plans de masse par de courts morceaux de tresse.

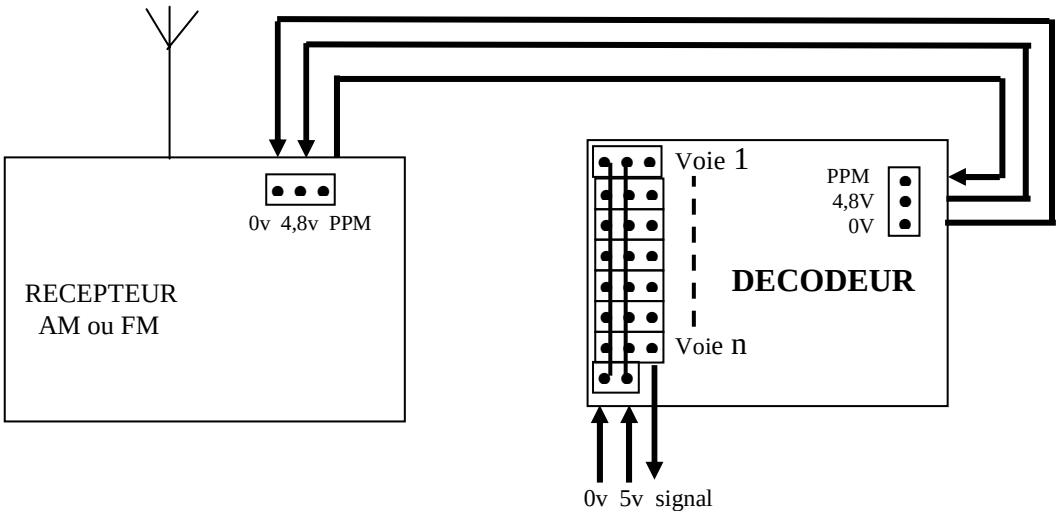
Toutes les liaisons doivent être les plus courtes possibles. Elles se feront par des fils soudés ou, pour des liaisons démontables, par des cordons radios type FUTUBA
(voir catalogue Electronique – Diffusion ou récupération sur vieux PC) .

Dans un même typon ou dans deux cartes voisines, éviter la proximité des signaux BF et entrée ou sortie antenne.

Pour l'émetteur, de préférence fixer l'antenne directement sur la carte, sinon la relier par un court morceau de fil blindé.

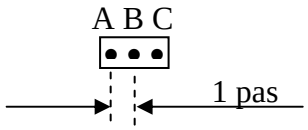
Liaisons des alimentations entre la carte réception AM ou FM, le décodeur et les cartes actionneurs

Pour GROUPE 2 et 4



Entrées alimentations fournies par la carte alim. servo-moteur ou par la sortie alimentation variateur de vitesse (si elle existe)

Connecteur :

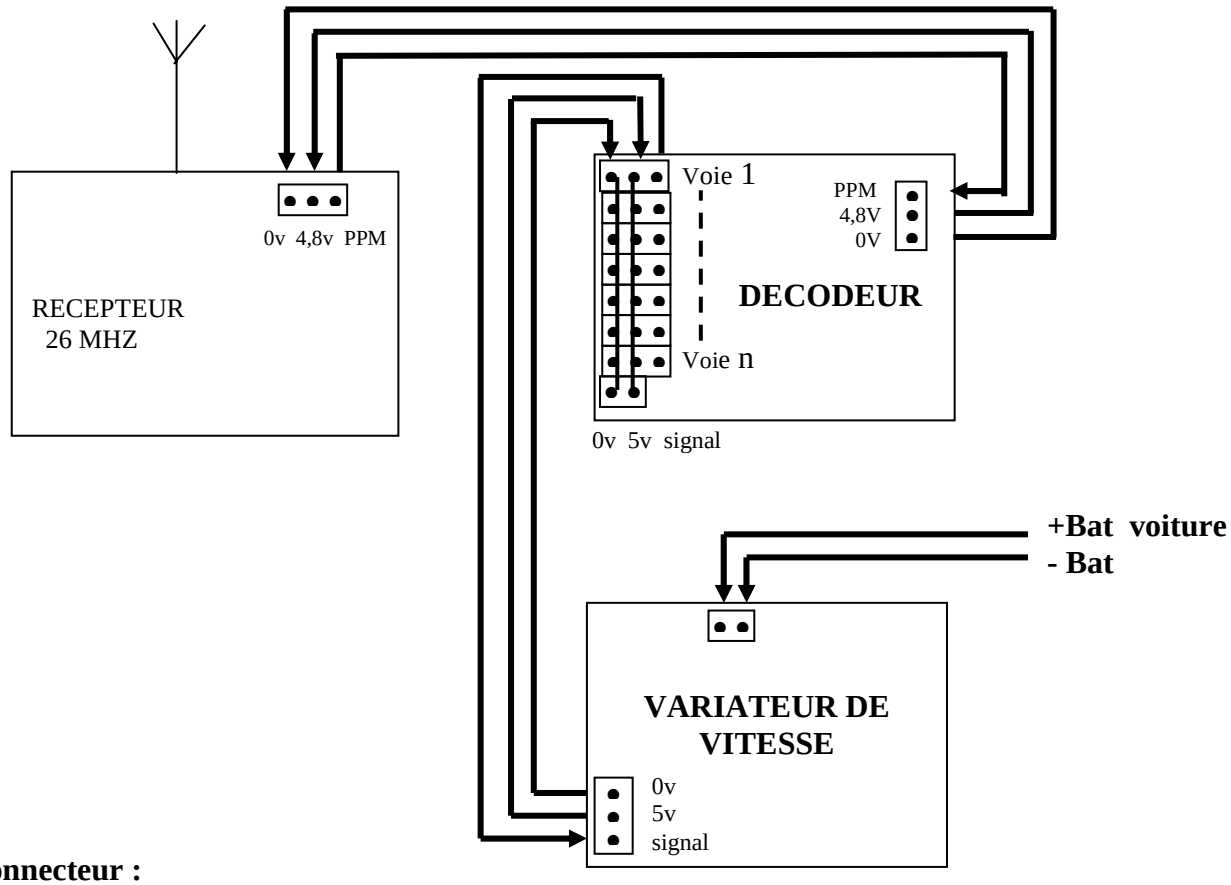


Pour les servo-moteurs: A = fil noir (masse)
B = fil rouge (+ alim.)
C = autre couleur dépendant du fabricant du servo-moteur.

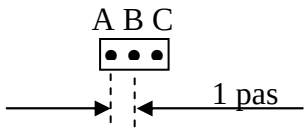
Branchement des différentes voies:
Voie 1 : variateur de vitesse de la voiture
Voie 2 : servo-moteur de direction
Voie 3 : Phares
Voie 4 : Avertisseur

Liaisons des alimentations entre la carte réception AM, le décodeur et le variateur de vitesse

Pour GROUPE 6



Connecteur :



Pour les servo-moteurs: A = fil noir (masse)
B = fil rouge (+ alim.)
C = autre couleur dépendant du fabricant du servo-moteur.

Branchement des différentes voies:
Voie 1 : variateur de vitesse
Voie 2 : servo-moteur de direction
Voie 3 : Phares
Voie 4 : Avertisseur

L'alimentation du décodeur est fournie par le variateur de vitesse.
L'alimentation du récepteur est fournie par le décodeur

CARACTERISTIQUES DES BOBINES A REALISER

Les bobines 41 MHz utilisent les ensembles 7T1K de NEOSID

Carte Emetteur FM à synthèse de fréquence : (cs = couche soie)

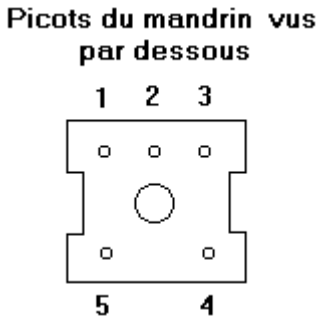
L1 : 10 spires 1/2 de 30/100 2cs (3-1) prise à 2 sp 1/4 (5)

L2 : P = 7 sp 1/4 de 30/100 2cs (1-3) ; S = 2 sp 1/4 même fil (4-5)

L3 : 5 spires 1/4 de 30/100 2cs (1-3)

L4 : 6 spires 1/4 de 30/100 2cs (1-3) - Pas de coupelle ni de blindage

L5 : 20 spires 15/100 émail (1-3) - Pas de coupelle ni de blindage



NB :
L'indication (1-3) indique que l'enroulement commence au picot 1 et se termine au picot 3 .
Dans cette vue, les enroulements tournent dans le sens horaire

Pour les enroulements nous utilisons du fil 30/100 2 couches soies pré-étamé (2 cs).
Ce fil peut cependant être émaillé ordinaire.

Pour la bobine L2, commencer par le secondaire, au bas du mandrin, puis à côté, bobiner le primaire.

Pour réussir ces bobines , il faut disposer d'une bobineuse rudimentaire constituée d'une simple manivelle installée sur deux paliers et terminée par une filetage de 3mm ISO. Les mandrins sont vissés sur ce filetage . Les fils sont accrochés sur les picots par une petite boucle. Le bobinage terminé, déposer le mandrin et coller les spires à la colle cellulosique.
La colle sèche, procéder au décapage des fils et à leur soudure sur les picots. Si le fil est émaillé, procéder d'abord à son étamage. (l'émail est généralement thermo-soudable).

Carte Récepteur FM :

L1 : 10 spires 1/2 de 30/100 2cs (3-1) prise à 3 sp 1/4 (5)
L2 : P = 10 sp 1/4 de 30/100 2cs (1-3) ; S = 3 sp 1/4 22/100 émail (4-5)
TR2 : 6 couches de spires jointives de 7/100 émail (1-3)

LES PRINCIPES DE LA RADIOCOMMANDE POUR MODELE REDUIT

Signaux échangés, codage, décodage, émission, réception, actionneurs

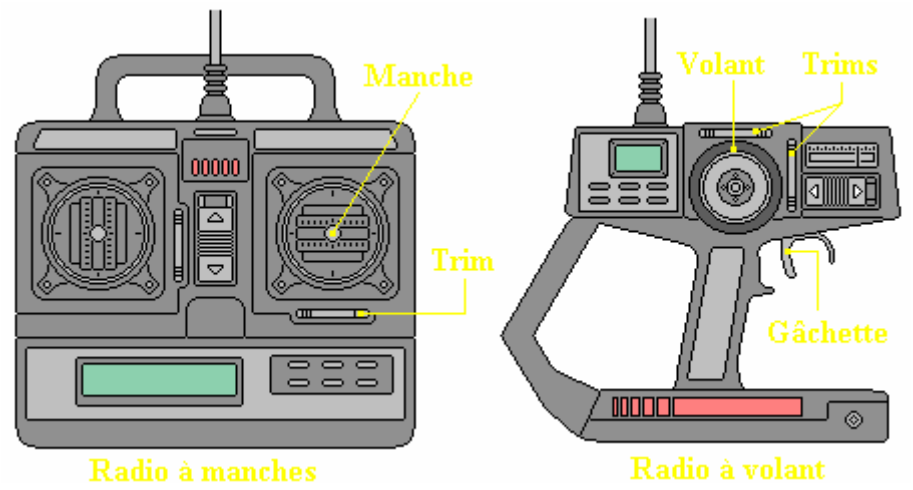
Initialement dérivées de celles développées pour l'aéromodélisme, les radiocommandes de voitures actuelles sont conçues spécifiquement pour cet usage. L'ensemble comprend 3 parties distinctes: le boîtier d'émission, le boîtier de réception, le (ou les) servo(s).

Le boîtier d'émission (souvent appelé émetteur) :

Il existe principalement deux catégories **:** les émetteurs à manches et les émetteurs à volant.

Ce sont normalement des émetteurs à 2 voies : une pour commander la direction, l'autre pour le variateur. Deux systèmes de réglage, baptisés TRIM, permettent d'ajuster la position neutre des deux voies. On trouve aussi souvent des commutateurs pour inverser leur sens, c'est en général les seuls réglages sur les radios d'entrée de gamme.

Il existe des radios avec une multitude d'autres réglages possibles, destinées à la compétition : réglage du débattement de direction, réponse exponentielle du servo de direction, réglage de la puissance de freinage (utile surtout en thermique) et bien d'autres encore... Les radios les plus modernes disposent d'un affichage LCD avec des menus déroulants pour les programmer.



L'émission se fait en modulation d'amplitude (AM) sur les modèles bas de gamme, ou en modulation de fréquence (FM) dans la bande des 26 MHz, 41 MHz ou 72 MHz (les seules qui soient autorisées en voiture RC). Bien sûr, lors d'une course, chaque voiture doit utiliser une fréquence différente des autres (on la modifie par échange des quartz de l'émetteur et du récepteur ou par programmation).

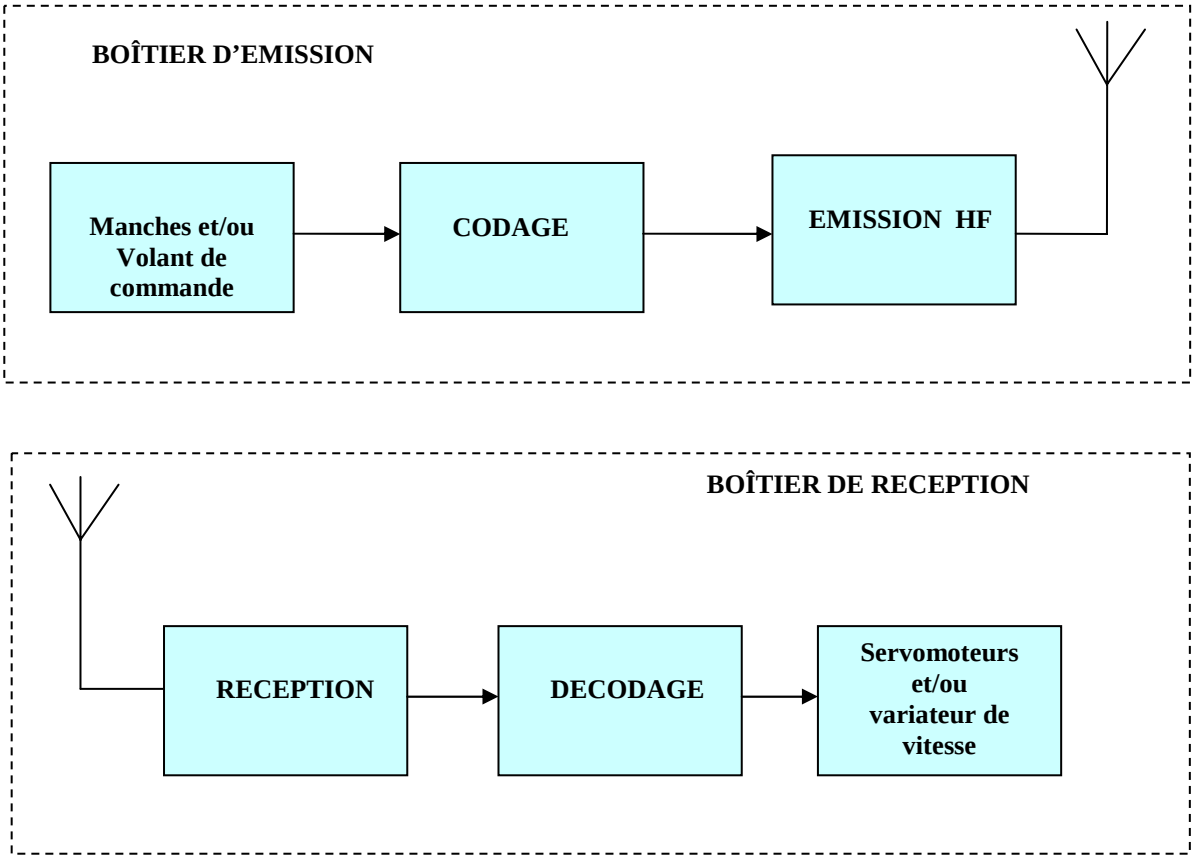
Le boîtier de réception (souvent appelé récepteur):

C'est un simple boîtier installé à bord de la voiture, qui reçoit et interprète les ordres émis par l'émetteur. En électrique, il est généralement alimenté directement par la batterie de propulsion (en thermique, il faut une batterie spécifique pour l'électronique embarquée) .

Remarque : Pourquoi module-t-on un signal ?

La réception d'un signal nécessite des antennes dont les dimensions dépendent de la longueur d'onde du signal (en général de l'ordre de l / 2).
Un signal haute fréquence HF sera facilement transmissible [H.F correspond à des fréquences F > 100 MHz soit des longueurs d'onde L= c / F donc L < $3.10^8 / 10^8$ =3m ; soit une antenne de longueur inférieure à 3m . Par contre , pour les signaux B.F (f de l'ordre de 20 Hz) la longueur d'onde sera beaucoup plus grande et cela nécessiterait des antennes démesurées et le signal serait rapidement atténué. Exemple : Pour f = 10 Hz ,
L = 3.10^4 m soit une antenne de 15 km. Le but de la modulation est de translater le spectre d'un signal B.F [sons, musique , parole] vers les H.F pour pouvoir le transmettre facilement par voie hertzienne. La radio , la télévision , les lignes téléphoniques, la radiocommande de modèle réduit utilisent le procédé de modulation . Le signal H.F est appelé PORTEUSE . Le signal B.F est appelé ***SIGNAL MODULANT*** .

CONSTITUTION D'UN BOÎTIER D'EMISSION ET DE RECEPTION

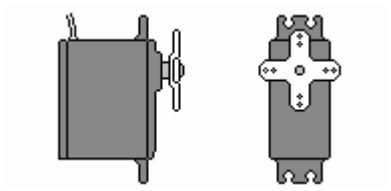


LES ACTIONNEURS

Les servomécanismes :

On les appelle généralement les " servos ". Ce sont les systèmes qui transforment les ordres reçus par le récepteur, en mouvements mécaniques.

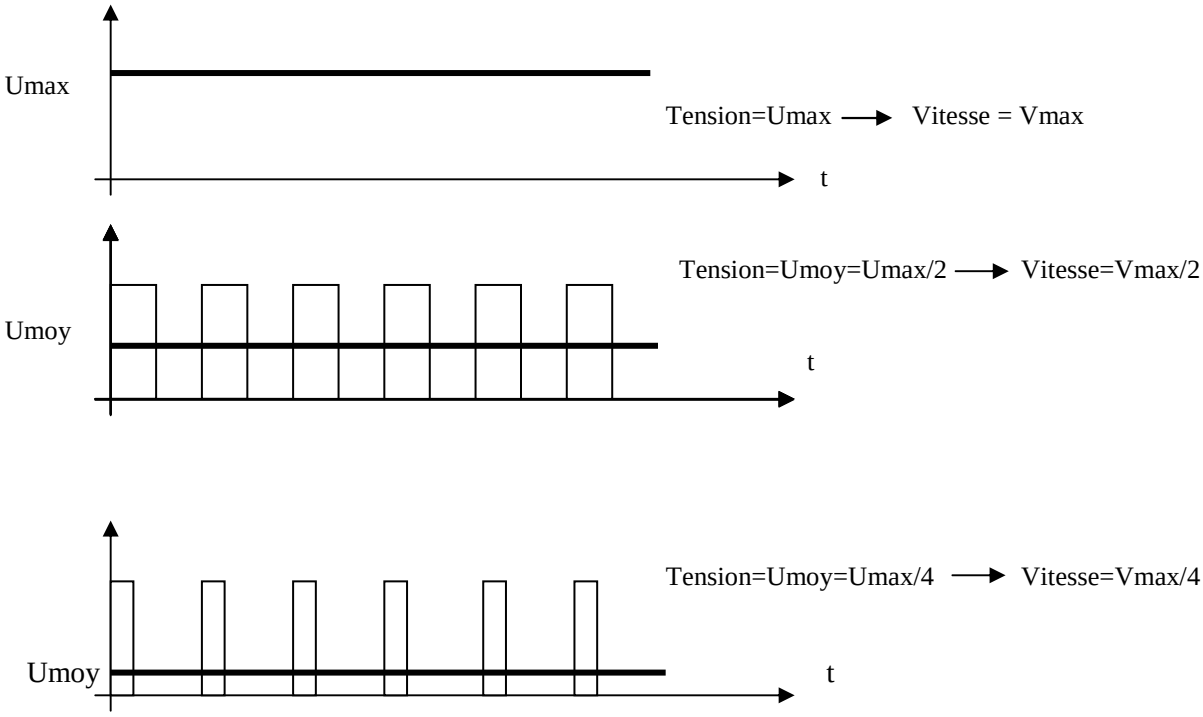
En voiture électrique, on utilise la plupart du temps un seul servo, pour commander la direction (s'il y a un variateur mécanique, il nécessite un second servo pour fonctionner). Un servo est constitué d'un moteur électrique, d'une démultiplication par cascade de pignons, et d'un système d'asservissement.



Le variateur de vitesse :

C'est l'élément qui permet comme son nom l'indique de faire varier la vitesse de rotation du moteur. Autrefois, il s'agissait d'un simple rhéostat manoeuvré par un servomécanisme (ce principe, totalement dépassé aujourd'hui, reste utilisé sur certains modèles bas de gamme). Cette fonction est aujourd'hui prise en charge par un variateur électronique.

C'est une série de transistors (il peut y en avoir jusqu'à 9) qui commandent la vitesse du moteur par variation de la tension moyenne à ses bornes. La technique utilisé est la modulation de largeur d'impulsion
(MLI en français ou PWM en anglais).



COMMANDE D'UN SERVO –MOTEUR

LE SIGNAL de COMMANDE de d'ANGLE DE ROTATION est une impulsion positive pendant un temps variable et court (de 1 à 2 ms) : Cette impulsion doit se ***répéter toutes les 20 ms environ*** (50 fois par seconde).
C'est la durée de 1 à 2 ms qui détermine la position angulaire du servomoteur. Une standardisation des valeurs s'est imposée :

1 ms --> limite basse (gauche par ex.)
1.5 ms --> neutre
2 ms --> limite haute (droite par ex.)

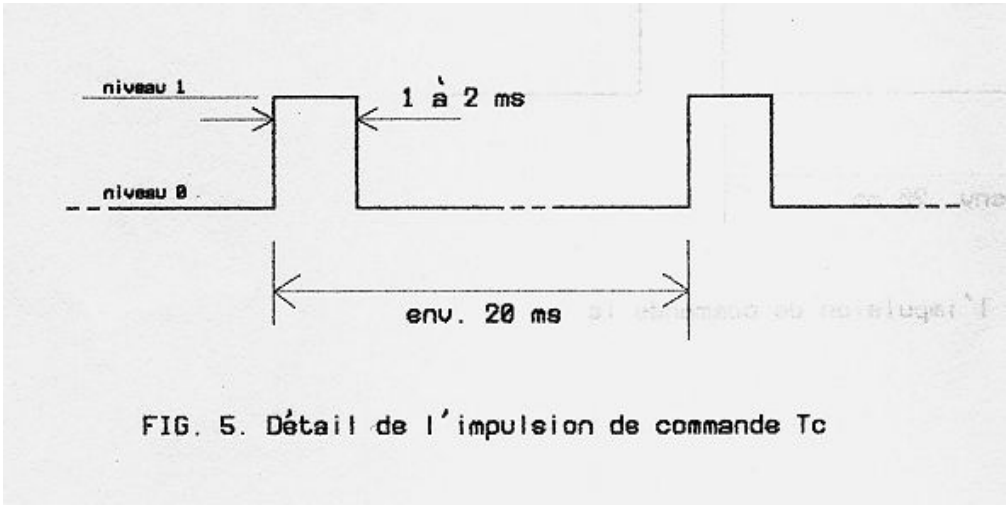
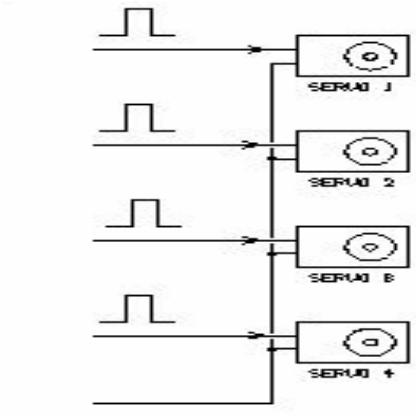


FIG. 5. Détail de l'impulsion de commande Tc

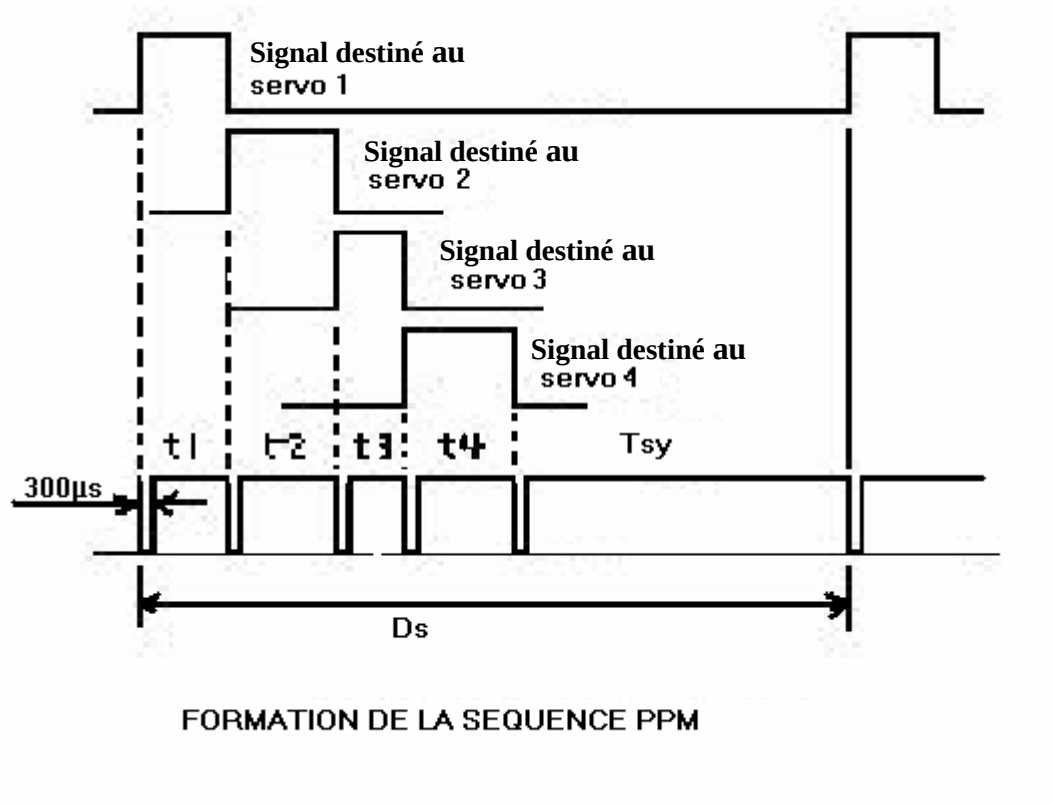
L'impulsion de commande est fabriquée par le codeur du boîtier émission qui par l'intermédiaire de la fonction émission HF la transmet au récepteur HF . Elle est, après décodage, délivrée sur la prise de servo.

Si on désire commander plusieurs servomoteurs, il faut plusieurs émetteurs :



La solution employée pour utiliser un seul émetteur implique une commande SERIE. C'est la PPM (Pulse Position Modulation)

LE CODAGE PPM



FORMATION DE LA SEQUENCE PPM

PPM = Pulse Position Modulation , c'est-à-dire codage par la position relative des impulsions dans le temps.

- **Les impulsions** fines durent 300 µs environ. (c'est le temps de séparation de voie ou inter-voie)

- **Les temps de voies** se mesurent ***d'impulsion à impulsion*** (souvent de front montant à front montant) : t1, t2 ...
- La distance entre deux impulsions de même repère (de "1" à "1" par ex.) est la **durée de séquence Ds**
- Le temps séparant la dernière impulsion d'une séquence de la première de la suivante est le temps de synchronisation **Tsy.**
  On a bien sûr : **Tsy = Ds - (t1 + t2 +t3 + t4 + ..)**
  Ce temps est essentiel car il va permettre au décodeur la reconnaissance sûre de l'impulsion du début de séquence.
  Tsy doit donc être nettement plus grand que la durée maximale d'une voie (2 ms) Il sera souvent de 7 à 8 ms.

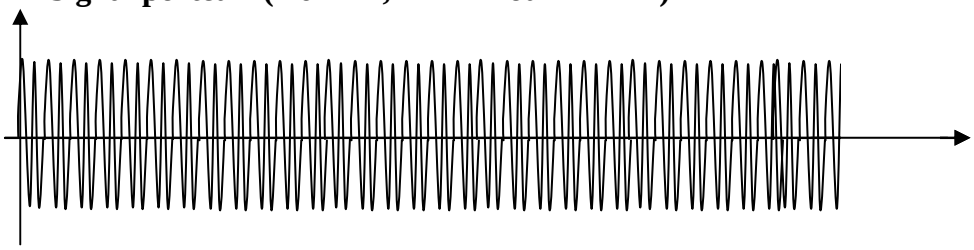
Deux solutions sont envisageables et ont été utilisées :
- **Ds constant** : Par exemple 20 ms. Dans ce cas le temps Tsy varie avec la durée des temps de voies et leur nombre, et peut devenir trop petit.
C'était le cas des codeurs de 1ére génération .

- **Tsy constant :** Par exemple 8 ms. Cette fois le décodeur n'a pas de problème car c'est Ds qui varie en fonction des temps de voies et de leur nombre. (Codeurs de 2ème .... génération) . Cette valeur ne doit pas excéder 30ms (sinon risque d'instabilité des servos).

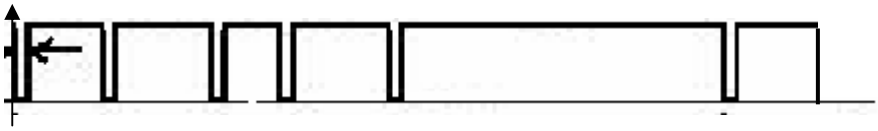
ENVOI DE LA TRAME VERS LE BOÎTIER DE RECEPTION

Exemple : Cas de la Modulation d'Amplitude

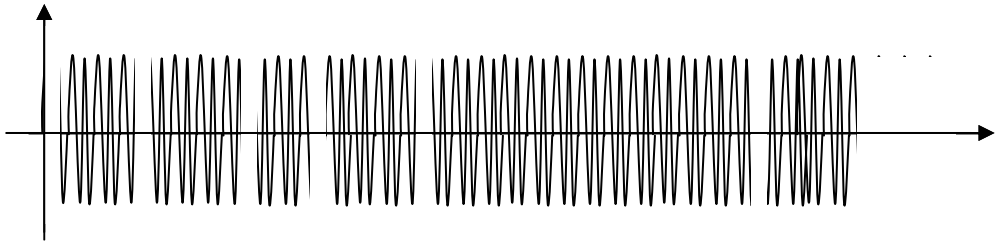
Signal porteur (26MHz, 41MHz ou 72MHz)



Signal modulant (signal à transmettre)

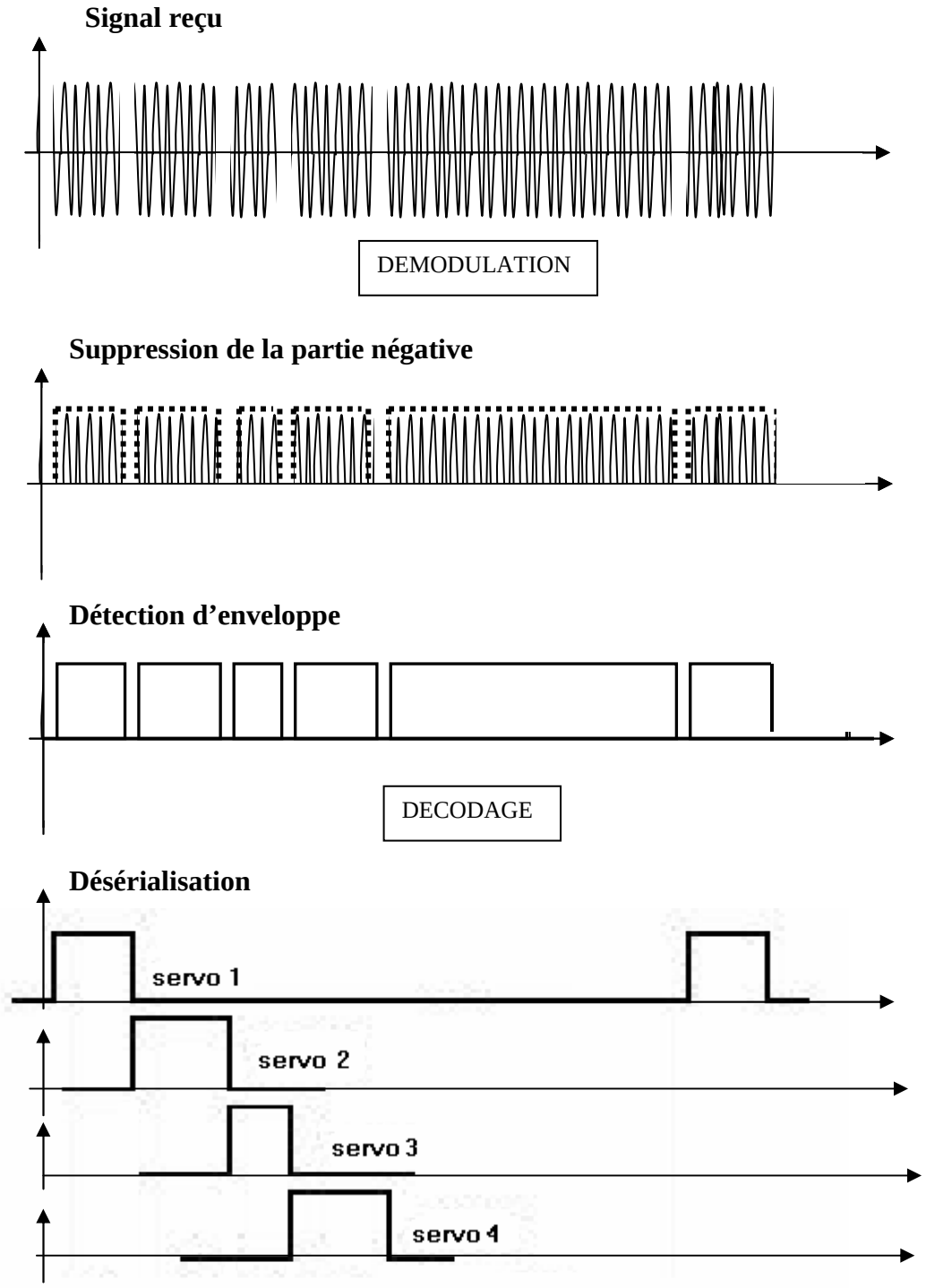


Signal émis



RECEPTION ET DECODAGE DE LA TRAME

Exemple : Cas de la Modulation d'Amplitude



Remarque : En FM, les durées de voie sont émises à une fréquence f_1 (41 ou 72MHz) et les impulsions inter-voie à une fréquence f_2 voisine. Ce système à l'avantage d'être insensible aux parasites mais la démodulation est plus délicate.

LES FRÉQUENCES AUTORISÉES (Document FFAM)

Des fréquences ont été attribuées par l'Autorité de Régulation de Télécommunications pour la pratique du modélisme.

Ces fréquences autorisées sont réparties pour tous types de modèles réduits

- dans la bande des fréquences 26MHz:

Les fréquences .

26815	26825	26835	26845	26855	26865
26875	26885	26895	26905	26915	--

- dans la bande des fréquences 41MHz:

Les fréquences.

41110	41120	41130	41140	41150	41160
41170	41180	41190	41200	--	--

- dans la bande des fréquences 72MHz:

Les fréquences.

72210	72230	72250	72270	72290	72310
72330	72350	72370	72390	72410	72430
72450	72470	72490	--	--	--

- Cependant, dans la bande de fréquence 41000 à 41100 kHz:
Les fréquences suivantes:

41000	41010	41020	41030	41040	41050
41060	41070	41080	41090	41100	--

sont spécifiquement réservées à *l'aéromodélisme.*

Pour plus de précisions, les textes des arrêtés (références 17611 du 21 novembre 1998 et 583 du lundi 11 et mardi 12 janvier 1999) sont consultables en tapant http://www.legifrance.gouv.fr

Boucle De Réaction à Verrouillage De Phase

Introduction

La fonction d'un circuit à boucle de réaction à verrouillage de phase (PHASE-LOCKED LOOP «PLL») est de comparer, en fréquence et en phase, la sortie d'un oscillateur, à fréquence accordée par la tension (VCO), à celle d'un oscillateur de référence, à fréquence fixe. C'est une «servo-boucle électronique» qui permet la filtration et l'accord par sélection de fréquence sans le recours de bobines ou d'inductances, une caractéristique importante dans les circuits électroniques miniatures d'aujourd'hui.

Parmi les applications de la boucle de réaction à verrouillage de phase, on retrouve le décodage de tonalité, la démodulation des signaux MA et MF, la multiplication de fréquence, la synchronisation d'impulsions et la régénération de signaux.

Principes De Base

Fr = Fréquence de référence
Fo = Fréquence de sortie
Se= Signal d'erreur

FIGURE 1 : *Diagramme synoptique d'une boucle de réaction à verrouillage de phase*

existe différents types de circuit à boucle de réaction à verrouillage de phase (PLL). Cependant, tous fonctionnent selon les mêmes principes de base (FIG.1).

Le comparateur de phase (FIG.2) reçoit et compare la phase et la fréquence, du circuit de sortie, avec une fréquence de référence externe d'entrée, et génère une tension d'erreur variable correspondante, à sa sortie.

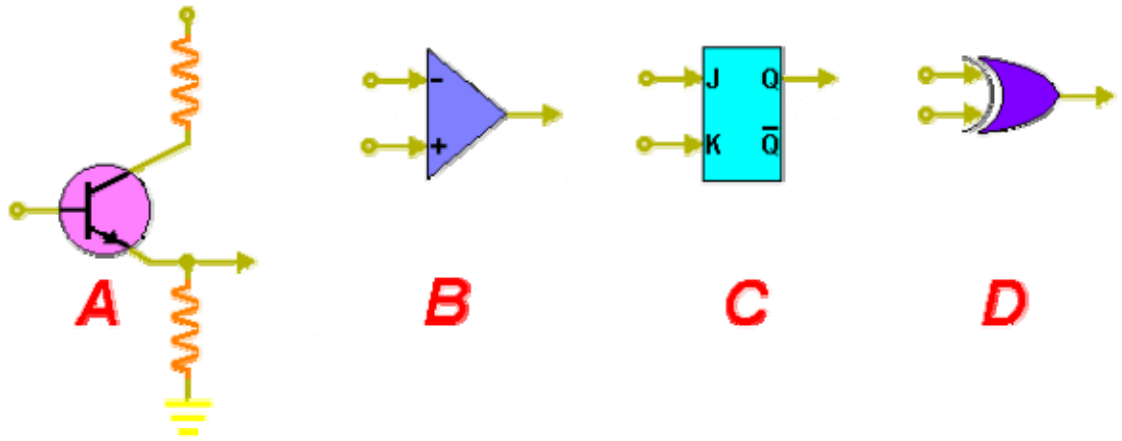


FIGURE 2 : *Comparateurs de phase les plus utilisés.* ***(A et B)*** *Circuits analogiques.* ***(C et D)*** *Circuits numériques.*

Ensuite, la tension d'erreur est filtrée par un filtre passe-bas (FIG.3) et envoyée à l'entrée de contrôle du VCO (oscillateur accordé par la tension)(FIG.4). Il en résulte, que chaque différence de phase ou de fréquence, entre Fo et Fr, est progressivement réduite à zéro. Quand ce phénomène se produit, on dit que la boucle est "verrouillée".

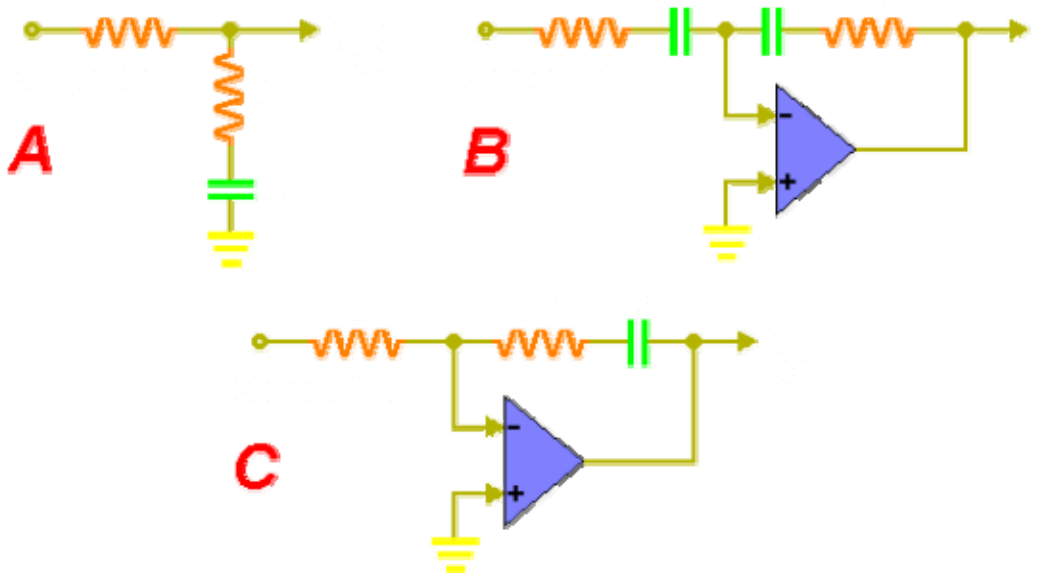


FIGURE 3 : *Filtres passe-bas utilisés dans les circuits analogiques.* ***(A)*** *FIltre passif.* ***(B)*** *Filtre actif.* ***(C)*** *Filtre actif en PI.*

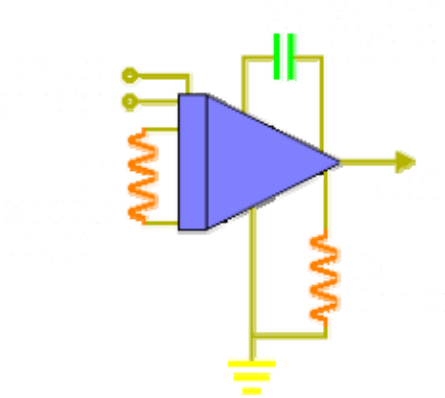


FIGURE 4 : *Diagramme simplifié d'un VCO.*

Si la fréquence du VCO est initialement plus basse que la référence d'entrée, la sortie du comparateur de phase sera une tension positive. Cette tension, filtrée, commande alors au VCO d'augmenter sa fréquence jusqu'à ce que cette dernière et sa phase épousent parfaitement celles de la référence d'entrée.

À l'inverse, la tension de sortie du comparateur décroît et commande une diminution de fréquence de la part du VCO.

Le filtre passe-bas (FIG.3) est la partie essentielle, du circuit à boucle de réaction à verrouillage de phase, qui convertit la sortie du comparateur de phase en tension CC pour le contrôle du VCO. Parce qu'on y retrouve une constante de temps, le verrouillage n'est pas instantané et la fréquence de sortie verrouille à la valeur moyenne de la fréquence de référence. Cette caractéristique permet d'obtenir une fréquence de sortie propre, à partir de fréquences d'entrée de référence contenant du bruit. Le filtre passe-bas crée un déphasage entre Fo et Fr. Ce déphasage constitue la tension qui stabilise la fréquence du VCO.

Multiplication De Fréquence

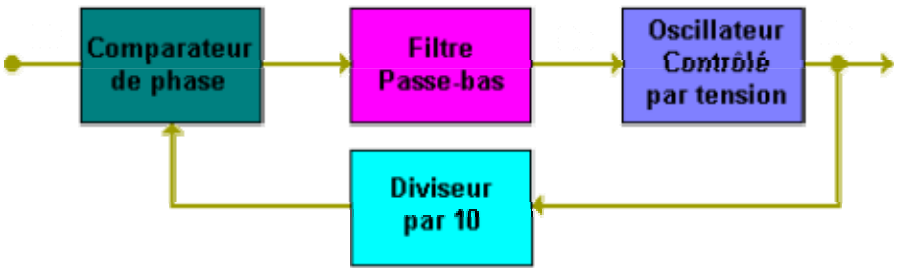


FIGURE 5 : *Multiplicateur de fréquence basé sur une boucle de réaction à verrouillage de phase.*

Dans le circuit de base de la figure 1, la fréquence du signal de sortie verrouille avec la valeur moyenne de la fréquence d'entrée, ainsi, les fréquences d'entrée et de sortie sont identiques. La figure 5 présente une variation de ce circuit dans laquelle la fréquence de sortie est précisément dix fois plus élevée que celle d'entrée. Il en résulte que le circuit fonctionne comme un multiplicateur de fréquence.

Dans le diagramme synoptique de la figure 5, un compteur diviseur par dix est inséré dans la boucle de réaction entre la sortie du VCO et l'entrée du comparateur de phase. Par conséquent, le comparateur de phase verrouille à la fréquence de sortie du diviseur par dix au lieu de la sortie du VCO.

Toutefois, dans la condition de verrouillage, la fréquence de sortie (Fo) du VCO est dix fois plus grande que le signal d'entrée de référence (Fr). Le circuit agit donc comme un multiplicateur X10. Ce circuit peut multiplier par n'importe quel nombre autre que dix, à la condition d'avoir un compteur possédant un ratio de division approprié dans sa boucle de réaction.

Synthèse De Fréquence

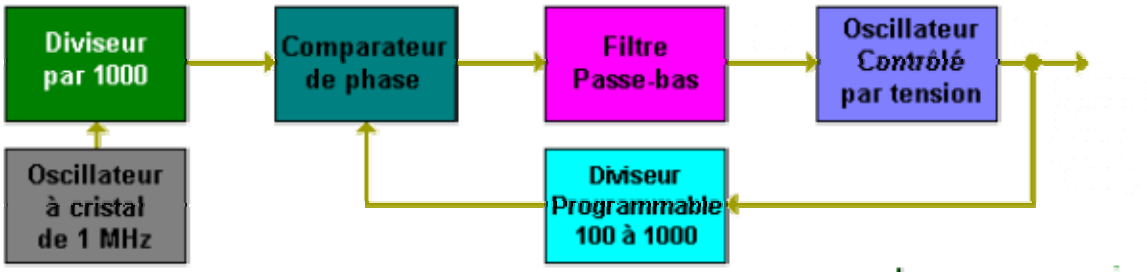


FIGURE 6 : *Synthétiseur de fréquence basé sur une boucle de réaction à verrouillage de phase.*

Le circuit de boucle de réaction à verrouillage de phase peut aussi fonctionner en tant que synthétiseur de fréquence programmable (fig.6) et ce, avec une grande précision. La fréquence de référence d'entrée du comparateur de phase est un signal fixe et précis de 1 kHz dérivé d'un oscillateur à cristal de 1 MHz à travers un compteur diviseur par 1000.

Comme dans le circuit multiplicateur de fréquence, il y a un compteur dans la boucle de réaction entre la sortie du VCO et l'entrée du comparateur de phase. Cependant, ce circuit est programmable extérieurement. Ainsi, il peut exécuter n'importe quelle division de nombre entier avec un ratio entre 100X et 1000X.

Cette caractéristique permet au circuit de générer ou de synthétiser des fréquences exactes et stables, comprises entre 100 kHz et 1 MHz par bonds de 1 kHz. Le circuit du VCO de la figure 6 doit avoir une gamme de fréquence étendue, de 10 à 1, pour couvrir la gamme requise. De plus, la valeur, du bond en fréquence, correspond à la fréquence externe de 1 kHz.

Synthèse De Haute Fréquence

Le compteur programmable est une fonction essentielle de tous les synthétiseurs de fréquence. Pratiquement tous les compteurs répondent à une fréquence d'entrée d'un maximum de quelques mégahertz à peine. Comme résultat, le circuit de la figure 6 ne peut pas synthétiser

directement de fréquences plus élevées que quelques mégahertz. Les figures 7 à 9 présentent trois versions alternatives de circuits synthétiseurs de haute fréquence, basés sur la boucle de réaction à verrouillage de phase.

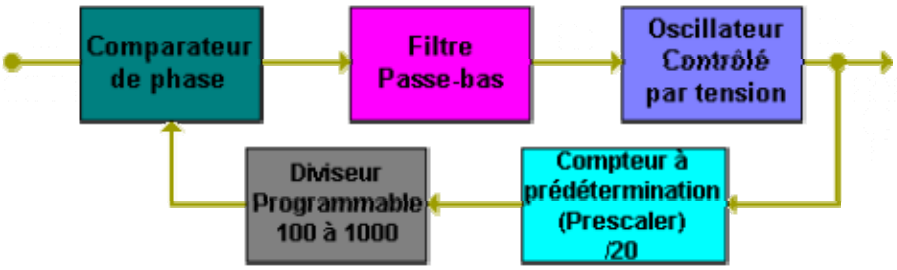


FIGURE 7 : *Synthétiseur de fréquence avec compteur à prédétermination (prescaler), basé sur une boucle de réaction à verrouillage de phase.*

Le circuit de la figure 7 utilise la technique de la prédétermination (prescaling). Un étage additionnel de compteur haute fréquence, diviseur par X, de valeur fixe, (compteur à prédétermination (prescaler)) est placé entre la sortie du VCO et l'entrée du compteur programmable.

Cette configuration permet au VCO d'opérer à une fréquence X fois supérieure à celle de l'étage du compteur programmable. Dans l'exemple montrée, la prédétermination est une division par 20, donnant au synthétiseur la possibilité de couvrir une gamme variant de 2 à 20 MHz en 900 pas. Le désavantage, c'est que la valeur du bond du synthétiseur est augmentée par un ratio égal à la valeur de la prédétermination (c.à.d. 20X Fr dans ce circuit).

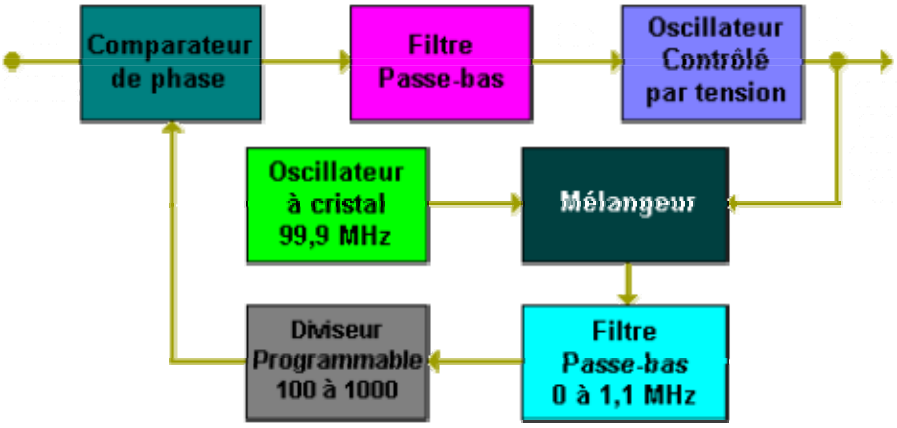


FIGURE 8 : *Synthétiseur de haute fréquence, de type mélangeur, basé sur une boucle de réaction à verrouillage de phase.*

Dans le circuit de la figure 8, l'emploi du mélangeur synthétise les fréquences entre 100 et 101 MHz en 1000 bonds de 1 kHz. La sortie du VCO est mélangée à une fréquence de 99.9 MHz, dérivée de l'oscillateur à cristal, avant d'être passée à travers le filtre passe-bas, pour produire une fréquence de différence de 100 kHz à 1.1 MHz. Cette fréquence de différence pénètre alors dans le PLL et passe à travers l'étage du compteur programmable.

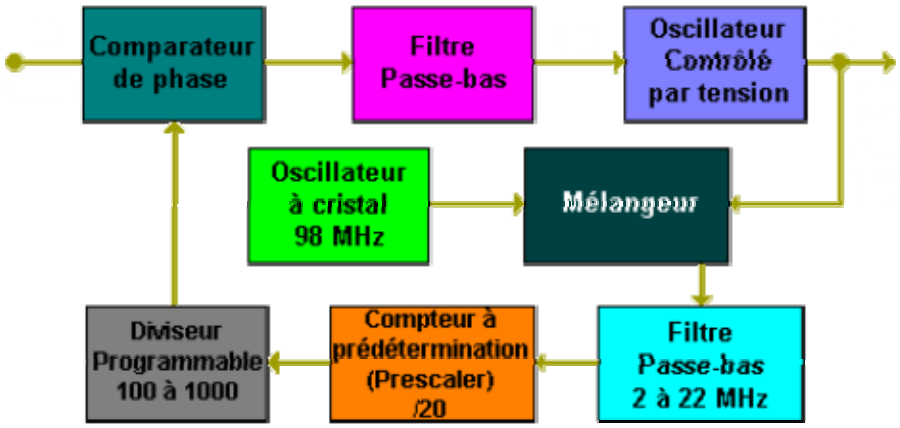


FIGURE 9 : *Synthétiseur de fréquence, à large gamme, basé sur une boucle de réaction à verrouillage de phase.*

La figure 9, montre comment les circuits du mélangeur et du compteur à prédétermination de la figure 8 peuvent être combinés pour produire un synthétiseur de haute fréquence, à large gamme, pouvant générer des fréquences comprises entre 100 et 120 MHz en 1000 bonds de 20 Hz. Le signal de sortie du VCO est mélangée à la fréquence de 98 MHz , dérivée de l'oscillateur à cristal, et passée à travers le filtre passe-bas afin de produire une sortie de 2 à 22 MHz.

Cette sortie est alors réduite une gamme de 100 kHz à 1.1 MHz par l'étage de prédétermination du diviseur par 20, avant d'être retournée au PLL via le compteur programmable. Ce circuit donne d'excellents résultats.

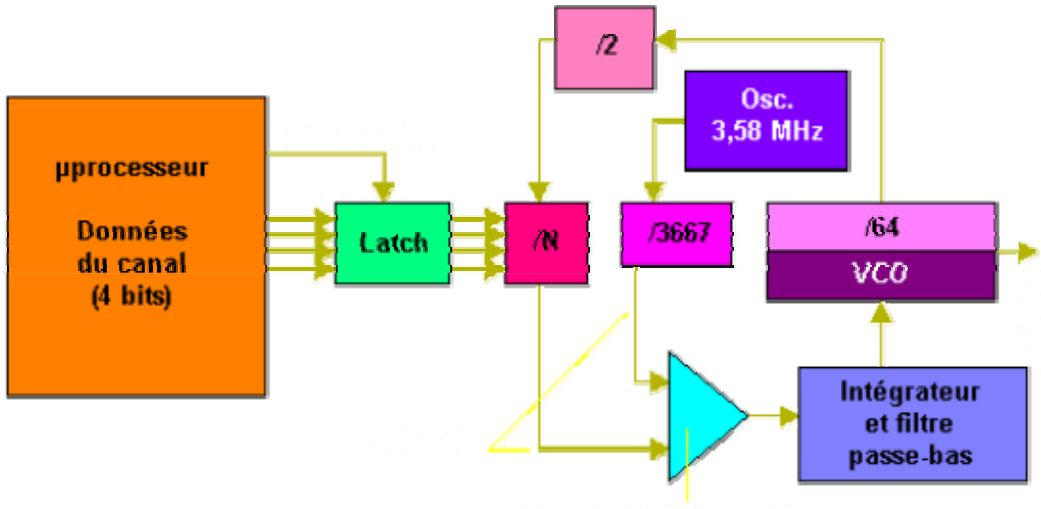


FIGURE 10 : *Version numérique d'une boucle de réaction à verrouillage de phase.*

figure 10 représente une version numérique, simplifiée, du circuit à boucle de réaction à verrouillage de phase, que l'on retrouve dans les téléviseurs. Ce système est généralement appelé « PLL ÉTENDU » et garde la fréquence de l'oscillateur du syntoniseur à une sous-harmonique de l'oscillateur de référence (3.58 MHz dans ce cas). Ici, l'élément de division, qui est habituellement fixe, est remplacé par un diviseur variable programmable (÷N). Le changement de canal s'effectue en variant le ratio de division, du diviseur programmable, avec la commande de 4 bits de donnée du système de contrôle du micro-processeur (qui, à son tour, est actionné par les touches du panneau avant de l'appareil ou par la télécommande).

National Semiconductor

March 1988

CD4015BM/CD4015BC Dual 4-Bit Static Shift Register

General Description

The CD4015BM/CD4015BC contains two identical, 4-stage, serial-input/parallel-output registers with independent "Data", "Clock," and "Reset" inputs. The logic level present at the input of each stage is transferred to the output of that stage at each positive-going clock transition. A logic high on the "Reset" input resets all four stages covered by that input. All inputs are protected from static discharge by a series resistor and diode clamps to V_{DD} and V_{SS}.

Features

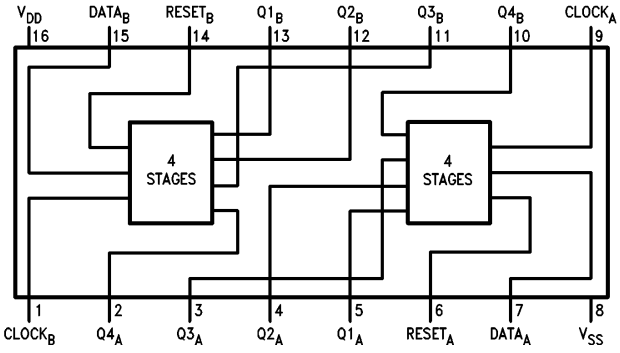
■ Wide supply voltage range	3.0V to 18V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	Fan out of 2 driving 74L or 1 driving 74LS
■ Medium speed operation	8 MHz (typ.) clock rate
■ Fully static design	@$V_{DD} - V_{SS} = 10V$

Applications

- Serial-input/parallel-output data queueing
- Serial to parallel data conversion
- General purpose register

Connection Diagram and Truth Table

Dual-In-Line Package



TL/F/5948–1

CL▲	D	R	Q_1	Q_n	
⌐	0	0	0	Q_{n-1}	
⌐	1	0	1	Q_{n-1}	
¬	X	0	Q_1	Q_n	(No change)
X	X	1	0	0	

▲ Level change

X = Don't care case

Order Number CD4015B

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	-0.5 to $+18$ V_{DC}
Input Voltage (V_{IN})	-0.5 to V_{DD} $+0.5$ V_{DC}
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

DC Supply Voltage (V_{DD})	$+3$ to $+15$ V_{DC}
Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD4015BM	$-55°C$ to $+125°C$
CD4015BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4015BM (Note 2)

Symbol	Parameter	Conditions	$-55°C$		$+25°C$			$+125°C$		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$, $V_{IN} = V_{DD}$ or V_{SS}		5		0.005	5		150	μA
		$V_{DD} = 10V$, $V_{IN} = V_{DD}$ or V_{SS}		10		0.010	10		300	μA
		$V_{DD} = 15V$, $V_{IN} = V_{DD}$ or V_{SS}		20		0.015	20		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$ } $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$ } $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$ } $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$ } $\lvert I_O \rvert < 1\ \mu A$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$ } $\lvert I_O \rvert < 1\ \mu A$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$ } $\lvert I_O \rvert < 1\ \mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$		3.0		4.50	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$	7.0		7.0	5.50		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 4.6V$	-0.64		-0.51	-0.88		-0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	-1.6		-1.3	-2.25		-0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	-4.2		-3.4	-8.8		-2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		-0.1		-10^{-5}	-0.1		-1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

DC Electrical Characteristics CD4015BC (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20		0.005	20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40		0.010	40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80		0.015	80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

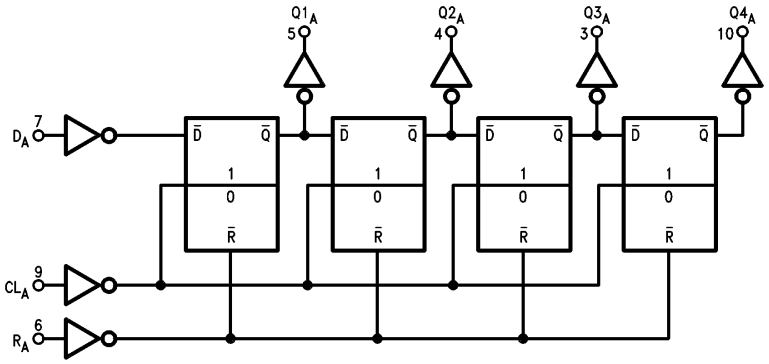
AC Electrical Characteristics*

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, $t_r = t_f = 20$ ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CLOCK OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		230	350	ns
		$V_{DD} = 10V$		80	160	ns
		$V_{DD} = 15V$		60	120	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WL}, t_{WM}	Minimum Clock Pulse-Width	$V_{DD} = 5V$		160	250	ns
		$V_{DD} = 10V$		60	110	ns
		$V_{DD} = 15V$		50	85	ns
t_{rCL}, t_{fCL}	Clock Rise and Fall Time	$V_{DD} = 5V$			15	μs
		$V_{DD} = 10V$			15	μs
		$V_{DD} = 15V$			15	μs
t_{SU}	Minimum Data Set-Up Time	$V_{DD} = 5V$		50	100	μs
		$V_{DD} = 10V$		20	40	μs
		$V_{DD} = 15V$		15	30	μs
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	2	3.5		MHz
		$V_{DD} = 10V$	4.5	8		MHz
		$V_{DD} = 15V$	6	11		MHz
C_{IN}	Input Capacitance	Clock Input		7.5	10	pF
		Other Inputs		5	7.5	pF
RESET OPERATION						
$t_{PHL(R)}$	Propagation Delay Time	$V_{DD} = 5V$		200	400	ns
		$V_{DD} = 10V$		100	200	ns
		$V_{DD} = 15V$		80	160	ns
$t_{WH(R)}$	Minimum Reset Pulse Width	$V_{DD} = 5V$		135	250	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		30	60	ns

*AC Parameters are guaranteed by DC correlated testing.

Logic Diagrams



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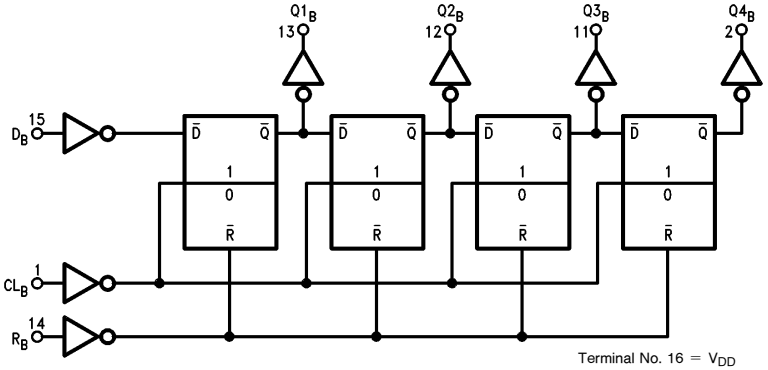
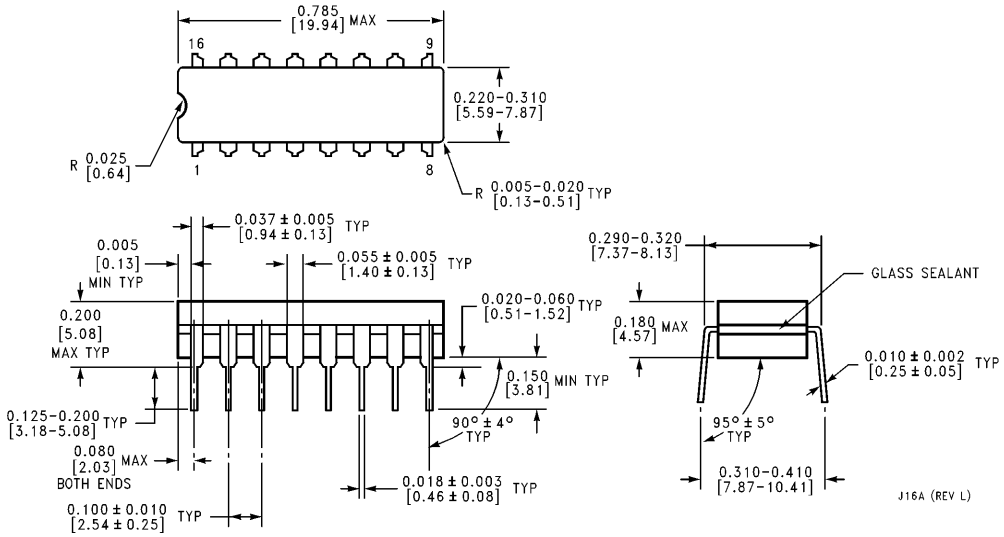
Logic Diagrams (Continued)



Terminal No. 16 = V_{DD}
Terminal No. 8 = GND

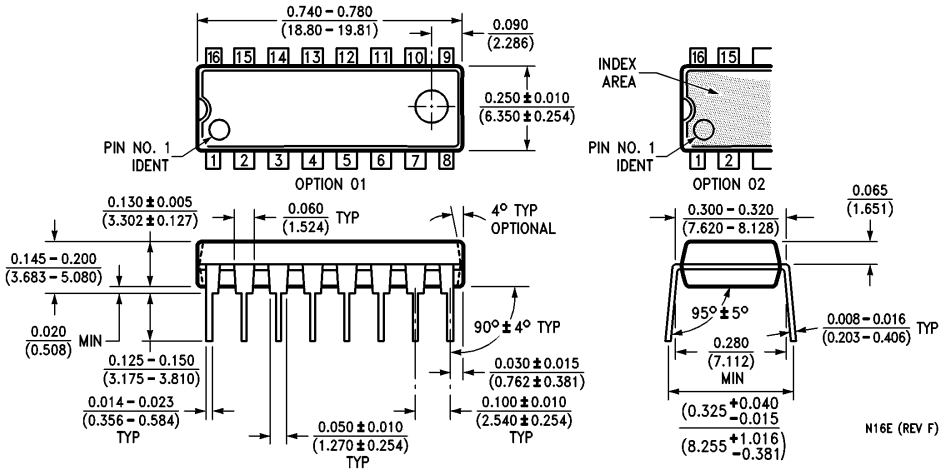
TL/F/5948–3

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number CD4015BMJ or CD4015BCJ
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number CD4015BMN or CD4015BCN
NS Package Number N16E

LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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National Semiconductor

March 1988

CD4017BM/CD4017BC Decade Counter/Divider with 10 Decoded Outputs CD4022BM/CD4022BC Divide-by-8 Counter/Divider with 8 Decoded Outputs

CD4017BM/CD4017BC Decade Counter/Divider with 10 Decoded Outputs
CD4022BM/CD4022BC Divide-by-8 Counter/Divider with 8 Decoded Outputs

General Description

The CD4017BM/CD4017BC is a 5-stage divide-by-10 Johnson counter with 10 decoded outputs and a carry out bit.

The CD4022BM/CD4022BC is a 4-stage divide-by-8 Johnson counter with 8 decoded outputs and a carry-out bit.

These counters are cleared to their zero count by a logical "1" on their reset line. These counters are advanced on the positive edge of the clock signal when the clock enable signal is in the logical "0" state.

The configuration of the CD4017BM/CD4017BC and CD4022BM/CD4022BC permits medium speed operation and assures a hazard free counting sequence. The 10/8 decoded outputs are normally in the logical "0" state and go to the logical "1" state only at their respective time slot. Each decoded output remains high for 1 full clock cycle. The carry-out signal completes a full cycle for every 10/8 clock input cycles and is used as a ripple carry signal to any succeeding stages.

Features

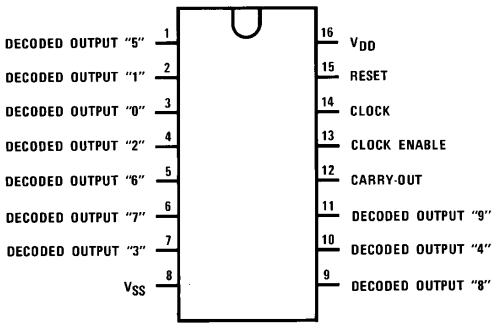
■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	Fan out of 2 driving 74L or 1 driving 74LS
■ Medium speed operation	5.0 MHz (typ.) with 10V V_{DD}
■ Low power	10 μW (typ.)
■ Fully static operation	

Applications

- Automotive
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering

Connection Diagrams

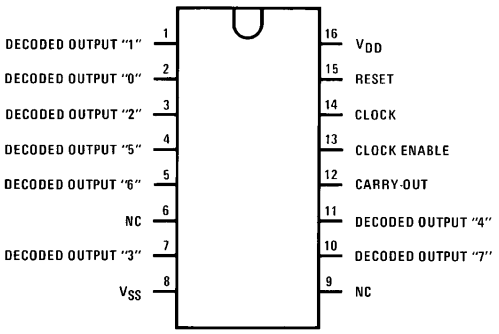
CD4017B
Dual-In-Line Package



TL/F/5950–1

Top View

CD4022B
Dual-In-Line Package



TL/F/5950–2

Top View

Order Number CD4017B or CD4022B

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
Input Voltage (V_{IN})	$-0.5\ V_{DC}$ to $V_{DD} + 0.5\ V_{DC}$
Storage Temperature (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	$+3\ V_{DC}$ to $+15\ V_{DC}$
Input Voltage (V_{IN})	0 to $V_{DD}\ V_{DC}$
Operating Temperature Range (T_A)	
CD4017BM, CD4022BM	$-55°C$ to $+125°C$
CD4017BC, CD4022BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4017BM, CD4022BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$, $V_{IN} = V_{DD}$ or V_{SS}		5		0.3	5		150	μA
		$V_{DD} = 10V$, $V_{IN} = V_{DD}$ or V_{SS}		10		0.5	10		300	μA
		$V_{DD} = 15V$, $V_{IN} = V_{DD}$ or V_{SS}		20		1.0	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5			1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$		3.0			3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$	7.0		7.0			7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 4.6V$	−0.25		−0.2	−0.36		−0.14		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−0.62		−0.5	−0.9		−0.35		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−1.8		−1.5	−3.5		−1.1		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4017BC, CD4022BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		20		0.5	20		150	μA
		$V_{DD} = 10V$		40		1.0	40		300	μA
		$V_{DD} = 15V$		80		5.0	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

DC Electrical Characteristics CD4017BC, CD4022BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		+25°			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1.0\ \mu A$ $V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$ $V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$ $V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		 1.5 3.0 4.0			 1.5 3.0 4.0		 1.5 3.0 4.0	 V V V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1.0\ \mu A$ $V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$ $V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$ $V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	 3.5 7.0 11.0		 3.5 7.0 11.0			 3.5 7.0 11.0		 V V V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 0.4V$ $V_{DD} = 10V$, $V_O = 0.5V$ $V_{DD} = 15V$, $V_O = 1.5V$	0.52 1.3 3.6		0.44 1.1 3.0	0.88 2.25 8.8		0.36 0.9 2.4		mA mA mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 4.6V$ $V_{DD} = 10V$, $V_O = 9.5V$ $V_{DD} = 15V$, $V_O = 13.5V$	−0.2 −0.5 −1.4		−0.16 −0.4 −1.2	−0.36 −0.9 −3.5		−0.12 −0.3 −1.0		mA mA mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$ $V_{DD} = 15V$, $V_{IN} = 15V$		−0.3 0.3		-10^{-5} 10^{-5}	−0.3 0.3		−1.0 1.0	μA μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides condtions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

AC Electrical Characteristics*

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, t_{rCL} and $t_{fCL} = 20$ ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CLOCK OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time Carry Out Line	 $V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		 415 160 130	 800 320 250	 ns ns ns
	Carry Out Line	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$ } $C_L = 15$ pF		240 85 70	480 170 140	ns ns ns
	Decode Out Lines	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		500 200 160	1000 400 320	ns ns ns
t_{TLH}, t_{THL}	Transition Time Carry Out and Decode Out Lines t_{TLH}	 $V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		 200 100 80	 360 180 130	 ns ns ns
	t_{THL}	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		100 50 40	200 100 80	ns ns ns
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$ } Measured with Respect to Carry Output Line	1.0 2.5 3.0	2 5 6		MHz MHz MHz
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		125 45 35	250 90 70	ns ns ns
t_{rCL}, t_{fCL}	Clock Rise and Fall Time	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$			20 15 5	μs μs μs
t_{SU}	Minimum Clock Inhibit Data Setup Time	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		120 40 32	240 80 65	ns ns ns
C_{IN}	Average Input Capacitance			5	7.5	pF

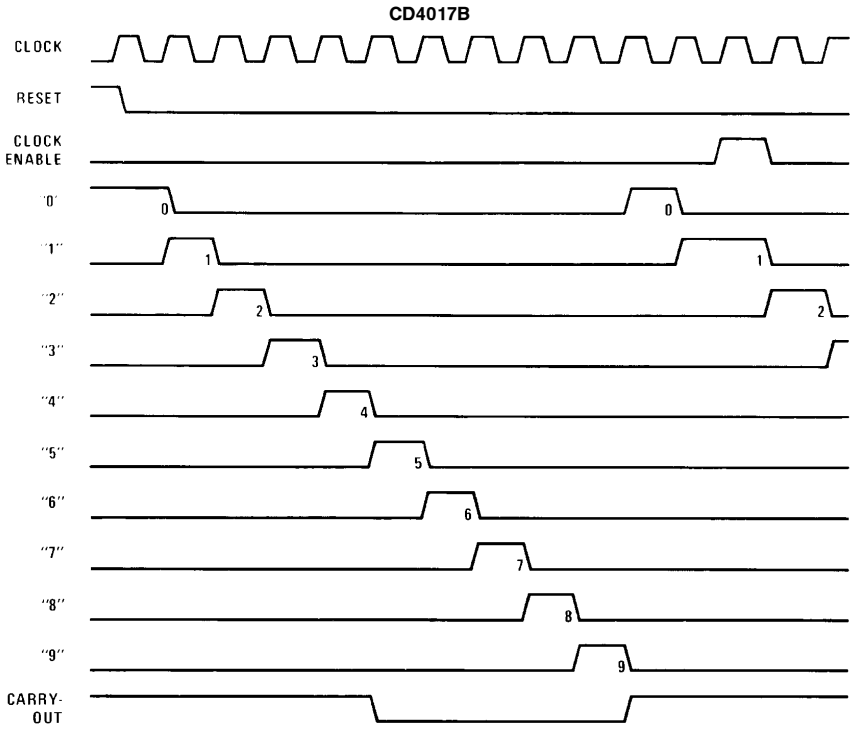
AC Electrical Characteristics*

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, t_{rCL} and $t_{fCL} = 20$ ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RESET OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time Carry Out Line	$V_{DD} = 5V$		415	800	ns
		$V_{DD} = 10V$		160	320	ns
		$V_{DD} = 15V$		130	250	ns
	Carry Out Line	$V_{DD} = 5V$ } $C_L = 15$ pF		240	480	ns
		$V_{DD} = 10V$ } $C_L = 15$ pF		85	170	ns
		$V_{DD} = 15V$ } $C_L = 15$ pF		70	140	ns
	Decode Out Lines	$V_{DD} = 5V$		500	1000	ns
		$V_{DD} = 10V$		200	400	ns
		$V_{DD} = 15V$		160	320	ns
t_W	Minimum Reset Pulse Width	$V_{DD} = 5V$		200	400	ns
		$V_{DD} = 10V$		70	140	ns
		$V_{DD} = 15V$		55	110	ns
t_{REM}	Minimum Reset Removal Time	$V_{DD} = 5V$		75	150	ns
		$V_{DD} = 10V$		30	60	ns
		$V_{DD} = 15V$		25	50	ns

*AC Parameters are guaranteed by DC correlated testing.

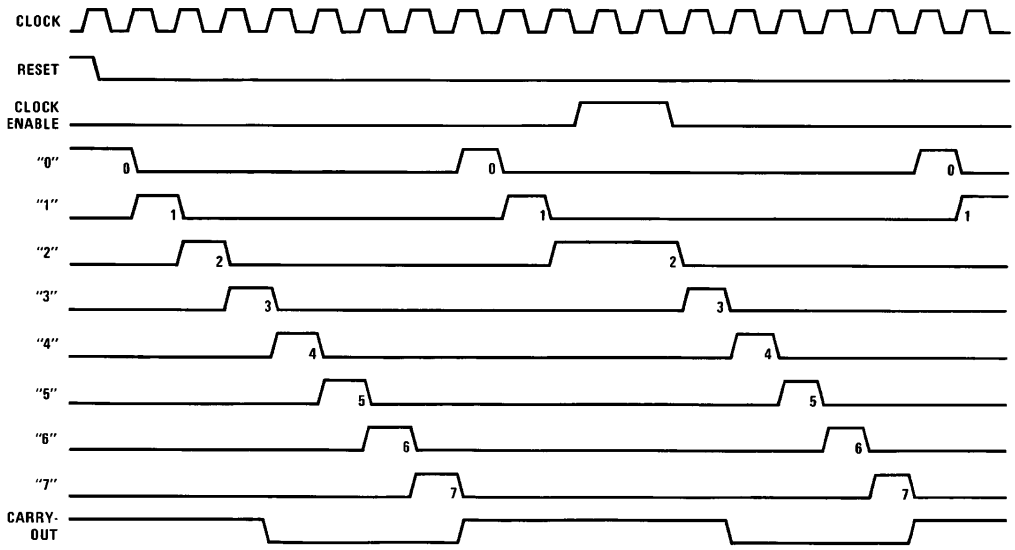
Timing Diagrams



TL/F/5950–3

Timing Diagrams (Continued)

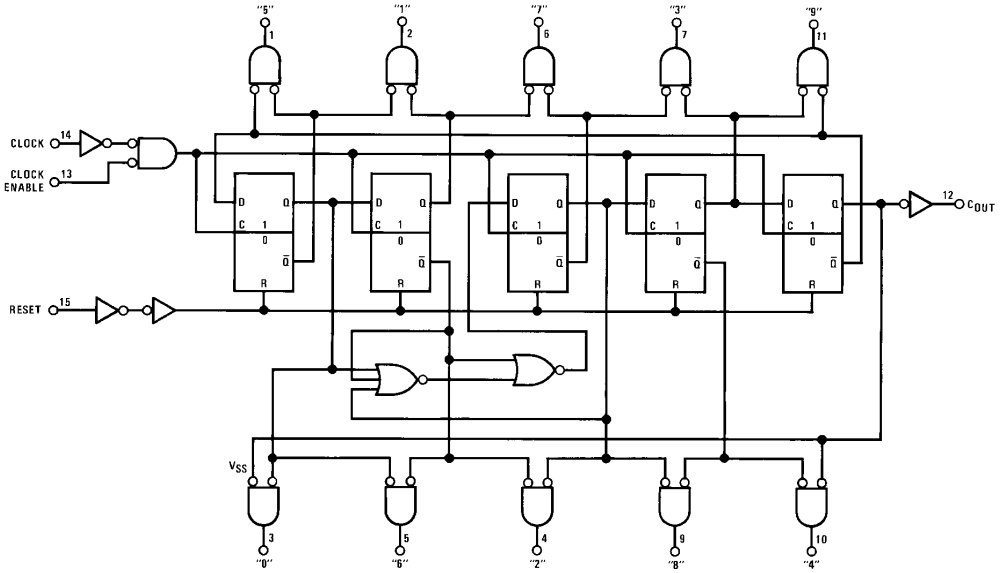
CD4022B



TL/F/5950–4

Logic Diagrams

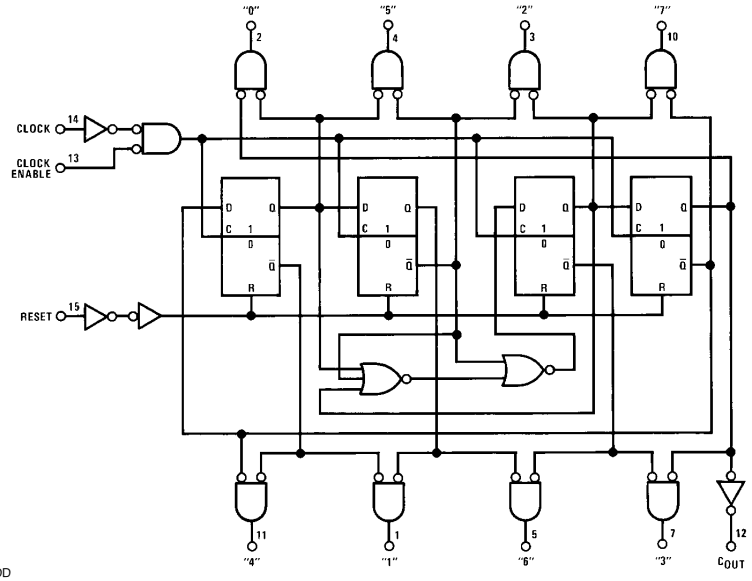
CD4017B



Terminal No. 8 = GND
Terminal No. 16 = V_{DD}

TL/F/5950–5

CD4022B



Terminal No. 16 = V_{DD}
Terminal No. 8 = GND

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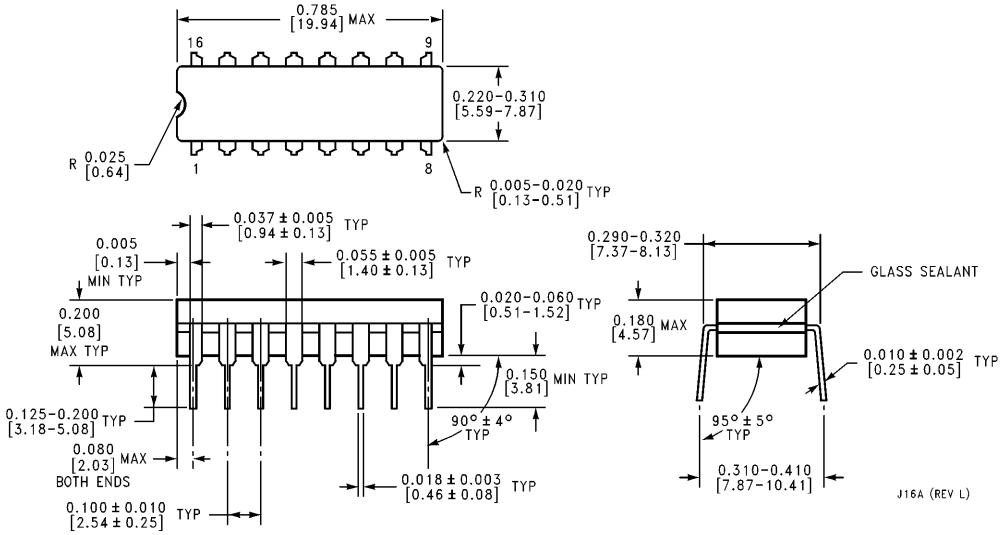
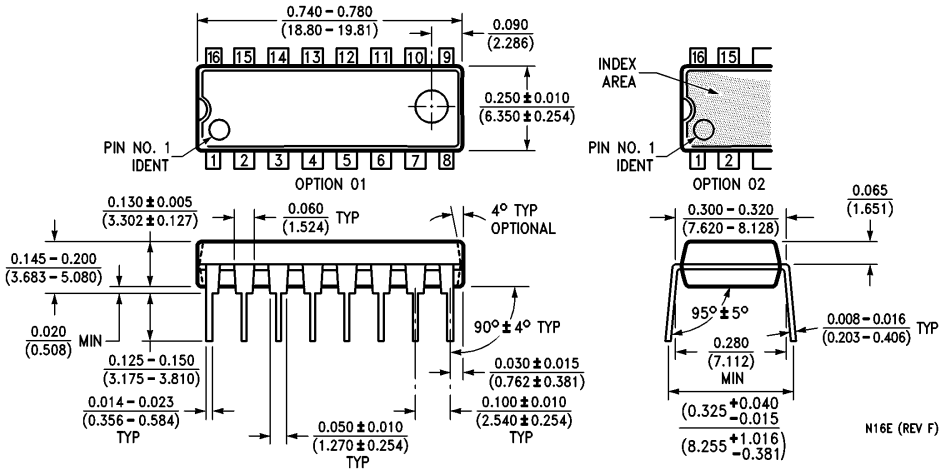
Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number CD4017BMJ, CD4017BCJ, CD4022BMJ, CD4022BCJ
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number CD4017BMN, CD4017BCN, CD4022BMN, CD4022BCN
NS Package Number N16E

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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National Semiconductor

February 1988

CD4528BM/CD4528BC Dual Monostable Multivibrator

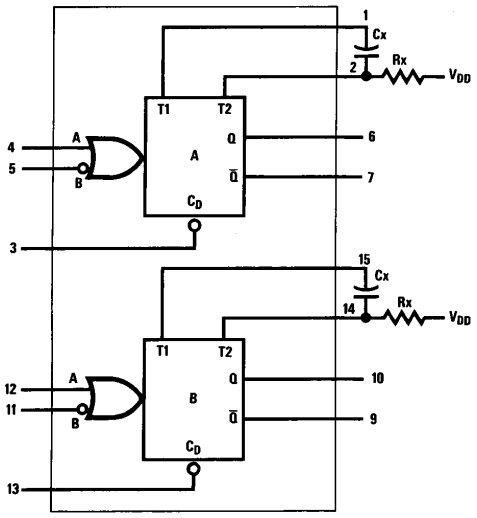
General Description

The CD4528B is a dual monostable multivibrator. Each device is retriggerable and resettable. Triggering can occur from either the rising or falling edge of an input pulse, resulting in an output pulse over a wide range of widths. Pulse duration and accuracy are determined by external timing components Rx and Cx.

Features

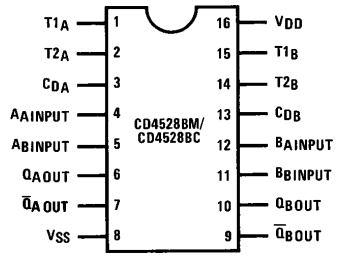
- Wide supply voltage range 3.0V to 18V
- Separate reset available
- Quiescent current = 5.0 nA/package (typ.) at 5.0 V_{DC}
- Diode protection on all inputs
- Triggerable from leading or trailing edge pulse
- Capable of driving two low-power TTL loads or one low-power Schottky TTL load over the rated temperature range

Connection Diagrams



TL/F/5998–1

Dual-In-Line Package



TL/F/5998–2

Top View

Order Number CD4528B

Truth Table

Inputs			Outputs	
Clear	A	B	Q	Q
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⎍	⎎
H	↑	H	⎍	⎎

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⎍ = One High Level Pulse
⎎ = One Low Level Pulse
X = Irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
Input Voltage, All Inputs (V_{IN})	$-0.5\ V_{DC}$ to $V_{DD} + 0.5\ V_{DC}$
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3V to 15V
Input Voltage (V_{IN})	0V to $V_{DD}\ V_{DC}$
Operating Temperature Range (T_A)	
CD4528BM	$-55°C$ to $+125°C$
CD4528BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4528BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		5	0.005		5		150	μA
		$V_{DD} = 10V$		10	0.010		10		300	μA
		$V_{DD} = 15V$		20	0.015		20		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$		0.05			0.05		0.05	V
		$V_{DD} = 10V$		0.05			0.05		0.05	V
		$V_{DD} = 15V$		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$	4.95		4.95	5.0		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10.0		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15.0		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$ or 4.5V		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1V$ or 9V		3.0		4.50	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$ or 4.5V	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$, $V_O = 1V$ or 9V	7.0		7.0	5.50		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 4.6V$	−0.25		−0.2	−0.36		−0.14		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−0.62		−0.5	−0.9		−0.35		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−1.8		−1.5	−3.5		−1.1		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

DC Electrical Characteristics CD4528BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.005	20		150	μA
		V_{DD} = 10V		40		0.010	40		300	μA
		V_{DD} = 15V		80		0.015	80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10V	9.95		9.95	10.0		9.95		V
		V_{DD} = 15V	14.95		14.95	15.0		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.2		−0.16	−0.36		−0.12		mA
		V_{DD} = 10V, V_O = 9.5V	−0.5		−0.4	−0.9		−0.3		mA
		V_{DD} = 15V, V_O = 13.5V	−1.4		−1.2	−3.5		−1.0		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

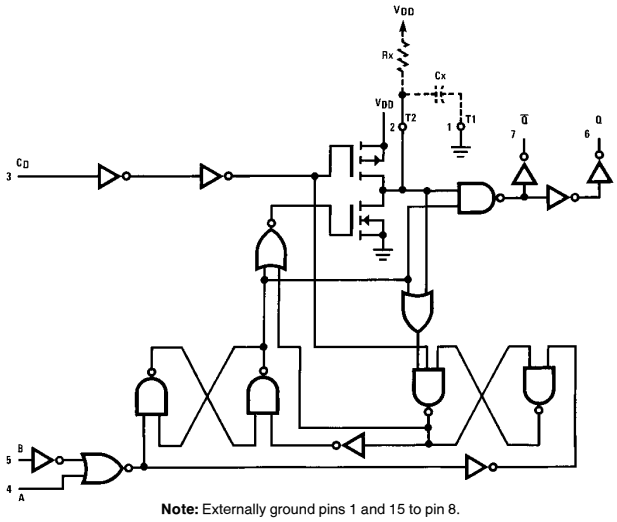
AC Electrical Characteristics* CD4528BM

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kΩ, Input $t_r = t_f = 20$ ns, unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Output Rise Time	$t_r = (3.0 \text{ ns/pF}) C_L + 30$ ns, $V_{DD} = 5.0V$		180	400	ns
	$t_r = (1.5 \text{ ns/pF}) C_L + 15$ ns, $V_{DD} = 10.0V$		90	200	ns
	$t_r = (1.1 \text{ ns/pF}) C_L + 10$ ns, $V_{DD} = 15.0V$		65	160	ns
Output Fall Time	$t_f = (1.5 \text{ ns/pF}) C_L + 25$ ns, $V_{DD} = 5.0V$		100	200	ns
	$t_f = (0.75 \text{ ns/pF}) C_L + 12.5$ ns, $V_{DD} = 10V$		50	100	ns
	$t_f = (0.55 \text{ ns/pF}) C_L + 9.5$ ns, $V_{DD} = 15.0V$		35	80	ns
Turn-Off, Turn-On Delay	$t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 240$ ns, $V_{DD} = 5.0V$		230	500	ns
A or B to Q or $\overline{Q}$	$t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 8$ ns, $V_{DD} = 10.0V$		100	250	ns
Cx = 15 pF, Rx = 5.0 kΩ	$t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 65$ ns, $V_{DD} = 15.0V$		65	150	ns
Turn-Off, Turn-On Delay	$t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 620$ ns, $V_{DD} = 5.0V$		230	500	ns
A or B to Q or $\overline{Q}$	$t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 257$ ns, $V_{DD} = 10.0V$		100	250	ns
Cx = 100 pF, Rx = 10 kΩ	$t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 185$ ns, $V_{DD} = 15.0V$		65	150	ns
Minimum Input Pulse Width	$V_{DD} = 5.0V$		60	150	ns
A or B	$V_{DD} = 10.0V$		20	50	ns
Cx = 15 pF, Rx = 5.0 kΩ	$V_{DD} = 15V$		20	50	ns
Cx = 1000 pF, Rx = 10 kΩ	$V_{DD} = 5.0V$		60	150	ns
	$V_{DD} = 10.0V$		20	50	ns
	$V_{DD} = 15.0V$		20	50	ns
Output Pulse Width Q or $\overline{Q}$	$V_{DD} = 5.0V$		550		ns
For Cx < 0.01 μF (See Graph for Appropriate V_{DD} Level)	$V_{DD} = 10.0V$		350		ns
Cx = 15 pF, Rx = 5.0 kΩ	$V_{DD} = 15.0V$		300		ns
For Cx > 0.01 μF Use	$V_{DD} = 5.0V$	15	29	45	μs
$PW_{out} = 0.2$ Rx Cx In $[V_{DD} - V_{SS}]$	$V_{DD} = 10.0V$	10	37	90	μs
Cx = 10,000 pF, Rx = 10 kΩ	$V_{DD} = 15.0V$	15	42	95	μs
Pulse Width Match between Circuits	$V_{DD} = 5.0V$		6	25	%
in the Same Package	$V_{DD} = 10.0V$		8	35	%
Cx = 10,000 pF, Rx = 10 kΩ	$V_{DD} = 15.0V$		8	35	%
Reset Propagation Delay,	$V_{DD} = 5.0V$		325	600	ns
t_{PLH}, t_{PHL}	$V_{DD} = 10.0V$		90	225	ns
Cx = 15 pF, Rx = 5.0 kΩ	$V_{DD} = 15.0V$		60	170	ns
Cx = 1000 pF, Rx = 10 kΩ	$V_{DD} = 5.0V$		7.0		μs
	$V_{DD} = 10.0V$		6.7		μs
	$V_{DD} = 15.0V$		6.7		μs
Minimum Retrigger Time	$V_{DD} = 5.0V$		0		ns
Cx = 15 pF, Rx = 5.0 kΩ	$V_{DD} = 10.0V$		0		ns
	$V_{DD} = 15.0V$		0		ns
Cx = 1000 pF, Rx = 10 kΩ	$V_{DD} = 5.0V$		0		ns
	$V_{DD} = 10.0V$		0		ns
	$V_{DD} = 15.0V$		0		ns

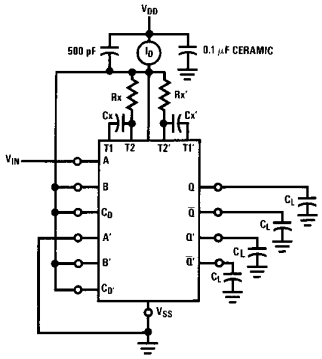
*AC parameters are guaranteed by DC correlated testing.

Logic Diagrams (1/2 of Device Shown)

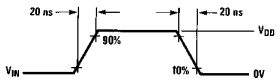


Note: Externally ground pins 1 and 15 to pin 8.

TL/F/5998–3



TL/F/5998–4



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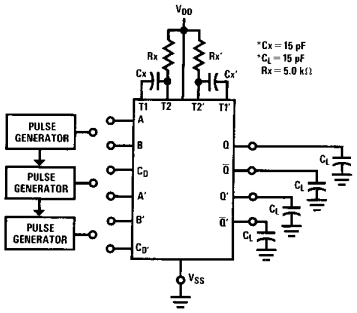
Duty Cycle = 50%

FIGURE 1. Power Dissipation Test Circuit and Waveforms



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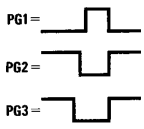
Input Connections

Characteristics	C_D	A	B
t_{PLH}, t_{PHL}, t_r, t_f, PW_{out}, PW_{in}	V_{DD}	PG1	V_{DD}
t_{PLH}, t_{PHL}, t_r, t_f, PW_{out}, PW_{in}	V_{DD}	V_{SS}	PG2
$t_{PLH(R)}$, $t_{PHL(R)}$, PW_{in}	PG3	PG1	PG2

*Includes capacitance of probes, wiring, and fixture parasitic.

Note: AC test waveforms for PG1, PG2, and PG3 on next page.



TL/F/5998–6

FIGURE 2. AC Test Circuit

Logic Diagrams (½ of Device Shown) (Continued)

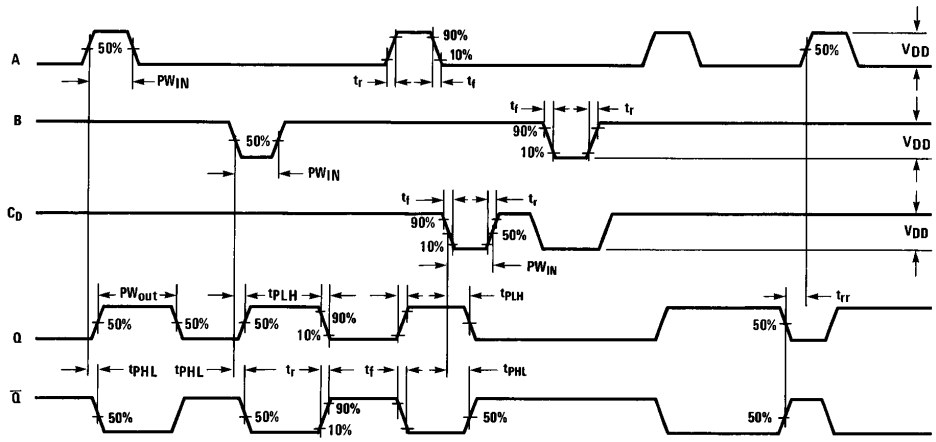


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FIGURE 3. AC Test Waveforms

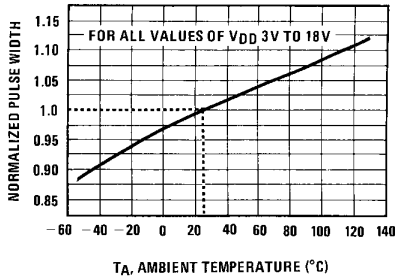

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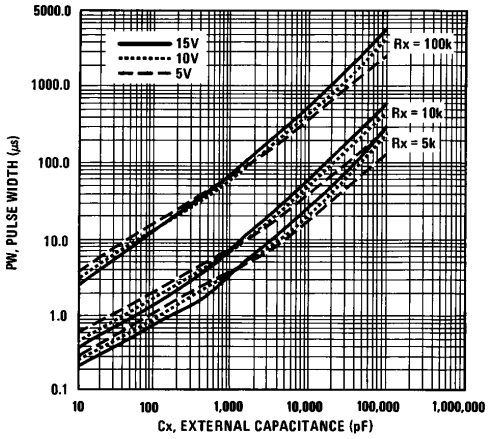
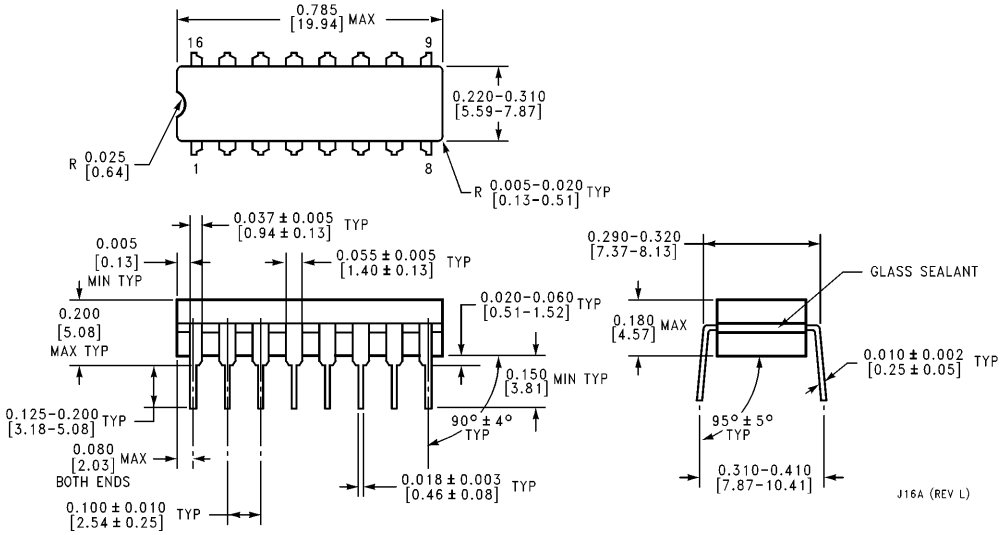
FIGURE 4. Normalized Pulse Width vs Temperature



TL/F/5998–9

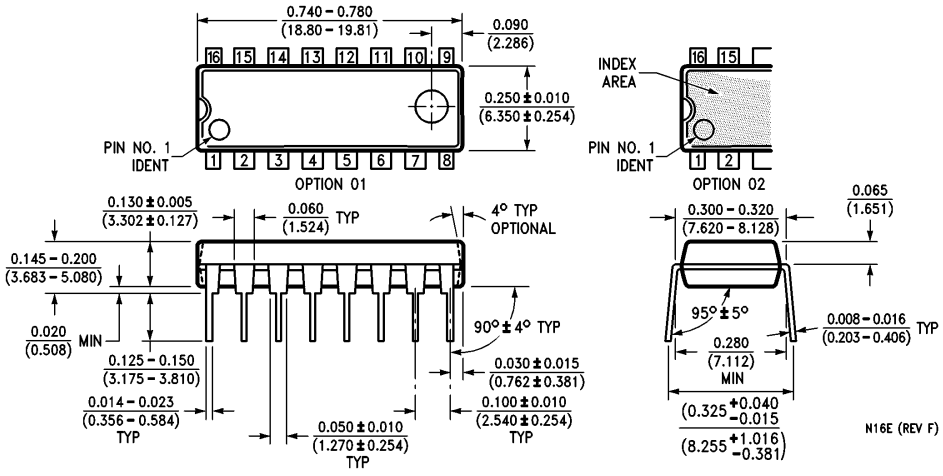
FIGURE 5. Pulse Width vs Cx

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number CD4528BMJ or CD4528BCJ
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number CD4528BMN or CD4528BCN
NS Package Number N16E

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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For more than two decades, ceramic filter technology has been instrumental in the proliferation of solid state electronics. A view of the future reveals that even greater expectations will be placed on piezoelectric material in the area of new applications and for more stringent performance criteria in current products. Traditionally, nearly all low and high-end AM and FM commercial radios use ceramic band-pass filters. However, applications are also found in cordless telephones, cellular systems, 2-way communications, and the television industry.

As a world leader in the development of piezo ceramic filter technology, Murata Electronics had been able to develop specialized ceramic materials which when combined with an advance filter design have resulted in a complete line of practical, inexpensive ceramic filters for entertainment and communications applications. In this catalog, the principle of ceramic filters, the design of representative test circuits and specifications concerning various models are described.

PIEZOELECTRIC THEORY AS APPLIED TO CERAMIC FILTERS

All ceramic filters derive their basic frequency selectivity from a mechanical vibration resulting from a piezoelectric effect. While a total theoretical analysis of piezoelectric technology as applied to ceramic filters is very complex, it can be shown as the equivalent circuit as illustrated in Fig. 426-1. This equivalent circuit represents a typical two-terminal filter, a device which forms the basic building block for more complex filters.

The resonant frequency of this device is calculated by the equation:

$$f_r = \frac{1}{2\pi\sqrt{L_1 C_1}}$$

The anti-resonant frequency is expressed as:

$$f_a = \frac{1}{2\pi\sqrt{L_1 \frac{C_1 C_0}{C_1 + C_0}}}$$

This filter exhibits the impedance shown in Fig. 426-2.

Two-terminal filters are typically used as emitter bypasses and they exhibit the frequency characteristics shown in Fig. 426-3.

Three-terminal ceramic filters can be used as inter-stage coupling devices as shown in Fig. 426-4. By using our filters in this manner, increased selectivity, improved band pass characteristics, reliability and stability can be obtained without increasing circuit complexity or parts count.

By cascading two or more filters as shown in Figs. 427-5 and 6, Murata can greatly enhance selectivity. By controlling the coefficient of electromechanical coupling between the filter elements, bandwidth can be “peaked” or “flattened.” Typical 455kHz response curves are shown in Figs. 427-7 and 8.

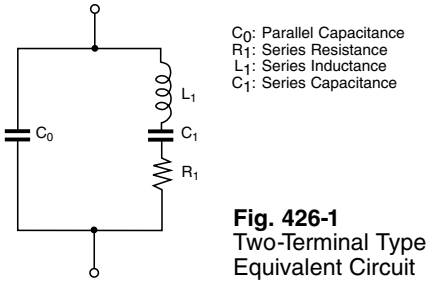


Fig. 426-1
Two-Terminal Type
Equivalent Circuit

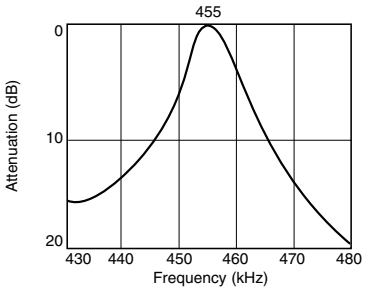


Fig. 426-3
Typical Attenuation Characteristics
For A 455kHz (Two-Terminal)
Ceramic Filter

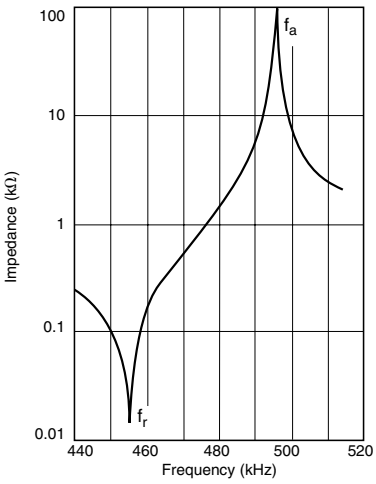


Fig. 426-2
Typical Impedance vs
Frequency Response Curve For
A Two-Terminal Device

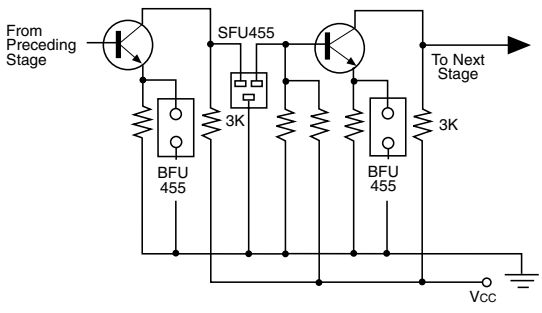


Fig. 426-4
Three-Terminal
Filter Used As Inter-Stage
Coupling Device

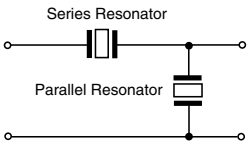


Fig. 427-5
Ladder Connection

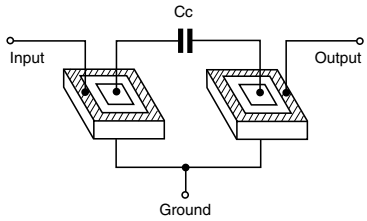


Fig. 427-6
Cascade Connection

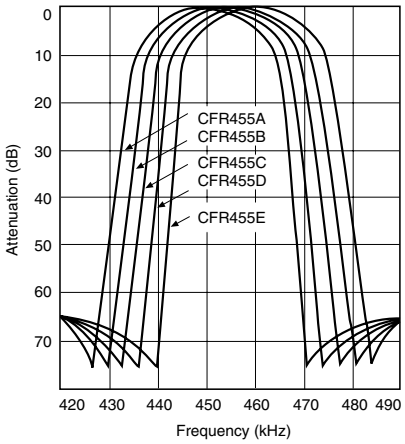


Fig. 427-7
Typical Response Curves For
CFR455 A-E Series Ceramic Filters

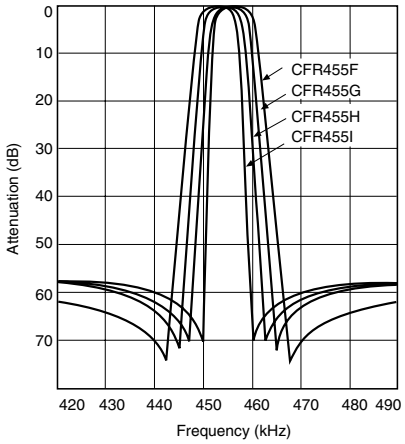


Fig. 427-8
Typical Response Curves For
CFR455 F-I Series Ceramic Filters

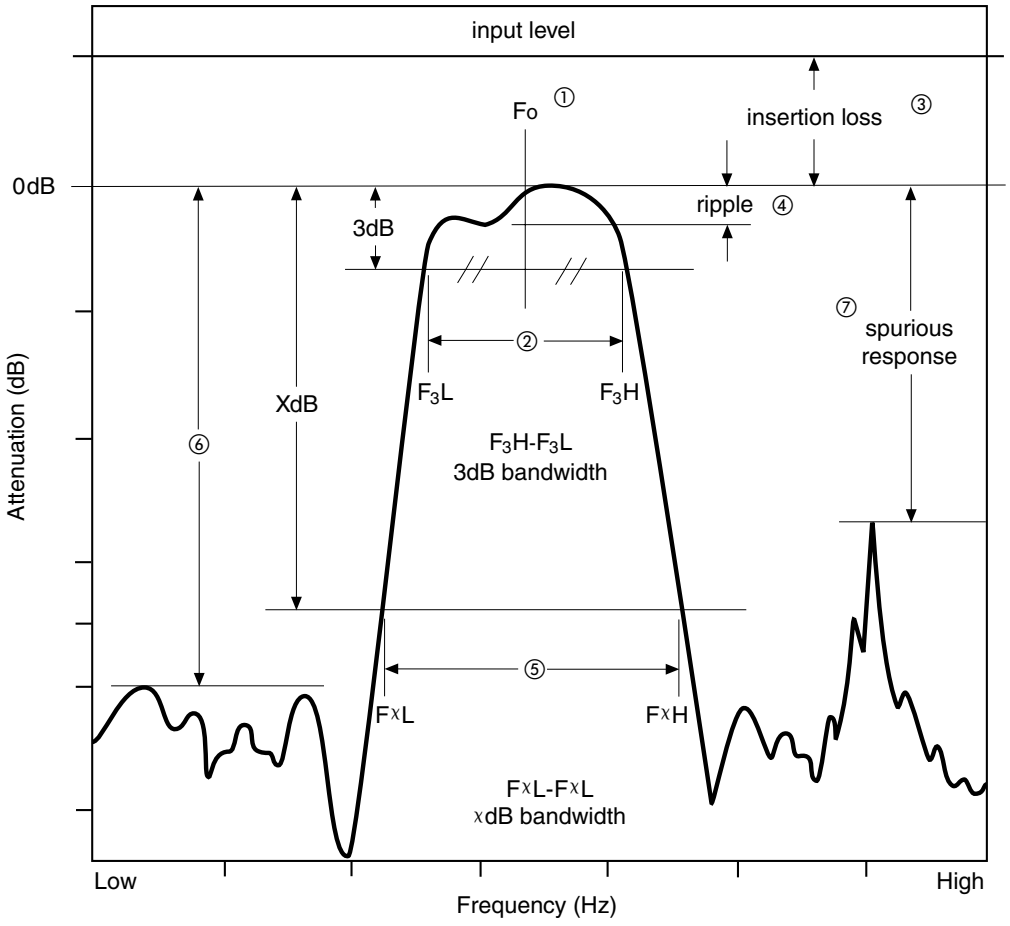


Fig. 427-9
Graphical Representation of Ceramic Filter Terminology

CERAMIC FILTER TERMINOLOGY

Although the previous section has presented a concise discussion of piezoelectric theory as applied to ceramic filter technology, it is necessary that the respective terminology used in conjunction with ceramic filters be discussed before any further examination of ceramic filter technology is made.

Using Fig.427-9 as a typical model of a response curve for a ceramic filter, it can be seen that there are a number of relevant factors to be considered in specifying ceramic filters. These include: center frequency, pass-bandwidth, insertion loss, ripple, attenuation bandwidth, stopband attenuation, spurious response and selectivity. Although not all of these factors will apply to each filter design, these are the key specifications to consider with most filters. From the symbol key shown in Table 428-1 below, a thorough understanding of this basic terminology should be possible.

IMPEDANCE MATCHING

As it is imperative to properly match the impedances whenever any circuit is connected to another circuit, any component to another component, or any circuit to another component, it is also important that this be taken into account in using ceramic filters. Without proper impedance matching, the operational characteristics of the ceramic filters cannot be met.

Fig. 429-12 illustrates a typical example of this requirement.

This example shows the changes produced in the frequency characteristics of the SFZ455A ceramic filter when the resistance values are altered. For instance, if the input/output impedances R_1 and R_2 are connected to lower values than those specified, the insertion loss increases, the center frequency shifts toward the low side and the ripple increases.

TABLE 432-1 – CERAMIC FILTER TERMINOLOGY CHART

Numbers In Fig. 427-9	Terminology	Symbol	Unit	Explanation of Term
1	Center Frequency	f_o	Hz	The frequency in the center of the pass-bandwidth. However, the center frequency for some products is expressed as the point where the loss is at its lowest point.
2	Pass-bandwidth (3dB Bandwidth)	(3dB) B.W.	Hz	Signifies a difference between the two frequencies where the attenuation becomes 3dB from the level of the minimum loss point.
3	Insertion Loss	I.L.	dB	Expressed as the input/output ratio at the point of minimum loss. (The insertion loss for some products is expressed as the input/output ratio at the center frequency.) Insertion loss = 20 LOG (V_2/V_1) in dB.
4	Ripple	—	dB	If there are peaks and valleys in the pass-bandwidth, the ripple expresses the difference between the maximum peak and the minimum valley.
5	Attenuation Bandwidth (dB Bandwidth)	20 (dB) (B.W.)	Hz	The bandwidth at a specified level of attenuation. Attenuation may be expressed as the ratio of the input signal strength to the output signal strength in decibels.
6	Stopband Attenuation	—	dB	The level of signal strength at a specified frequency outside of the passband.
7	Spurious Response	SR	dB	The difference in decibels between the insertion loss and the spurious signal in the stopband.
	Input/Output Impedance	—	Ohm	Internal impedance value of the input and output of the ceramic filter
	Selectivity	—	dB	The ability of a filter to pass signals of one frequency and reject all others. A highly selective filter has an abrupt transition between a passband region and the stopband region. This is expressed as the shape factor—the attenuation bandwidth divided by the pass - bandwidth. The filter becomes more selective as the resultant value approaches one.

On the other hand, if R_1 and R_2 are connected to higher values other than those specified, the insertion loss will increase, the center frequency will shift toward the high side and the ripple will increase.

DEALING WITH SPURIOUS RESPONSE

Frequently in using 455kHz filters, spurious will cause problems due to the fact that the resonance occurs under an alien vibrating mode or overtone deviating from the basic vibration characteristics. Among available solutions for dealing with spurious response are:

1. The use of a supplementary IFT together with the ceramic filter for suppression of the spurious.
2. The arrangement of two or more ceramic filters in parallel for the mutual cancellation of spurious.
3. The addition of a low-pass or high-pass LC filter for suppression of spurious. Perhaps the most commonly used method of dealing with spurious is the use of a supplementary IFT in conjunction with the ceramic filter. The before and after effects of the use of an IFT are shown in Figs. 429-10 and 11. In Fig. 429-10, only a single SFZ455A ceramic filter is employed and spurious is a significant problem. With the addition of an IFT, the spurious problem is reduced as is shown in Fig. 429-11.

Although spurious is a significant problem to contend with when using 455kHz ceramic filters, it is not a problem in 4.5MHz and 10.7MHz ceramic filters, as their vibration modes are significantly different.

CONSIDERATIONS FOR GAIN DISTRIBUTION

Since the impedance of both the input and output values of the ceramic filters are symmetric and small, it is necessary that the overall gain distribution within the circuit itself be taken into consideration. For instance, in the discussion concerning proper impedance matching, it was illustrated that a certain DC loss occurs if the recommended resistance values are not used. This can cause an overall reduction in the gain which could present a problem if no allowances have been made for the corresponding loss. To compensate for this problem, it is recommended that the following be done:

1. The amplifier stage should be designed to compensate for this loss.
2. The ceramic filter should be used in combination with the IFT for minimizing both matching and DC losses. The IFT should be used strictly as a matching transformer and the ceramic filter only for selectivity.

As the use of IC's has become more prevalent with ceramic filters, these considerations have been taken into account. It should be noted that few of the problems discussed above have been realized when more than three (3) IF stages have been employed.

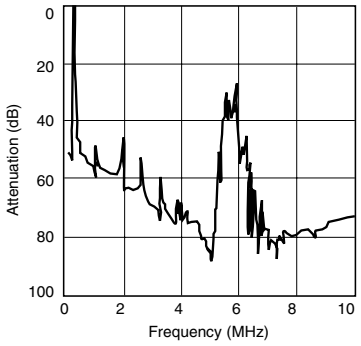


Fig. 429-10
Spurious Response With Model SFZ455A Ceramic Filter

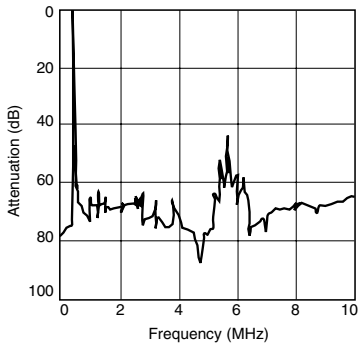


Fig. 429-11
Spurious Response With Model SFZ455A Ceramic Filter And IFT

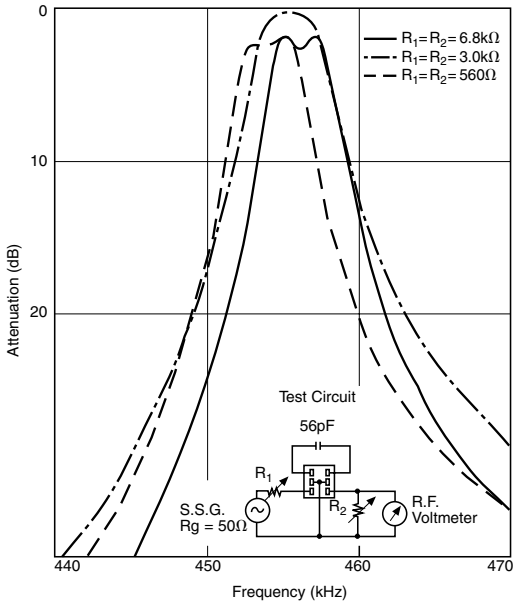


Fig. 429-12
Model SFZ455A Ceramic Filter Matching Impedance vs. Pass-Band Characteristics

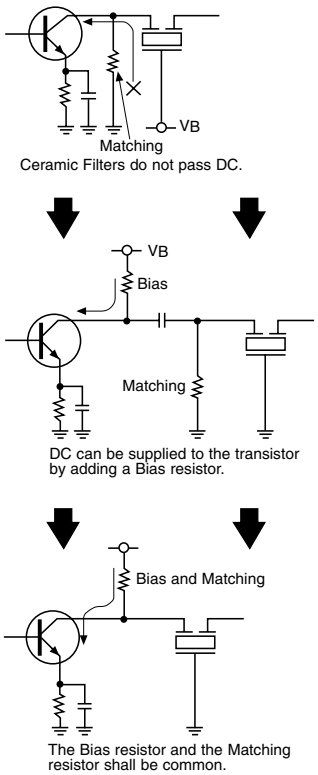


Fig. 429-13
Coupling With A Transistor

CERAMIC FILTERS DO NOT PASS DC

It is important to note in designing circuits that ceramic filters are incapable of passing DC. As is illustrated in Fig. 429-13, in a typical circuit where a transistor is used, a bias circuit will be required to drive the transistor. Since the ceramic filter requires matching resistance to operate properly, the matching resistor shown in the diagram can play a dual role as both a matching and bias resistor.

If the bias circuit is used, it is important that the parallel circuit of both the bias resistance and the transistor's internal resistance be taken into consideration in meeting the resistance values. This is necessary since the internal resistance of the transistor is changed by the bias resistance. However, when an IC is used, there is no need for an additional bias circuit since the IC has a bias circuit within itself.

Here it is recommended that an IFT be used for impedance matching with the ceramic filter when coupling with a mixer stage, as shown in Fig. 430-14.

COUPLING CAPACITANCE

The SFZ455A is composed of two filter elements which must be connected by a coupling capacitor. Moreover, the frequency characteristic changes according to the coupling capacitance (Cc). As shown in Fig. 430-15, the larger the coupling capacitance (Cc) becomes, the wider the bandwidth and more the ripple increases. Conversely, the smaller the coupling capacitance becomes, the narrower the bandwidth becomes and the more the insertion loss increases. Therefore, the specified value of the coupling capacitance in the catalog is desired in determining the specified passband characteristics.

GROUP DELAY TIME CHARACTERISTICS

Perhaps one of the most important characteristics of a transmitting element is to transmit a signal with the lowest possible distortion level. This distortion occurs when the phase shift of a signal which passes through a certain transmitting path is non-linear with respect to the frequency. For convenience, the group delay time (GDT) characteristic is used for the purpose of expressing non-linearity.

It is important to note the relationship between the amplitude and the GDT characteristics when using group delay time terminology. This relationship differs depending upon the filter characteristics. For example, in the Butterworth type, which has a relatively flat top, the passband is flat while the GDT characteristic is extremely curved, as shown in Fig. 430-16. On the other hand, a Gaussian type, is curved in the passband, while the GDT characteristic is flat. With the flat GDT characteristics, the Gaussian type has excellent distortion characteristics.

Since the amplitude characteristics for the Butterworth type is flat in the passband the bandwidth does not change even at a low input level. With the amplitude characteristic for the Gaussian type being curved in the passband, the bandwidth becomes narrow at a low input level and the sensitivity is poor. Therefore, it should be noted that the Gaussian type has a desirable distortion factor while the Butterworth type has the desirable sensitivity.

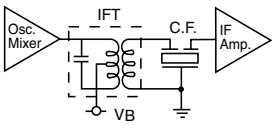


Fig. 430-14
Coupling From Mixer Stage

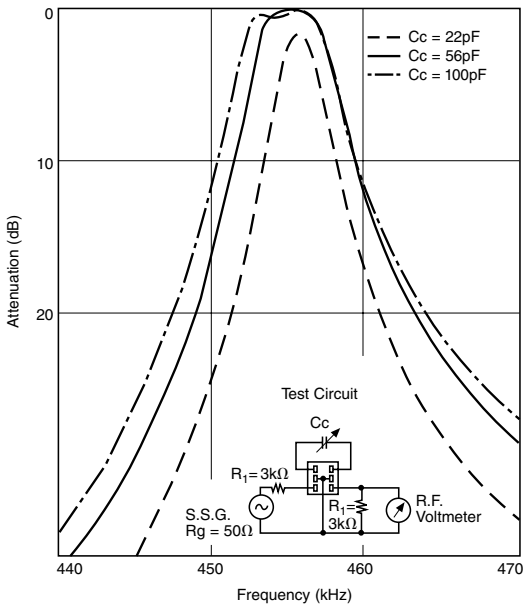


Fig. 430-15
Model SFZ455A Ceramic Filter Coupling Capacitance vs. Passband Characteristics

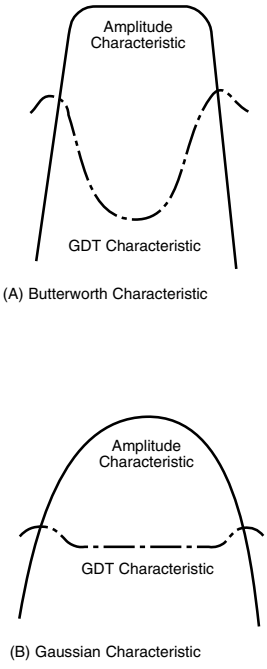


Fig. 430-16
Relationship Between Amplitude And GDT Characteristics

PIEZO FILTERS
MULTI-ELEMENT, ULTRA-MINIATURE

muRata
Innovator in Electronics

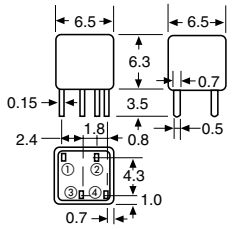
CFUM/CFWM 455kHz

The CFUM 455 and CFWM 455 lines of ceramic filters are miniaturized versions of the CFU/CFWS lines. These ultra-miniature versions consume approximately 40% less volume while still offering the same high performance filter characteristics available with the CFU/CFWS lines. (Also available in 450kHz version.)

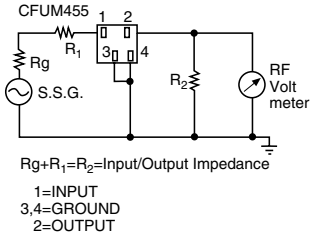
SPECIFICATIONS — CFUM 455kHz

Part Number	Nominal Center Frequency (kHz)	6dB Bandwidth (kHz) min.	40dB Bandwidth (kHz) max.	Attenuation 455±100kHz (dB) min.	Insertion Loss (dB) max.	Input/Output Impedance (Ohms)
★CFUM455B	455	±15	±30	27	4	1500
★CFUM455C	455	±12.5	±24	27	4	1500
★CFUM455D	455	±10	±20	27	4	1500
★CFUM455E	455	±7.5	±15	27	6	1500
★CFUM455F	455	±6	±12.5	27	6	2000
★CFUM455G	455	±4.5	±10	25	6	2000
★CFUM455H	455	±3	±9	35	6	2000
★CFUM455I	455	±2	±7.5	35	7	2000

DIMENSIONS: mm



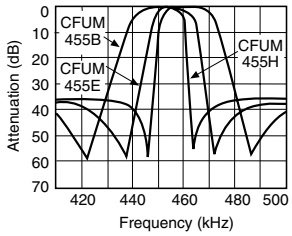
CIRCUIT



$Rg+R_1=R_2$=Input/Output Impedance

1=INPUT
3,4=GROUND
2=OUTPUT

CHARACTERISTICS

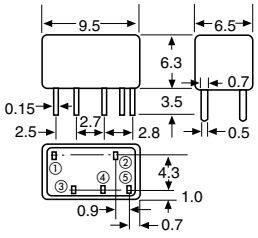


SPECIFICATIONS — CFWM 455kHz

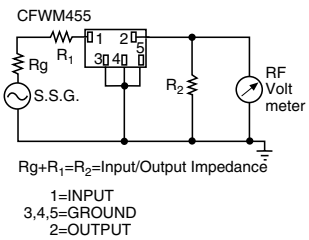
Part Number	Nominal Center Frequency (kHz)	6dB Bandwidth (kHz) min.	40dB Bandwidth (kHz) max.	Attenuation 455±100kHz (dB) min.	Insertion Loss (dB) max.	Input/Output Impedance (Ohms)
★CFWM455B	455	±15	±30	35	4	1500
★CFWM455C	455	±12.5	±24	35	4	1500
★CFWM455D	455	±10	±20	35	4	1500
★CFWM455E	455	±7.5	±15	35	6	1500
★CFWM455F	455	±6	±12.5	35	6	2000
★CFWM455G	455	±4.5	±10	35	6	2000
★CFWM455H	455	±3	±9	55	6	2000
★CFWM455I	455	±2	±7.5	55	7	2000

• CFWM455☐ series filters are 6-element ceramic filters and ultraminiature versions of CFWS455☐ series.

DIMENSIONS: mm



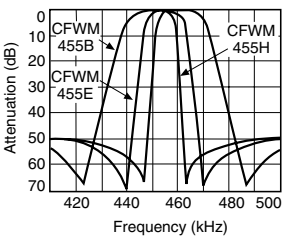
CIRCUIT



$Rg+R_1=R_2$=Input/Output Impedance

1=INPUT
3,4,5=GROUND
2=OUTPUT

CHARACTERISTICS



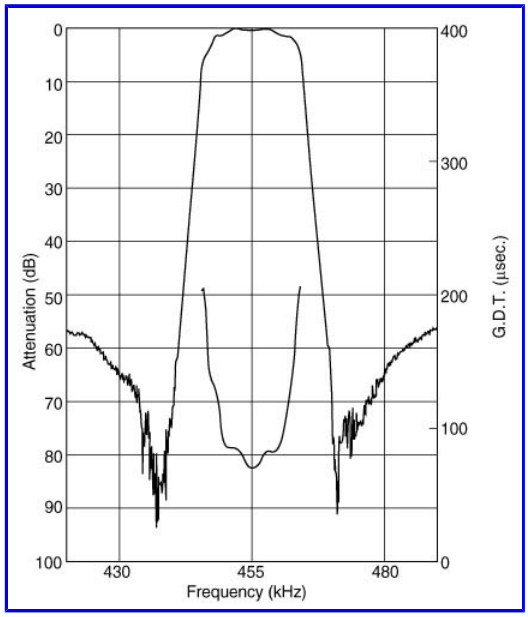
★Available as standard through authorized Murata Electronics Distributors.

***Note:** For safety purposes, connect the output of filters to the IF amplifier through a DC blocking capacitor. Avoid applying a direct current to the output of ceramic filters.

CFWS455E

Caractéristiques

Part Number	CFWS455E
Center Frequency (fo)	
Nominal Center Frequency (fn)	455.0kHz
3dB Bandwidth	
6dB Bandwidth	fn±7.5kHz min.
Stop Bandwidth	fn±15.0kHz max.
Area of Stop Bandwidth	[within 50dB]
Stop Band Att.(1)	35dB min.
Area of Stop Band Att.(1)	[within fn±100kHz]
Insertion Loss	6.0dB max.
Area of Insertion Loss	[at minimum loss point]
Ripple	3.0dB max.
Area of Ripple	[within fn±5kHz]
Input/Output Impedance	1500ohm



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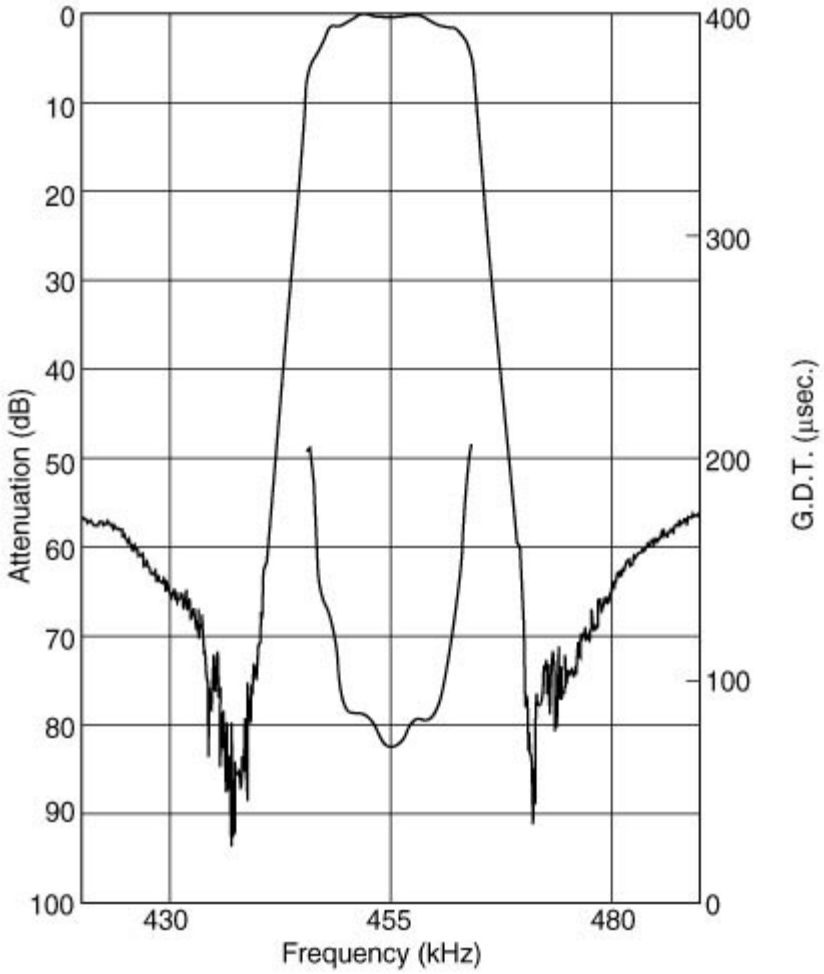
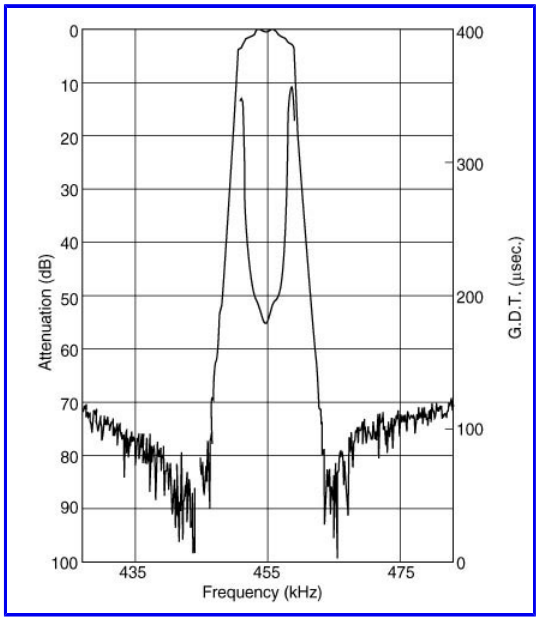

0
10
20
30
40
50
60
70
80
90
100
Attenuation (dB)
400
300
200
100
0
G.D.T. (µsec.)
430
455
480
Frequency (kHz)

CFWS455HT

Caractéristiques

Part Number	CFWS455HT
Center Frequency (fo)	
Nominal Center Frequency (fn)	455.0kHz
3dB Bandwidth	
6dB Bandwidth	fn±3.0kHz min.
Stop Bandwidth	fn±9.0kHz max.
Area of Stop Bandwidth	[within 50dB]
Stop Band Att.(1)	60dB min.
Area of Stop Band Att.(1)	[within fn±100kHz]
Insertion Loss	6.0dB max.
Area of Insertion Loss	[at minimum loss point]
Ripple	2.0dB max.
Area of Ripple	[within fn±2kHz]
Input/Output Impedance	2000ohm



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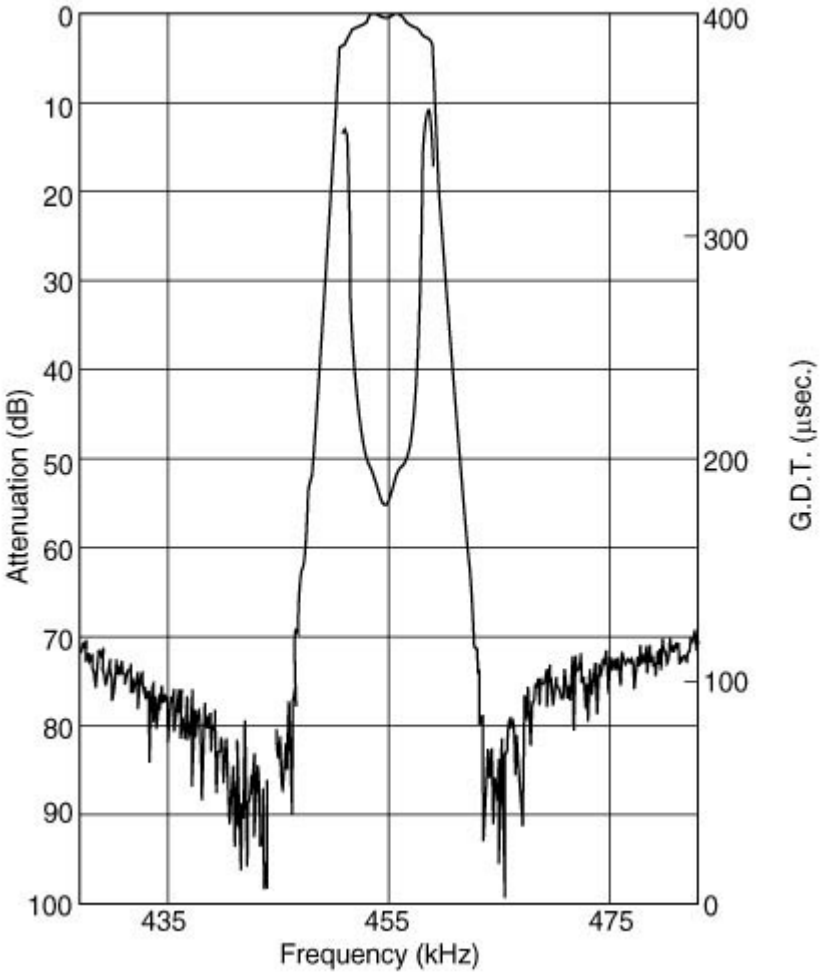
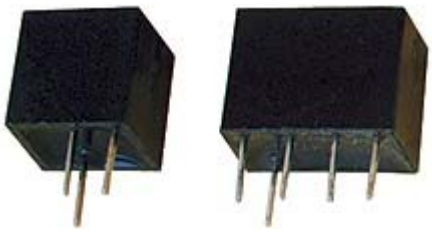

0
10
20
30
40
50
60
70
80
90
100
Attenuation (dB)
400
300
200
100
0
G.D.T. (µsec.)
435
455
475
Frequency (kHz)

Filtres centrés sur 455 KHz



Modèles	CFU455G	CFW455HT	CFW455G
BP à 6 dB	± 4,5 KHz*	± 3 KHz*	± 4,5 KHz*
BP à 50 dB	± 10 KHz*	± 9 KHz*	± 10 KHz*
Perte insertion	6 dB	6 dB	6 dB
Impédance E/S	2000 Ω	2000 Ω	2000 Ω

* Bande passante à 40 dB

30-N	Le filtre "CFU455G"	**2,55 € HT**	**3,05 € TTC**
30-O HT	Le filtre "CFW455HT"	**3,57 € HT**	**4,27 € TTC**
30-O G	Le filtre "CFW455G"	**3,57 € HT**	**4,27 € TTC**

The LM3900: A New Current-Differencing Quad of ± Input Amplifiers

National Semiconductor
Application Note 72
September 1972

PREFACE

With all the existing literature on ''how to apply op amps'' why should another application note be produced on this subject? There are two answers to this question; 1) the LM3900 operates in quite an unusual manner (compared to a conventional op amp) and therefore needs some explanation to familiarize a new user with this product, and 2) the standard op amp applications assume a split power supply ($\pm 15\ V_{DC}$) is available and our emphasis here is directed toward circuits for lower cost single power supply control systems. Some of these circuits are simply ''re-biased'' versions of conventional handbook circuits but many are new approaches which are made possible by some of the unique features of the LM3900.

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The LM3900: A New Current-Differencing Quad of ± Input Amplifiers

1.0 An Introduction to the New "Norton" Amplifier

The LM3900 represents a departure from conventional amplifier designs. Instead of using a standard transistor differential amplifier at the input, the non-inverting input function has been achieved by making use of a "current-mirror" to "mirror" the non-inverting input current about ground and then to extract this current from that which is entering the inverting input terminal. Whereas the conventional op amp differences input voltages, this amplifier differences input currents and therefore the name "Norton Amp" has been used to indicate this new type of operation. Many biasing advantages are realized when operating with only a single power supply voltage. The fact that currents can be passed between the input terminals allows some unusual applications. If external, large valued input resistors are used (to convert from input voltages to input currents) most of the standard op amp applications can be realized.

Many industrial electronic control systems are designed that operate off of only a single power supply voltage. The conventional integrated-circuit operational amplifier (IC op amp) is typically designed for split power supplies ($\pm 15\ V_{DC}$) and suffers from a poor output voltage swing and a rather large minimum common-mode input voltage range (approximately $+\ 2\ V_{DC}$) when used in a single power supply application. In addition, some of the performance characteristics of these op amps could be sacrificed—especially in favor of reduced costs.

To meet the needs of the designers of low-cost, single-power-supply control systems, a new internally compensated amplifier has been designed that operates over a power supply voltage range of $+4\ V_{DC}$ to $36\ V_{DC}$ with small changes in performance characteristics and provides an output peak-to-peak voltage swing that is only 1V less than the magnitude of the power supply voltage. Four of these amplifiers have been fabricated on a single chip and are provided in the standard 14-pin dual-in-line package.

The cost, application and performance advantages of this new quad amplifier will guarantee it a place in many single power supply electronic systems. Many of the "housekeeping" applications which are now handled by standard IC op amps can also be handled by this "Norton" amplifier operating off the existing $\pm 15\ V_{DC}$ power supplies.

1.1 BASIC GAIN STAGE

The gain stage is basically a single common-emitter amplifier. By making use of current source loads, a large voltage gain has been achieved which is very constant over temperature changes. The output voltage has a large dynamic range, from essentially ground to one V_{BE} less than the power supply voltage. The output stage is biased class A for small signals but converts to class B to increase the load current which can be "absorbed" by the amplifier under large signal conditions. Power supply current drain is essentially independent of the power supply voltage and ripple on the supply line is also rejected. A very small input biasing current allows high impedance feedback elements to be used and even lower "effective" input biasing currents can be realized by using one of the amplifiers to supply essentially all of the bias currents for the other amplifiers by making use of the "matching" which exists between the 4 amplifiers which are on the same IC chip (see *Figure 84*).

The simplest inverting amplifier is the common-emitter stage. If a current source is used in place of a load resistor, a large open-loop gain can be obtained, even at low power-supply voltages. This basic stage (*Figure 1*) is used for the amplifier.

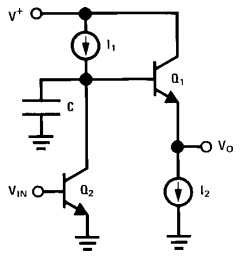

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FIGURE 1. Basic Gain Stage

All of the voltage gain is provided by the gain transistor, Q_2, and an output emitter-follower transistor, Q_1, serves to isolate the load impedance from the high impedance that exists at the collector of the gain transistor, Q_2. Closed-loop stability is guaranteed by an on-chip capacitor $C = 3$ pF, which provides the single dominant open-loop pole. The output emitter-follower is biased for class-A operation by the current source I_2.

This basic stage can provide an adequate open-loop voltage gain (70 dB) and has the desired large output voltage swing capability. A disadvantage of this circuit is that the DC input current, I_{IN}, is large; as it is essentially equal to the maximum output current, I_{OUT}, divided by β^2. For example, for an output current capability of 10 mA the input current would be at least 1 μA (assuming $\beta^2 = 10^4$). It would be desirable to further reduce this by adding an additional transistor to achieve an overall β^3 reduction. Unfortunately, if a transistor is added at the output (by making Q_1 a Darlington pair) the peak-to-peak output voltage swing would be somewhat reduced and if Q_2 were made a Darlington pair the DC input voltage level would be undesirably doubled.

To overcome these problems, a lateral PNP transistor has been added as shown in *Figure 2*. This connection neither reduces the output voltage swing nor raises the DC input voltage, but does provide the additional gain that was needed to reduce the input current.

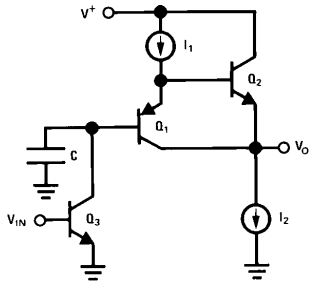

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FIGURE 2. Adding a PNP Transistor to the Basic Gain Stage

Notice that the collector of this PNP transistor, Q_1, is connected directly to the output terminal. This ''bootstraps'' the output impedance of Q_1 and therefore reduces the loading at the high-impedance collector of the gain transistor, Q_3.

In addition, the collector-base junction of the PNP transistor becomes forward biased under a large-signal negative output voltage swing condition. The design of this device has allowed Q_1 to convert to a vertical PNP transistor during this operating mode which causes the output to change from the class A bias to a class B output stage. This allows the amplifier to sink more current than that provided by the current source I_2, (1.3 mA) under large signal conditions.

1.2 OBTAINING A NON-INVERTING INPUT FUNCTION

The circuit of *Figure 2* has only the inverting input. A general purpose amplifier requires two input terminals to obtain both an inverting and a non-inverting input. In conventional op amp designs, an input differential amplifier provides these required inputs. The output voltage then depends upon the difference (or error) between the two input voltages. An input common-mode voltage range specification exists and, basically, input voltages are compared.

For circuit simplicity, and ease of application in single power supply systems, a non-inverting input can be provided by adding a standard IC ''current-mirror'' circuit directly across the inverting input terminal, as shown in *Figure 3*.

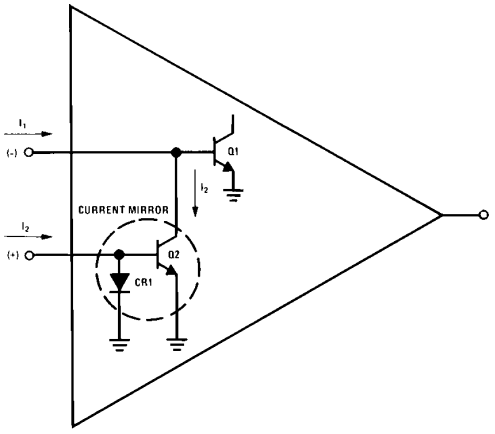

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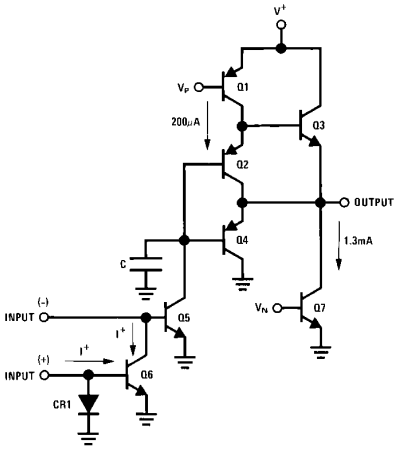
FIGURE 3. Adding a Current Mirror to Achieve a Non-inverting Input

This operates in the current mode as now input currents are compared or differenced (this can be thought of as a Norton differential amplifier). There is essentially no input common-mode voltage range directly at the input terminals (as both inputs will bias at one diode drop above ground) but if the input voltages are converted to currents (by use of input resistors), there is then no limit to the common-mode input voltage range. This is especially useful in high-voltage comparator applications. By making use of the input resistors, to convert input voltages to input currents, all of the standard op amp applications can be realized. Many additional applications are easily achieved, especially when operating with only a single power supply voltage. This results from the built-in voltage biasing that exists at both inputs (each input biases at $+ V_{BE}$) and additional resistors are not required to provide a suitable common-mode input DC biasing voltage level. Further, input summing can be performed at the relatively low impedance level of the input diode of the current-mirror circuit.

1.3 THE COMPLETE SINGLE-SUPPLY AMPLIFIER

The circuit schematic for a single amplifier stage is shown in *Figure 4a*. Due to the circuit simplicity, four of these amplifiers can be fabricated on a single chip. One common biasing circuit is used for all of the individual amplifiers.

A new symbol for this ''Norton'' amplifier is shown in *Figure 4b*. This is recommended to avoid using the standard op amp symbol as the basic operation is different. The current source symbol between the inputs implies this new current-mode of operation. In addition, it signifies that current is removed from the (−) input terminal. Also, the current arrow on the (+) input lead is used to indicate that this functions as a current input. The use of this symbol is helpful in understanding the operation of the application circuits and also in doing additional design work with the LM3900.



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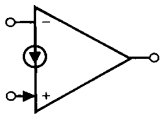
(a) Circuit Schematic



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(b) New ''NORTON'' Amplifier Symbol

FIGURE 4. The Amplifier Stage

The bias reference for the PNP current source, V_p which biases Q_1, is designed to cause the upper current source (200 μA) to change with temperature to give first order compensation for the β variations of the NPN output transistor, Q_3. The bias reference for the NPN ''pull-down'' current sink, V_n, (which biases Q_7) is designed to stabilize this current (1.3 mA) to reduce the variation when the temperature is changed. This provides a more constant pull-down capability for the amplifier over the temperature range. The transistor, Q_4, provides the class B action which exists under large signal operating conditions.

The performance characteristics of each amplifier stage are summarized below:

Power-supply voltage range ..... 4 to 36 V_{DC} or ± 2 to ± 18 V_{DC}

Bias current drain per amplifier stage ..... 1.3 mA_{DC}

Open loop:

- Voltage gain (R_L = 10k) ..... 70 dB
- Unity-gain frequency ..... 2.5 MHz
- Phase margin ..... 40°
- Input resistance ..... 1 MΩ
- Output resistance ..... 8 kΩ

Output voltage swing ..... (V_{CC} − 1) V_{pp}

Input bias current ..... 30 nA_{DC}

Slew rate 0.5V/μs

As the bias currents are all derived from diode forward voltage drops, there is only a small change in bias current magnitude as the power-supply voltage is varied. The open-loop gain changes only slightly over the complete power supply voltage range and is essentially independent of temperature changes. The open-loop frequency response is compared with the ''741'' op amp in *Figure 5*. The higher unity-gain crossover frequency is seen to provide an additional 10 dB of gain for all frequencies greater than 1 kHz.

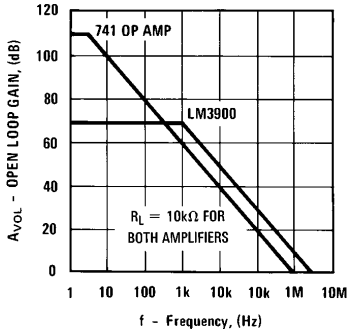

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FIGURE 5. Open-loop Gain Characteristics

The complete schematic diagram of the LM3900 is shown in *Figure 6*. The one resistor, R_5, establishes the power consumption of the circuit as it controls the conduction of transistor Q_{28}. The emitter current of Q_{28} is used to bias the NPN output class-A biasing current sources and the collector current of Q_{28} is the reference for the PNP current source of each amplifier.

The biasing circuit is initially ''started'' by Q_{20}, Q_{30} and CR_6. After start-up is achieved, Q_{30} goes OFF and the current flow through the reference diodes: CR_5, CR_7 and CR_8, is dependent only on $V_{BE}/(R_6 + R_7)$. This guarantees that the power supply current drain is essentially independent of the magnitude of the power supply voltage.

The input clamp for negative voltages is provided by the multi-emitter NPN transistor Q_{21}. One of the emitters of this transistor goes to each of the input terminals. The reference voltage for the base of Q_{21} is provided by R_6 and R_7 and is approximately $V_{BE}/2$.

2.0 Introduction to Applications of the LM3900

Like the standard IC op amp, the LM3900 has a wide range of applications. A new approach must be taken to design circuits with this ''Norton'' amplifier and the object of this note is to present a variety of useful circuits to indicate how conventional and unique new applications can be designed—especially when operating with only a single power supply voltage.

To understand the operation of the LM3900 we will compare it with the more familiar standard IC op amp. When operating on a single power supply voltage, the minimum input common-mode voltage range of a standard op amp limits the smallest value of voltage which can be applied to both inputs and still have the amplifier respond to a differential input signal. In addition, the output voltage will not swing completely from ground to the power supply voltage. The output voltage depends upon the difference between the input voltages and a bias current must be supplied to both inputs. A simplified diagram of a standard IC op amp operating from a single power supply is shown in *Figure 7*. The (+) and (−) inputs go only to current sources and therefore are free to be biased or operated at any voltage values which are within the input common-mode voltage range. The current sources at the input terminals, I_B^+ and I_B^-, represent the bias currents which must be supplied to both of the input transistors of the op amp (base currents). The output circuit is modeled as an active voltage source which depends upon the open-loop gain of the amplifier, A_V, and the difference which exists between the input voltages, ($V^+ - V^-$).

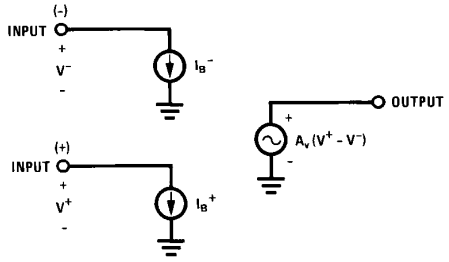

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FIGURE 7. An Equivalent Circuit of a Standard IC Op Amp

An equivalent circuit for the ''Norton'' amplifier is shown in *Figure 8*. The (+) and (−) inputs are both clamped by diodes to force them to be one-diode drop above ground—always! They are not free to move and the ''input common-mode voltage range'' directly at these input terminals is very small—a few hundred mV centered about 0.5 V_{DC}. This is

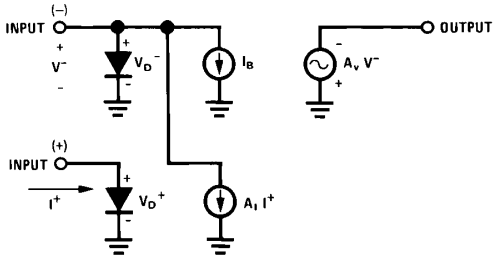

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FIGURE 8. An Equivalent Circuit of the ''Norton'' Amplifier

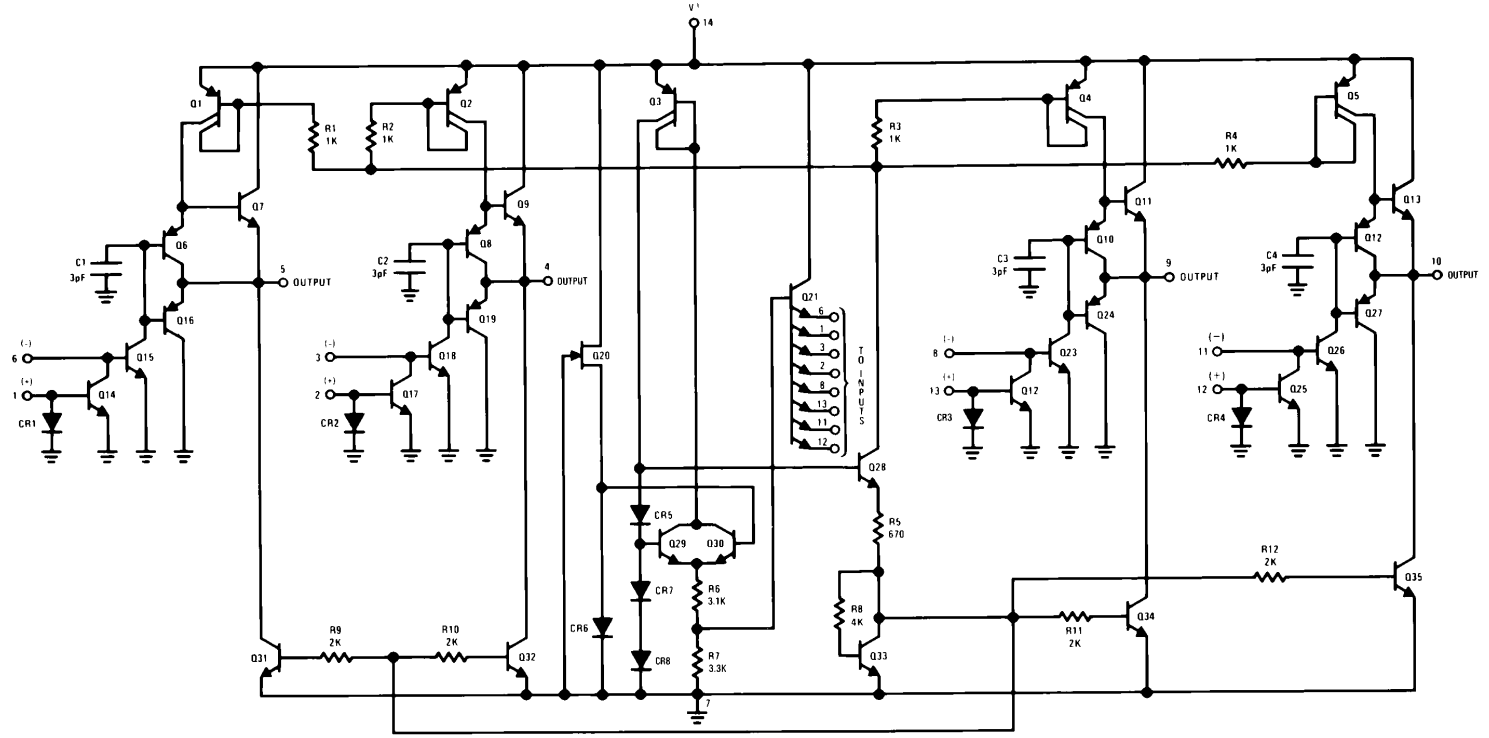

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FIGURE 6. Schematic Diagram of the LM3900

why external voltages must be first converted to currents (using resistors) before being applied to the inputs—and is the basis for the current-mode (or Norton) type of operation. With external input resistors—there is *no limit* to the ''input common-mode voltage range''. The diode shown across the (+) input actually exists as a diode in the circuit and the diode across the (−) input is used to model the base-emitter junction of the transistor which exists at this input.

Only the (−) input must be supplied with a DC biasing current, I_B. The (+) input couples only to the (−) input and then to extract from this (−) input terminal the same current (A_I, the mirror gain, is approximately equal to 1) which is entered (by the external circuitry) into the (+) input terminal. This operation is described as a ''current-mirror'' as the current entering the (+) input is ''mirrored'' or ''reflected'' about ground and is then extracted from the (−) input. There is a maximum or near saturation value of current which the ''mirror'' at the (+) input can handle. This is listed on the data sheet as ''maximum mirror current'' and ranges from approximately 6 mA at 25°C to 3.8 mA at 70°C.

This fact that the (+) input current modulates or affects the (−) input current causes this amplifier to pass currents between the input terminals and is the basis for many new application circuits—especially when operating with only a single power supply voltage.

The output is modeled as an active voltage source which also depends upon the open-loop voltage gain, A_V, but only the (−) input voltage, V^-, (not the differential input voltage). Finally, the output voltage of the LM3900 can swing from essentially ground (+90 mV) to within one V_{BE} of the power supply voltage.

As an example of the use of the equivalent circuit of the LM3900, the AC coupled inverting amplifier of *Figure 9a* will be analyzed. *Figure 9b* shows the complete equivalent circuit which, for convenience, can be separated into a biasing equivalent circuit (*Figure 10*) and an AC equivalent circuit (*Figure 11*). From the biasing model of *Figure 10* we find the output quiescent voltage, V_O, is:

$$V_O = V_D^- + (I_B + I^+)\,R_2, \tag{1}$$

and

$$I^+ = \frac{V^+ - V_D^+}{R_3} \tag{2}$$

where

$$V_D^+ \cong V_D^- \cong 0.5\,V_{DC}$$

I_B = INPUT bias current (30 nA)

and

V^+ = Power supply voltage.

If (2) is substituted into (1)

$$V_O = V_D^- + \left(I_B + \frac{V^+ - V_D^+}{R_3}\right) R_2 \tag{3}$$

which is an exact expression for V_O.

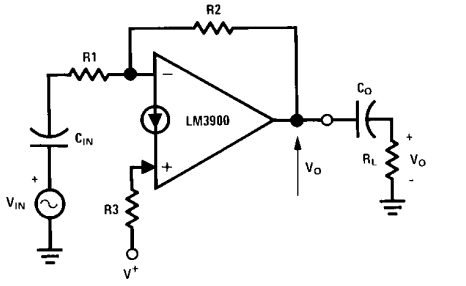
As the second term usually dominates ($V_O \gg V_D^-$) and $I^+ \gg I_B$ and $V^+ \gg V_D^+$ we can simplify (3) to provide a more useful design relationship

$$V_O \cong \frac{R_2}{R_3}\ V^+. \tag{4}$$

Using (4), if $R_3 = 2R_2$ we find

$$V_O \cong \frac{R_2}{2R_2} V^+ = \frac{V^+}{2}, \tag{5}$$

which shows that the output is easily biased to one-half of the power supply voltage by using V^+ as a biasing reference at the (+) input.



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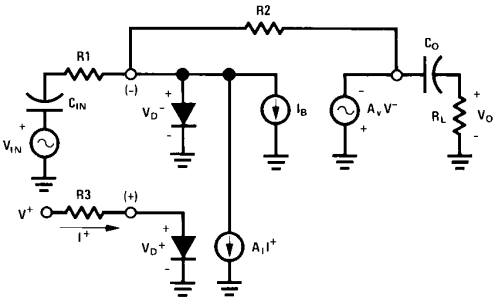
(a) A Typical Biased Amplifier



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(b) Using the LM3900 Equivalent Circuit

FIGURE 9. Applying the LM3900 Equivalent Circuit

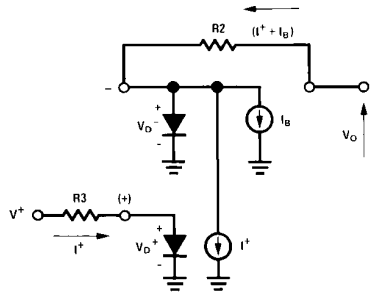

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FIGURE 10. Biasing Equivalent Circuit

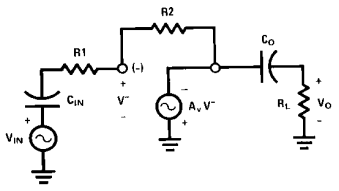

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FIGURE 11. AC Equivalent Circuit

The AC equivalent circuit of *Figure 11* is the same as that which would result if a standard IC op amp were used with the (+) input grounded. The closed-loop voltage gain A_{VCL}, is given by:

$$A_{VCL} \equiv \frac{V_O}{V_{IN}} \cong -\frac{R_2}{R_1} \quad (6)$$

if A_V (open-loop) $> \frac{R_2}{R_1}$.

The design procedure for an AC coupled inverting amplifier using the LM3900 is therefore to first select R_1, C_{IN}, R_2, and C_O as with a standard IC op amp and then to simply add $R_3 = 2R_2$ as a final biasing consideration. Other biasing techniques are presented in the following sections of this note. For the switching circuit applications, the biasing model of *Figure 10* is adequate to predict circuit operation.

Although the LM3900 has four independent amplifiers, the use of the label ''¼LM3900'' will be shortened to simply ''LM3900'' for the application drawings contained in this note.

3.0 Designing AC Amplifiers

The LM3900 readily lends itself to use as an AC amplifier because the output can be biased to any desired DC level within the range of the output voltage swing and the AC gain is independent of the biasing network. In addition, the single power supply requirement makes the LM3900 attractive for any low frequency gain application. For lowest noise performance, the (+) input should be grounded (*Figure 9a*) and the output will then bias at $+V_{BE}$. Although the LM3900 is not suitable as an ultra low noise tape pre-amp, it is useful in most other applications. The restriction to only shunt feedback causes a small input impedance. Transducers which can be loaded can operate with this low input impedance. The noise degradation which would result from the use of a large input resistor limits the usefulness where low noise and high input impedance are both required.

3.1 SINGLE POWER SUPPLY BIASING

The LM3900 can be biased in several different ways. The circuit in *Figure 12* is a standard inverting AC amplifier which has been biased from the same power supply which is used to operate the amplifier. (The design of this amplifier has been presented in the previous section). Notice that if AC ripple voltages are present on the V^+ power supply line they will couple to the output with a ''gain'' of ½. To eliminate this, one source of ripple filtered voltage can be provided and then used for many amplifiers. This is shown in the next section.

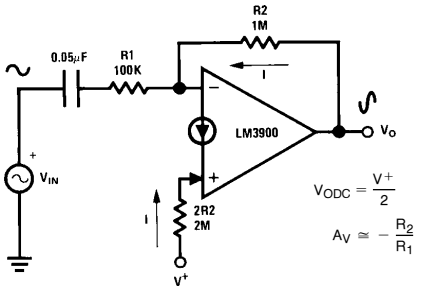

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FIGURE 12. Inverting AC Amplifier Using Single-Supply Biasing

3.2 A NON-INVERTING AMPLIFIER

The amplifier in *Figure 13* shows both a non-inverting AC amplifier and a second method for DC biasing. Once again the AC gain of the amplifier is set by the ratio of feedback resistor to input resistor. The small signal impedance of the diode at the (+) input should be added to the value of R_1 when calculating gain, as shown in *Figure 13*.

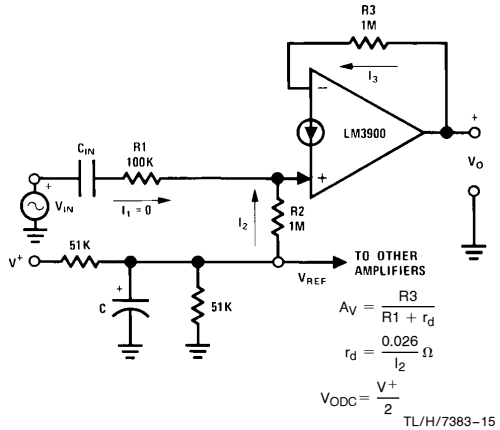

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FIGURE 13. Non-inverting AC Amplifier Using Voltage Reference Biasing

By making $R_2 = R_3$, V_{ODC} will be equal to the reference voltage which is applied to the resistor R_2. The filtered $V^+/2$ reference shown can also be used for other amplifiers.

3.3 ''N V_{BE}'' BIASING

A third technique of output DC biasing is best described as the ''N V_{BE}'' method. This technique is shown in *Figure 14* and is most useful with inverting AC amplifier applications.

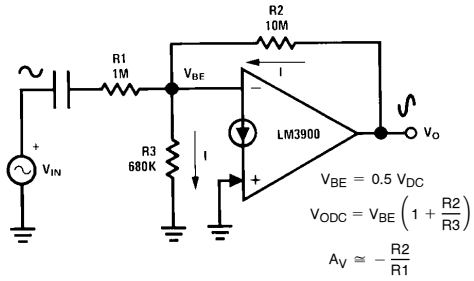

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FIGURE 14. Inverting AC Amplifier Using N V_{BE} Biasing

The input bias voltage (V_{BE}) at the inverting input establishes a current through resistor R_3 to ground. This current must come from the output of the amplifier. Therefore, V_O must rise to a level which will cause this current to flow through R_2. The bias voltage, V_O, may be calculated from the ratio of R_2 to R_3 as follows:

$$V_{ODC} = V_{BE}\left(1 + \frac{R_2}{R_3}\right)$$

When NV_{BE} biasing is employed, values for resistors R_1 and R_2 are first established and then resistor R_3 is added to provide the desired DC output voltage.

For a design example (*Figure 14*), a Z in = 1M and $A_v \cong 10$ are required.

Select $R_1 = 1M$.

Calculate $R_2 \cong A_v R_1 = 10M$.

To bias the output voltage at 7.5 V_{DC}, R_3 is found as:

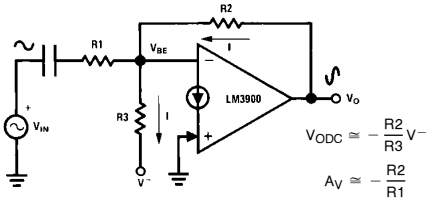
$$R_3 = \frac{R_2}{\frac{V_O}{V_{BE}} - 1} = \frac{10M}{\frac{7.5}{0.5} - 1}$$

or

$$R_3 \cong 680\ k\Omega.$$

3.4 BIASING USING A NEGATIVE SUPPLY

If a negative power supply is available, the circuit of *Figure 15* can be used. The DC biasing current, I, is established by the negative supply voltage via R_3 and provides a very stable output quiescent point for the amplifier.

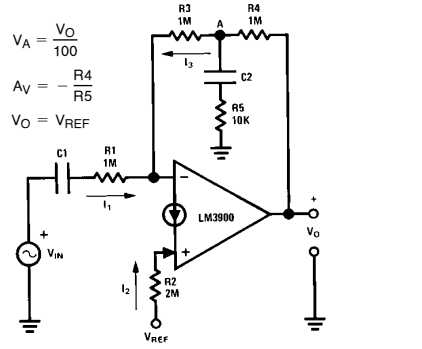


TL/H/7383–17

FIGURE 15. Negative Supply Biasing

3.5 OBTAINING HIGH INPUT IMPEDANCE AND HIGH GAIN

For the AC amplifiers which have been presented, a designer is able to obtain either high gain or high input impedance with very little difficulty. The application which requires both and still employs only one amplifier presents a new problem. This can be achieved by the use of a circuit similar to the one shown in *Figure 16*. When the A_V from the input to point A is unity ($R_1 = R_3$), the A_v of the complete stage will be set by the voltage divider network composed of R_4, R_5, and C_2. As the value of R_5 is decreased, the A_v of the stage will approach the AC open loop limit of the amplifier. The insertion of capacitor C_2 allows the DC bias to be controlled by the series combination of R_3 and R_4 with no effect from R_5. Therefore, R_2 may be selected to obtain the desired output DC biasing level using any of the methods which have been discussed. The circuit in *Figure 16* has an input impedance of 1M and a gain of 100.



TL/H/7383–18

FIGURE 16. A High Z_{IN} High Gain Inverting AC Amplifier

3.6 AN AMPLIFIER WITH A DC GAIN CONTROL

A DC gain control can be added to an amplifier as shown in *Figure 17*. The output of the amplifier is kept from being driven to saturation as the DC gain control is varied by providing a minimum biasing current via R_3. For maximum gain, CR_2 is OFF and both the current through R_2 and R_3 enter the (+) input and cause the output of the amplifier to bias at approximately 0.6 V^+. For minimum gain, CR_2 is ON and only the current through R_3 enters the (+) input to bias the output at approximately 0.3 V^+. The proper output bias for large output signal accommodation is provided for the maximum gain situation. The DC gain control input ranges from 0 V_{DC} for minimum gain to less than 10 V_{DC} for maximum gain.

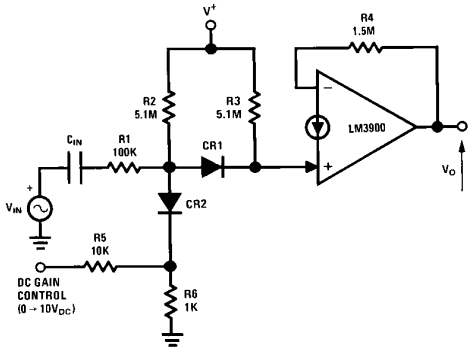


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FIGURE 17. An Amplifier with a DC Gain Control

3.7 A LINE-RECEIVER AMPLIFIER

The line-receiver amplifier is shown in *Figure 18*. The use of both inputs cancels out common-mode signals. The line is terminated by R_{LINE} and the larger input impedance of the amplifier will not affect this matched loading.

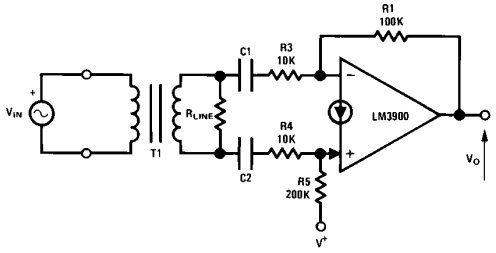

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FIGURE 18. A Line-receiver Amplifier

4.0 Designing DC Amplifiers

The design of DC amplifiers using the LM3900 tends to be more difficult than the design of AC amplifiers. These difficulties occur when designing a DC amplifier which will operate from only a single power supply voltage and yet provide an output voltage which goes to zero volts DC and also will accept input voltages of zero volts DC. To accomplish this, the inputs must be biased into the linear region ($+V_{BE}$) with DC input signals of zero volts and the output must be modified if operation to actual ground (and not V_{SAT}) is required. Therefore, the problem becomes one of determining what type of network is necessary to provide an output voltage (V_O) equal to zero when the input voltage (V_{IN}) is equal to zero. (See also section 10.15, ''adding a Differential Input Stage'').

We will start with a careful evaluation of what actually takes place at the amplifier inputs. The mirror circuit demands that the current flowing into the positive input ($+$) be equaled by a current flowing into the negative input ($-$). The difference between the current demanded and the current provided by an external source must flow in the feedback circuit. The output voltage is then forced to seek the level required to cause this amount of current to flow. If, in the steady state condition $V_O = V_{IN} = 0$, the amplifier will operate in the desired manner. This condition can be established by the use of common-mode biasing at the inputs.

4.1 USING COMMON-MODE BIASING FOR $V_{IN} = 0\ V_{DC}$

Common-mode biasing is achieved by placing equal resistors between the amplifier input terminals and the supply voltage (V^+), as shown in *Figure 19*. When V_{IN} is set to 0 volts the circuit can be modeled as shown in *Figure 20*,

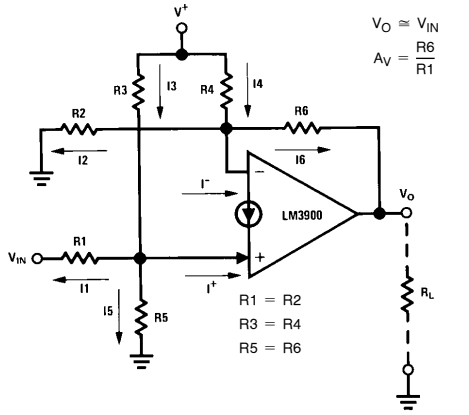

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FIGURE 19. A DC Amplifier Employing Common-mode Biasing

where:

$$R_{EQ_1} = R_1 \parallel R_5,$$

$$R_{EQ_2} = R_2 \parallel R_6,$$

and

$$R_3 = R_4.$$

Because the current mirror demands that the two current sources be equal, the current in the two equivalent resistors must be identical.

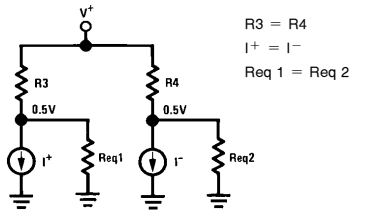

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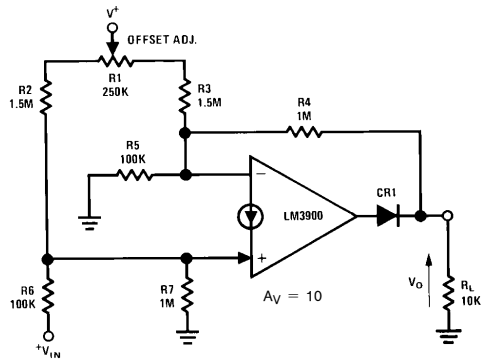
FIGURE 20. An Ideal Circuit Model of a DC Amplifier with Zero Input Voltage

If this is true, both R_2 and R_6 must have a voltage drop of 0.5 volt across them, which forces V_O to go to $V_{O\ MIN}$ (V_{SAT}).

4.2 ADDING AN OUTPUT DIODE FOR $V_O = 0\ V_{DC}$

For many applications a $V_{O\ MIN}$ Of 100 mV may not be acceptable. To overcome this problem a diode can be added between the output of the amplifier and the output terminal (*Figure 21*).



TL/H/7383–23

FIGURE 21. A Non-inverting DC Amplifier with Zero Volts Output for Zero Volts Input

The function of the diode is to provide a DC level shift which will allow V_O to go to ground. With a load impedance (R_L) connected, V_O becomes a function of the voltage divider formed by the series connection of R_4 and R_L.

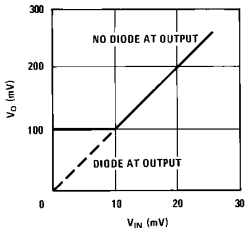
If $R_4 = 100\ R_L$, then $V_{O\ MIN} = \dfrac{0.5\ R_L}{101\ R_L}$,

or $V_{O\ MIN} \cong 5\ mV_{DC}$.

An offset voltage adjustment can be added as shown (R_1) to adjust V_O to $0V_{DC}$ with $V_{IN} = 0\ V_{DC}$.

The voltage transfer functions for the circuit in *Figure 21*, both with and without the diode, are shown in *Figure 22*. While the diode greatly improves the operation around 0 volts, the voltage drop across the diode will reduce the peak output voltage swing of the state by approximately 0.5 volt.

When using a DC amplifier similar to the one in *Figure 21*, the load impedance should be large enough to avoid excessively loading the amplifier. The value of R_L may be significantly reduced by replacing the diode with an NPN transistor.



TL/H/7383–24

FIGURE 22. Voltage Transfer Function for a DC Amplifier with a Voltage Gain of 10

4.3 A DC COUPLED POWER AMPLIFIER ($I_L \leq 3$ AMPS)

The LM3900 may be used as a power amplifier by the addition of a Darlington pair at the output. The circuit shown in *Figure 23* can deliver in excess of 3 amps to the load when the transistors are properly mounted on heat sinks.

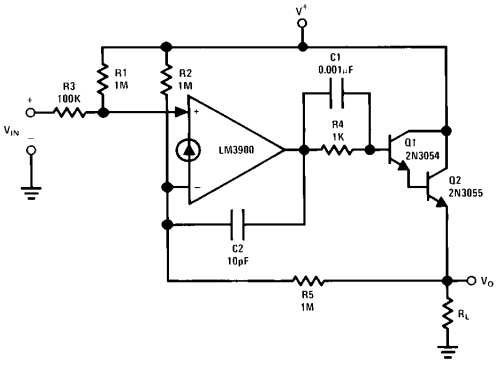


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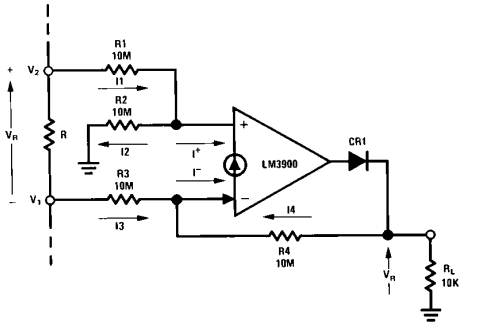
FIGURE 23. A DC Power Amplifier

4.4 GROUND REFERENCING A DIFFERENTIAL VOLTAGE

The circuit in *Figure 24* employs the LM3900 to ground reference a DC differential input voltage. Current I_1 is larger



TL/H/7383–26

FIGURE 24. Ground Referencing a Differential Input DC Voltage

than current I_3 by a factor proportional to the differential voltage, V_R. The currents labeled on *Figure 24* are given by:

$$I_1 = \frac{V_1 + V_R - \phi}{R_1}$$

$$I_2 = \phi/R_2$$

$$I_3 = \frac{(V_1 - \phi)}{R_3}$$

and

$$I_4 = \frac{V_O - \phi}{R_4}$$

where

$\phi \equiv V_{BE}$ at either input terminal of the LM3900.

Since the input current mirror demands that

$$I^- = I^+;$$

and

$$I^+ = I_1 - I_2$$

and

$$I^- = I_3 + I_4$$

Therefore

$$I_4 = I_1 - I_2 - I_3.$$

Substituting in from the above equation

$$\frac{V_O - \phi}{R_4} = \frac{(V_1 + V_R - \phi)}{R_1} - \frac{(\phi)}{R_2} - \frac{(V_1 - \phi)}{R_3}$$

and as $R_1 = R_2 = R_3 = R_4$

$$V_O = (V_1 + V_R - \phi) - (\phi) - V_1 + \phi + \phi$$

or

$$V_O = V_R.$$

The resistors are kept large to minimize loading. With the 10 MΩ resistors which are shown on the figure, an error exists at small values of V_1 due to the input bias current at the (–) input. For simplicity this has been neglected in the circuit description. Smaller R values reduce the percentage error or the bias current can be supplied by an additional amplifier (see Section 10.7.1).

For proper operation, the differential input voltage must be limited to be within the output dynamic voltage range of the amplifier and the input voltage V_2 must be greater than 1 volt. For example; if $V_2 = 1$ volt, the input voltage V_1 may vary over the range of 1 volt to −13 volts when operating from a 15 volt supply. Common-mode biasing may be added as shown in *Figure 25* to allow both V_1 and V_2 to be negative.

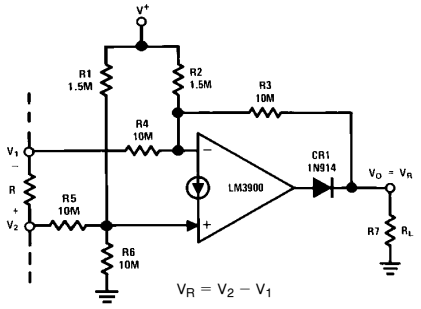


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FIGURE 25. A Network to Invert and to Ground Reference a Negative DC Differential Input Voltage

4.5 A UNITY GAIN BUFFER AMPLIFIER

The buffer amplifier with a gain of one is the simplest DC application for the LM3900. The voltage applied to the input (*Figure 26*) will be reproduced at the output. However, the input voltage must be greater than one V_{BE} but less than the maximum output swing. Common-mode biasing can be added to extend V_{IN} to 0 V_{DC}, if desired.

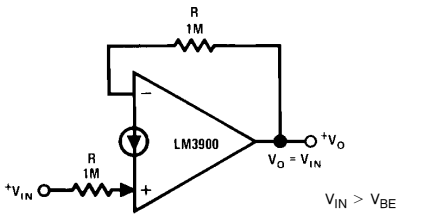

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FIGURE 26. A Unity-gain DC Buffer Amplifier

5.0 Designing Voltage Regulators

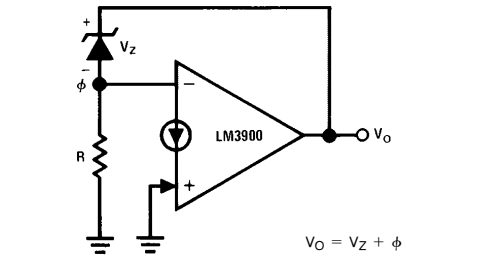
Many voltage regulators can be designed which make use of the basic amplifier of the LM3900. The simplest is shown in *Figure 27a* where only a Zener diode and a resistor are added. The voltage at the (–) input (one $V_{BE} \cong 0.5\ V_{DC}$) appears across R and therefore a resistor value of 510Ω will cause approximately 1 mA of bias current to be drawn through the Zener. This biasing is used to reduce the noise output of the Zener as the 30 nA input current is too small for proper Zener biasing. To compensate for a positive temperature coefficient of the Zener, an additional resistor can be added, R_2, (*Figure 27b*) to introduce an arbitrary number, N, of "effective" V_{BE} drops into the expression for the output voltage. The negative temperature coefficient of these diodes will also be added to temperature compensate the DC output voltage. For a larger output current, an emitter follower (Q_1 of *Figure 27c*) can be added. This will multiply the 10 mA (max.) output current of the LM3900 by the β of the added transistor. For example, a $\beta = 30$ will provide a max. load current of 300 mA. This added transistor also reduces the output impedance. An output frequency compensation capacitor is generally not required but may be added, if desired, to reduce the output impedance at high frequencies.

The DC output voltage can be increased and still preserve the temperature compensation of *Figure 27b* by adding resistors R_A and R_B as shown in *Figure 27d*. This also can be accomplished without the added transistor, Q_1. The unregulated input voltage, which is applied to pin 14 of the LM3900 (and to the collector of Q_1, if used) must always exceed the regulated DC output voltage by approximately 1V, when the unit is not current boosted or approximately 2V when the NPN current boosting transistor is added.

5.1 REDUCING THE INPUT-OUTPUT VOLTAGE

The use of an external PNP transistor will reduce the required ($V_{IN} - V_{OUT}$) to a few tenths of a volt. This will depend on the saturation characteristics of the external transistor at the operating current level. The circuit, shown in *Figure 28*, uses the LM3900 to supply base drive to the PNP transistor. The resistors R_1 and R_2 are used to allow the output of the amplifier to turn OFF the PNP transistor. It is important that pin 14 of the LM3900 be tied to the $+V_{IN}$ line to allow this OFF control to properly operate. Larger voltages are permissible (if the base-emitter junction of Q_1 is prevented from entering a breakdown by a shunting diode, for example), but smaller voltages will not allow the output of the amplifier to raise enough to give the OFF control.

The resistor, R_3, is used to supply the required bias current for the amplifier and R_4 is again used to bias the Zener diode. Due to a larger gain, a compensation capacitor, C_O, is required. Temperature compensation could be added as was shown in *Figure 27b*.



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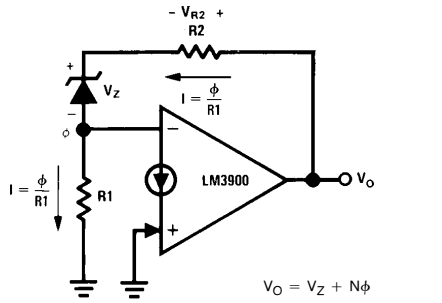
(a) Basic Current



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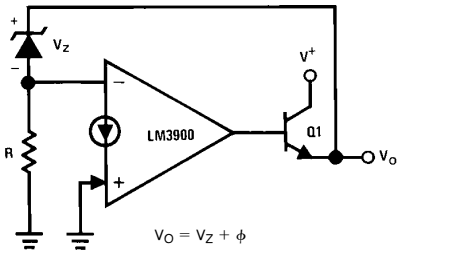
(b) Temperature Compensating



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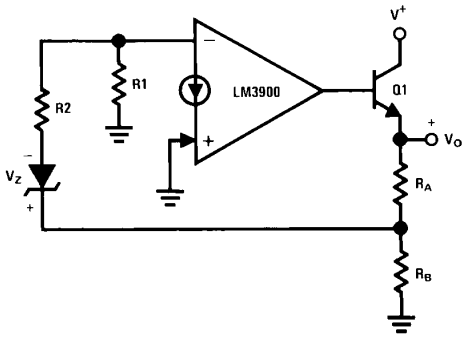
(c) Current Boosting



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(d) Raising V_O Without Disturbing Temperature Compensation

FIGURE 27. Simple Voltage Regulators

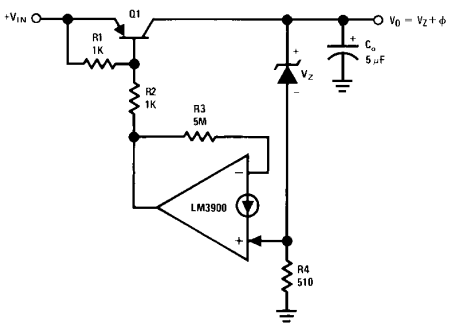

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FIGURE 28. Reducing ($V_{IN} - V_{OUT}$)

5.2 PROVIDING HIGH INPUT VOLTAGE PROTECTION

One of the four amplifiers can be used to regulate the supply line for the complete package (pin 14), to provide protection against large input voltage conditions, and in addition, to supply current to an external load. This circuit is shown in *Figure 29*. The regulated output voltage is the sum of the Zener voltage, CR_2, and the V_{BE} of the inverting input terminal. Again, temperature compensation can be added as in *Figure 27b*. The second Zener, CR_1, is a low tolerance component which simply serves as a DC level shift to allow the output voltage of the amplifier to control the conduction of the external transistor, Q_1. This Zener voltage should be approximately one-half of the CR_2 voltage to position the DC Output voltage level of the amplifier approximately in the center of the dynamic range.

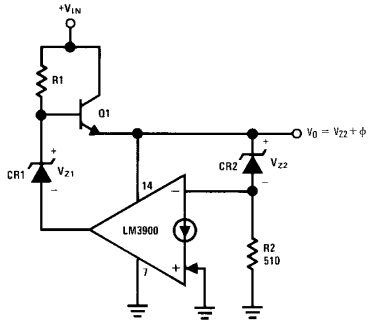

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FIGURE 29. High V_{IN} Protection and Self-regulation

The base drive current for Q_1 is supplied via R_1. The maximum current through R_1 should be limited to 10 mA as

$$I_{MAX} = \frac{V_{IN\ (MAX)} - (V_O + V_{BE})}{R_1}$$

To increase the maximum allowed input voltage, reduce the output ripple, or to reduce the ($V_{IN} - V_{OUT}$) requirements of this circuit, the connection described in the next section is recommended.

5.3 HIGH INPUT VOLTAGE PROTECTION AND LOW ($V_{IN} - V_{OUT}$)

The circuit shown in *Figure 30* basically adds one additional transistor to the circuit of *Figure 29* to improve the performance. In this circuit both transistors (Q_1 and Q_2) absorb any high input voltages (and therefore need to be high voltage devices) without any increases in current (as with R_1 of *Figure 29*). The resistor R_1 (of *Figure 30*) provides a "start-up" current into the base of Q_2.

A new input connection is shown on this regulator (the type on *Figure 29* could also be used) to control the DC output voltage. The Zener is biased via R_4 (at approximately 1 mA). The resistors R_3 and R_6 provide gain (non-inverting) to allow establishing V_O at any desired voltage larger than V_Z. Temperature compensation of either sign (±TC) can be obtained by shunting a resistor from either the (+) input to ground (to add + TC to V_O) or from the (−) input to ground (to add −TC to V_O). To understand this, notice that the resistor, R, from the (+) input to ground will add $-N\ V_{BE}$ to V_O where

$$N = 1 + \frac{R_3}{R},$$

and V_{BE} is the base emitter voltage of the transistor at the (+) input. This then also adds a positive temperature change at the output to provide the desired temperature correction.

The added transistor, Q_2, also increases the gain (which reduces the output impedance) and if a power device is used for Q_1 large load currents (amps) can be supplied. This regulator also supplies the power to the other three amplifiers of the LM3900.

5.4 REDUCING INPUT VOLTAGE DEPENDENCE AND ADDING SHORT-CIRCUIT PROTECTION

To reduce ripple feedthrough and input voltage dependence, diodes can be added as shown in *Figure 31* to drop-out the start once start-up has been achieved. Short-circuit protection can also be added as shown in *Figure 32*.

The emitter resistor of Q_2 will limit the maximum current of Q_2 to $(V_O - 2\ V_{BE})/R_5$.

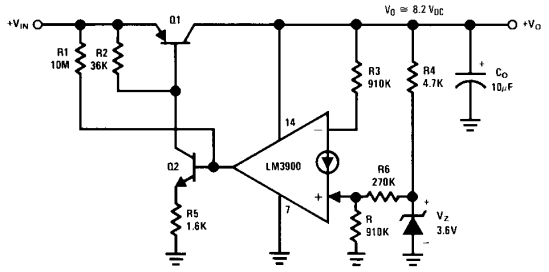

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FIGURE 30. A High V_{IN} Protected, Low ($V_{IN} - V_{OUT}$) Regulator

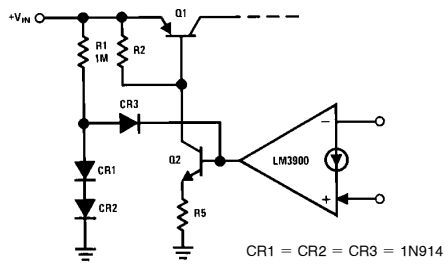

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FIGURE 31. Reducing V_{IN} Dependence

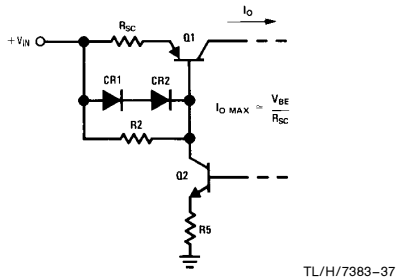

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FIGURE 32. Adding Short-circuit Current Limiting

6.0 Designing RC Active Filters

Recent work in RC active filters has shown that the performance characteristics of multiple-amplifier filters are relatively insensitive to the tolerance of the RC components used. This makes the performance of these filters easier to control in production runs. In many cases where gain is needed in a system design it is now relatively easy to also get frequency selectivity.

The basis of active filters is a gain stage and therefore a multiple amplifier product is a valuable addition to this application area. When additional amplifiers are available, less component selection and trimming is needed as the performance of the filter is less disturbed by the tolerance and temperature drifts of the passive components.

The *passive components* do *control* the *performance* of the filter and for this reason carbon composition resistors are useful mainly for room temperature breadboarding or for final trimming of the more stable metal film or wire-wound resistors. Capacitors present more of a problem in range of values available, tolerance and stability (with temperature, frequency, voltage and time). For example, the disk ceramic type of capacitors are generally not suited to active filter applications due to their relatively poor performance.

The impedance level of the passive components can be scaled without (theoretically) affecting the filter characteristics. In an actual circuit; if the resistor values become too small ($\leq$10 kΩ) an excessive loading may be placed on the output of the amplifier which will reduce gain or actually exceed either the output current or the package dissipation capabilities of the amplifier. This can easily be checked by calculating (or noticing) the impedance which is presented to the output terminal of the amplifier at the highest operating frequency. A second limit sets the upper range of impedance levels, this is due to the DC bias currents ($\cong$30 nA) and the input impedance of actual amplifiers. The solution to this problem is to reduce the impedance levels of the passive components ($\leq$10 MΩ). In general, better performance is obtained with relatively low passive component impedance levels and in filters which do not demand high gain, high Q (Q $\geq$ 50) and high frequency (f_o > 1 kHz) simultaneously.

A measure of the effects of changes in the values of the passive components on the filter performance has been given by ''sensitivity functions''. These assume infinite amplifier gain and relate the percentage change in a parameter of the filter, such as center frequency (f_o), Q, or gain to a percentage change in a particular passive component. Sensitivity functions which are small are desirable (as 1 or ½).

Negative signs simply mean an increase in the value of a passive component causes a decrease in that filter performance characteristic. As an example, if a bandpass filter listed the following sensitivity factor

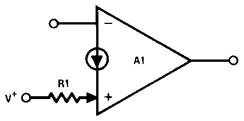
$$S^{\omega_o}_{C_3} = -½.$$

This states that ''if C_3 were to increase by 1%, the center frequency, ω_o, would decrease by 0.5%.'' Sensitivity functions are tabulated in the reference listed at the end of this section and will therefore not be included here.

A brief look at low pass, high pass and bandpass filters will indicate how the LM3900 can be applied in these areas. A recommended text (which provided these circuits) is, ''Operational Amplifiers'', Tobey, Graeme, and Huelsman, McGraw Hill, 1971.

6.1 BIASING THE AMPLIFIERS

Active filters can be easily operated off of a single power supply when using these multiple single supply amplifiers. The general technique is to use the (+) input to accomplish the biasing function. The power supply voltage, V^+, is used as the DC reference to bias the output voltage of each amplifier at approximately $V^+/2$. As shown in *Figure 33*, undesired AC components on the power supply line may have to



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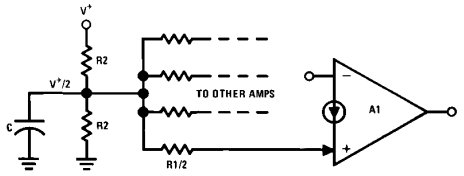
(a) Biasing From a ''Noise-Free'' Power Supply



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(b) Biasing From a ''Noisy'' Power Supply

FIGURE 33. Biasing Considerations

be removed (by a filter capacitor, *Figure 33b*) to keep the filter output free of this noise. One filtered DC reference can generally be used for all of the amplifiers as there is essentially no signal feedback to this bias point.

In the filter circuits presented here, all amplifiers will be biased at $V^+/2$ to allow the maximum AC voltage swing for any given DC power supply voltage. The inputs to these filters will also be assumed at a DC level of $V^+/2$ (for those which are direct coupled).

6.2 A HIGH PASS ACTIVE FILTER

A single amplifier high pass RC active filter is shown in *Figure 34*. This circuit is easily biased using the (+) input of the LM3900. The resistor, R_3, can be simply made equal to R_2 and a bias reference of $V^+/2$ will establish the output Q point at this value ($V^+/2$). The input is capacitively coupled (C_1) and there are therefore no further DC biasing problems.

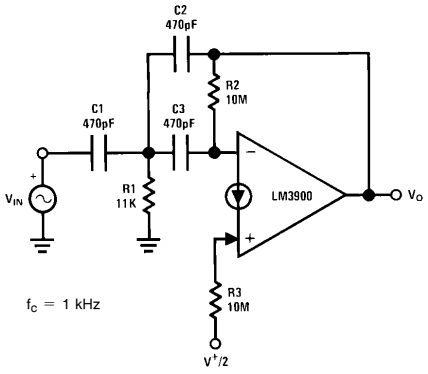

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FIGURE 34. A High Pass Active Filter

The design procedure for this filter is to select the pass band gain, H_O, the Q and the corner frequency, f_c. A Q value of 1 gives only a slight peaking near the bandedge (<2 dB) and smaller Q values decrease this peaking. The slope of the skirt of this filter is 12 dB/octave (or 40 dB/decade). If the gain, H_O, is unity all capacitors have the same value. The design proceeds as:

Given: H_O, Q and $\omega_c = 2\pi f_c$

To find: R_1, R_2, C_1, C_2, and C_3

let $C_1 = C_3$ and choose a convenient starting value.

Then:

$$R_1 = \frac{1}{Q\,\omega_c C_1\,(2H_O + 1)} \quad (1)$$

$$R_2 = \frac{Q}{\omega_c C_1}(2\,H_O + 1), \quad (2)$$

and

$$C_2 = \frac{C_1}{H_O}. \quad (3)$$

As a design example,

Require: $H_O = 1$,

$Q = 10$,

and $f_c = 1$ kHz ($\omega_c = 6.28 \times 10^3$ rps).

Start by selecting $C_1 = 300$ pF and then from equation (1)

$$R_1 = \frac{1}{(10)\,(6.28 \times 10^3)\,(3 \times 10^{-10})\,(3)}$$

$R_1 = 17.7\ \text{k}\Omega$

and from equation (2)

$$R_2 = \frac{10 \qquad (3)}{(6.28 \times 10^3)\,(3 \times 10^{-10})}$$

$R_2 = 15.9\ \text{M}\Omega$

and from equation (3)

$$C_2 = \frac{C_1}{1} = C_1$$

Now we see that the value of R_2 is quite large; but the other components look acceptable. Here is where impedance scaling comes in. We can reduce R_2 to the more convenient value of 10 MΩ which is a factor of 1.59:1. Reducing R_1 by this same scaling factor gives:

$$R_{1_{NEW}} = \frac{17.7 \times 10^3}{1.59} = 11.1\ \text{k}\Omega$$

and the capacitors are similarly reduced in impedance as:

$$\left(C_1 = C_2 = C_3\right)_{NEW} = (1.59)\,(300)\ \text{pF}$$

$$C_{1_{NEW}} = 477\ \text{pF}.$$

To complete the design, R_3 is made equal to R_2 (10 MΩ) and a V_{REF} of $V^+/2$ is used to bias the output for large signal accommodation.

Capacitor values should be adjusted to use standard valued components by using impedance scaling as a wider range of standard resistor values is generally available.

6.3 A LOW PASS ACTIVE FILTER

A single amplifier low pass filter is shown in *Figure 35*. The resistor, R_4, is used to set the output bias level and is selected after the other resistors have been established.

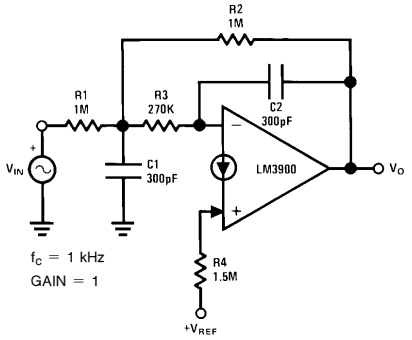

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FIGURE 35. A Low Pass Active Filter

The design procedure is as follows:

Given: H_O, Q, and $\omega_c = 2\pi f_c$

To find: R_1, R_2, R_3, R_4, C_1, and C_2

Let C_1 be a convenient value,

then

$$C_2 = KC_1 \quad (4)$$

where K is a constant which can be used to adjust component values. For example, with $K = 1$, $C_1 = C_2$. Larger values of K can be used to reduce R_2 and R_3 at the expense of a larger value for C_2.

$$R_1 = \frac{R_2}{H_O}, \quad (5)$$

$$R_2 = \frac{1}{2Q\,\omega_C\,C_1}\left[1 \pm \sqrt{1 + \frac{4Q^2\,(H_O + 1)}{K}}\,\right] \quad (6)$$

and

$$R_3 = \frac{1}{\omega_c^2 C_1^2 R_2(K)} \quad (7)$$

As a design example:

Require: $H_O = 1$,

$Q = 1$,

and $f_c = 1$ kHz ($\omega_c = 6.28 \times 10^3$ rps).

Start by selecting $C_1 = 300$ pF and $K = 1$ so C_2 is also 300 pF (equation 4).

Now from equation (6)

$$R_2 = \frac{1}{2\,(1)\,(6.28 \times 10^3)\,(3 \times 10^{-10})}\left[1 \pm \sqrt{1 + 4\,(2)}\right]$$

$R_2 = 1.06\ \text{M}\Omega$

Then from equation (5)

$$R_1 = R_2 = 1.06\ \text{M}\Omega$$

and finally from equation (7)

$$R_3 = \frac{1}{(6.28 \times 10^3)^2\,(3 \times 10^{-10})^2\,(1.06 \times 10^6)\,(1)}$$

$R_3 = 266\ \text{k}\Omega$.

To select R_4, we assume the DC input level is 7 V_{DC} and the DC output of this filter is to also be 7 V_{DC}. This gives us the circuit of *Figure 36*. Notice that $H_O = 1$ gives us not only

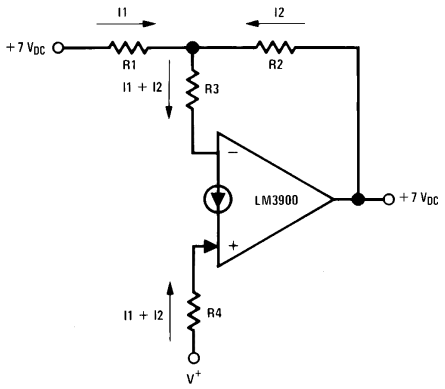

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FIGURE 36. Biasing the Low Pass Filter

equal resistor values (R_1 and R_2) but simplifies the DC bias calculation as $I_1 = I_2$ and we have a DC amplifier with a gain of -1 (so if the DC input voltage increases 1 V_{DC} the output voltage decreases 1 V_{DC}). The resistors R_1 and R_2 are in parallel so that the circuit simplifies to that shown in *Figure 37* where the actual resistance values have been added. The resistor R_4 is given by

$$R_4 = 2\left(\frac{R_1}{2} + R_3\right) + R_3$$

or, using values

$$R_4 = 2\left(\frac{1\ \text{M}\Omega}{2} + 266\text{k}\right) \cong 1.5\ \text{M}\Omega$$

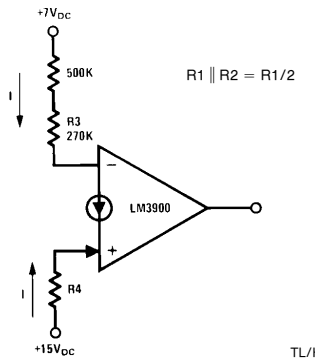

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FIGURE 37. Biasing Equivalent Circuit

6.4 A SINGLE-AMPLIFIER BANDPASS ACTIVE FILTER

The bandpass filter is perhaps the most interesting. For low frequencies, low gain and low Q (≤ 10) requirements, a single amplifier realization can be used. A one amplifier circuit is shown in *Figure 38* and the design procedure is as follows;

Given: H_O, Q and $\omega_o = 2\pi f$.

To find: R_1, R_2, R_3, R_4, C_1 and C_2.

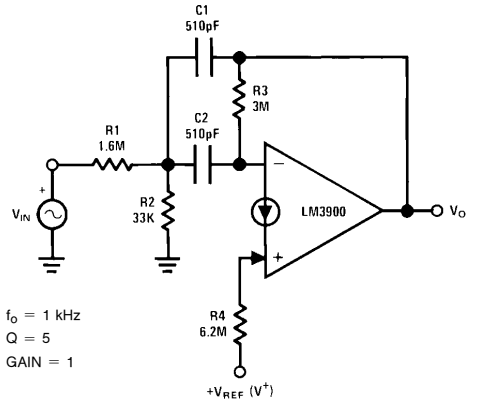

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FIGURE 38. A One Op Amp Bandpass Filter

Let $C_1 = C_2$ and select a convenient starting value.

Then

$$R_1 = \frac{Q}{H_O \omega_o C_1} \tag{8}$$

$$R_2 = \frac{Q}{(2\,Q^2 - H_O)\,\omega_o\,C_1} \tag{9}$$

$$R_3 = \frac{2Q}{\omega_o C_1} \tag{10}$$

and

$$R_4 = 2R_3\ (\text{for } V_{REF} = V^+) \tag{11}$$

As a design example:

Require: $H_O = 1$

$Q = 5$

$f_o = 1$ kHz ($\omega_o = 6.28 \times 10^3$ rps).

Start by selecting

$C_1 = C_2 = 510$ pF.

Then using equation (8)

$$R_1 = \frac{5}{(6.28 \times 10^3)\,(5.1 \times 10^{-10})}$$

$R_1 = 1.57\ \text{M}\Omega$,

and using equation (9)

$$R_2 = \frac{5}{[2(25) - 1]\,(6.28 \times 10^3)\,(5.1 \times 10^{-10})}$$

$R_2 = 32\ \text{k}\Omega$

from equation (10)

$$R_3 = \frac{2(5)}{(6.28 \times 10^3)\,(5.1 \times 10^{-10})}$$

$R_3 = 3.13\ \text{M}\Omega$,

and finally, for biasing, using equation (11)

$R_4 = 6.2\ \text{M}\Omega$.

6.5 A TWO-AMPLIFIER BANDPASS ACTIVE FILTER

To allow higher Q (between 10 and 50) and higher gain, a two amplifier filter is required. This circuit, shown in *Figure 39*, uses only two capacitors. It is similar to the previous single amplifier bandpass circuit and the added amplifier supplies a controlled amount of positive feedback to improve the response characteristics. The resistors R_5 and R_8 are used to bias the output voltage of the amplifiers at $V^+/2$.

Again, R_5 is simply chosen as twice R_4 and R_8 must be selected after R_6 and R_7 have been assigned values. The design procedure is as follows:

Given: Q and f_o

To find: R_1 through R_7, and C_1 and C_2

Let: $C_1 = C_2$ and choose a convenient starting value and choose a value for K to reduce the spread of element values or to optimize sensitivity ($1 \leq K_{Typically} \leq 10$).

Then

$$R_1 = R_4 = R_6 = \frac{Q}{\omega_o C_1} \tag{12}$$

$$R_2 = R_1 \frac{KQ}{(2Q - 1)} \tag{13}$$

$$R_3 = \frac{R_1}{Q^2 - 1 - 2/K + 1/KQ} \tag{14}$$

and

$$R_7 = KR_1 \tag{15}$$

$$H_O = \sqrt{Q}\,K. \tag{16}$$

As a design example:

Require: $Q = 25$ and $f_o = 1$ kHz.

Select: $C_1 = C_2 = 0.1\ \mu F$

and $K = 3$.

Then from equation (12)

$$R_1 = R_4 = R_6 = \frac{25}{(2\pi \times 10^3)(10^{-7})}$$

$$R_1 = 40\ k\Omega$$

and from equation (13)

$$R_2 = (40 \times 10^3)\frac{3(25)}{[2(25) - 1]}$$

$$R_2 = 61\ k\Omega$$

and from equation (14)

$$R_3 = \frac{40 \times 10^3}{(25)^2 - 1 - 2/3 + \dfrac{1}{3(25)}}$$

$$R_3 = 64\Omega$$

And R_7 is given by equation (15)

$$R_7 = 3\,(40\ k\Omega) = 120\ k\Omega,$$

and the gain is obtained from equation (16)

$$H_O = \sqrt{25}\,(3) = 15\ (23\ dB).$$

To properly bias the first amplifier

$$R_5 = 2R_4 = 80\ k\Omega$$

and the second amplifier is biased by R_8. Notice that the outputs of both amplifiers will be at $V^+/2$. Therefore R_6 and R_7 can be paralleled and

$$R_8 = 2(R_6 \parallel R_7)$$

or

$$R_8 = 2\left[\frac{(40)\,(120) \times 10^3}{160}\right] = 59\ k\Omega$$

These values, to the closest standard resistor values, have been added to *Figure 39*.

6.6 A THREE-AMPLIFIER BANDPASS ACTIVE FILTER

To reduce Q sensitivity to element variation even further or to provide higher Q ($Q > 50$) a three amplifier bandpass filter can be used. This circuit, *Figure 40*, pre-dates most of the literature on RC active filters and has been used on analog computers. Due to the use of three amplifiers it often is considered too costly—especially for low Q applications. The multiple amplifiers of the LM3900 make this a very useful circuit. It has been called the ''Bi-Quad'' as it can produce a transfer function which is ''Quad''–ratic in both numerator and denominator (to give the ''Bi''). A newer real-

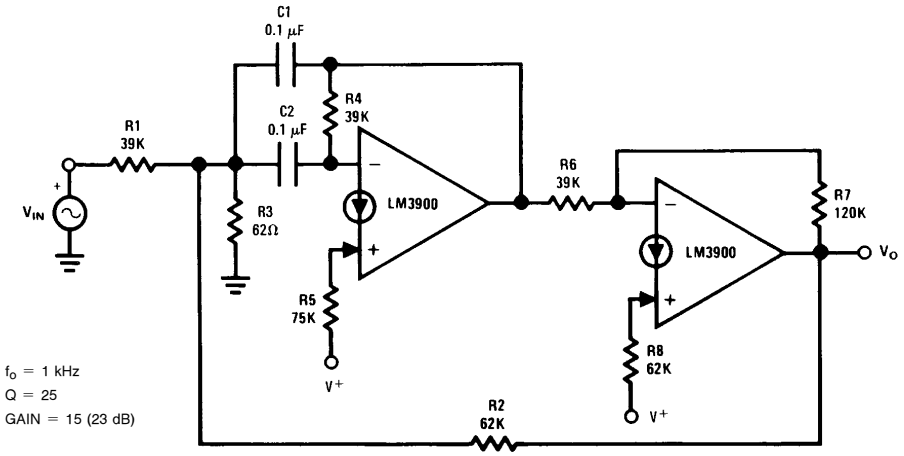

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FIGURE 39. A Two Op Amp Bandpass Filter

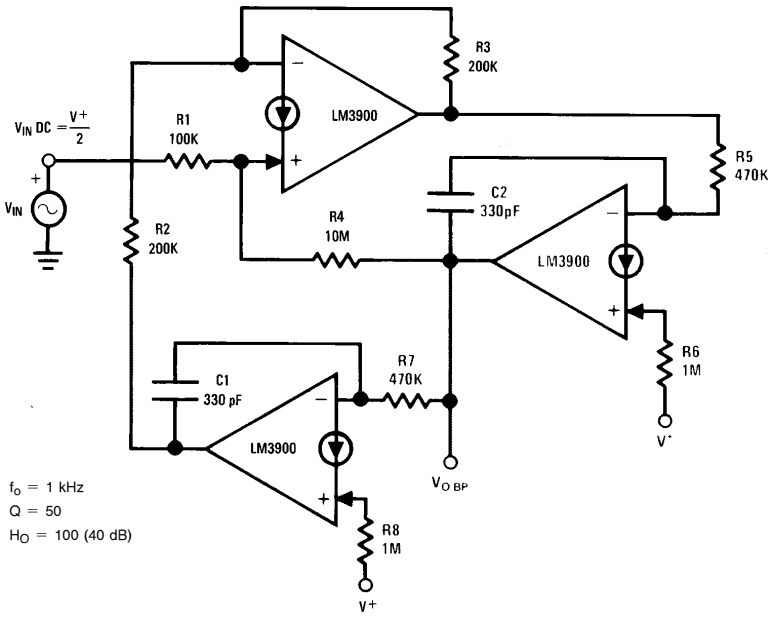

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FIGURE 40. The "Bi-quad" RC Active Bandpass Filter

ization technique for this type of filter is the "second-degree state-variable network." Outputs can be taken at any of three points to give low pass, high pass or bandpass response characteristics (see the reference cited).

The bandpass filter is shown in *Figure 40* and the design procedure is:

Given: Q and f_o.

To simplify: Let $C_1 = C_2$ and choose a convenient starting value and also let $2R_1 = R_2 = R_3$ and choose a convenient starting value.

Then:

$$R_4 = R_1 (2Q - 1), \quad (17)$$

$$R_5 = R_7 = \frac{1}{\omega_o C_1}, \quad (18)$$

and for biasing the amplifiers we require

$$R_6 = R_8 = 2R_5. \quad (19)$$

The mid-band gain is:

$$H_O = \frac{R_4}{R_1}. \quad (20)$$

As a design example;

Require: $f_o = 1$ kHz and $Q = 50$.

To find: C_1, C_2 and R_1 through R_8.

Choose: $C_1 = C_2 = 330$ pF

and $2R_1 = R_2 = R_3 = 360\ k\Omega$, and $R_1 = 180\ k\Omega$.

Then from equation (17),

$$R_4 = (1.8 \times 10^5)\,[2(50) - 1]$$

$$R_4 = 17.8\ M\Omega$$

From equation (18),

$$R_5 = R_7 = \frac{1}{(2\pi \times 10^3)\,(3.3 \times 10^{-10})}$$

$$R_5 = 483\ k\Omega.$$

And from equation (19),

$$R_6 = R_8 \cong 1\ M\Omega.$$

From equation (20) the midband gain is 100 (40 dB). The value of R_4 is high and can be lowered by scaling only R_1 through R_4 by the factor 1.78 to give:

$$2R_1 = R_2 = R_3 = \frac{360 \times 10^3}{1.78} = 200\ k\Omega,\ R_1 = 100\ k\Omega.$$

and

$$R_4 = \frac{17.8 \times 10^6}{1.78} = 10\ M\Omega.$$

These values (to the nearest 5% standard) have been added to *Figure 40*.

6.7 CONCLUSIONS

The unity-gain cross frequency of the LM3900 is 2.5 MHz which is approximately three times that of a "741" op amp. The performance of the amplifier does limit the performance of the filter. Historically, RC active filters started with little

concern for these practical problems. The sensitivity functions were a big step forward as these demonstrated that many of the earlier suggested realization techniques for RC active filters had passive component sensitivity functions which varied as Q or even Q^2. The Bi-Quad circuit has reduced the problems with the passive components (sensitivity functions of 1 or ½) and recently the contributions of the amplifier on the performance of the filter are being investigated. An excellent treatment (''The Biquad: Part I — Some Practical Design Considerations,'' L.C. Thomas, IEEE Transactions on Circuit Theory, Vol. CT-18, No. 3, May 1971) has indicated the limits imposed by the characteristics of the amplifier by showing that the design value of Q (Q_D) will differ from the actual measured value of Q (Q_A) by the given relationship

$$Q_A = \frac{Q_D}{1 + \frac{2Q_D}{A_O\omega_a}(\omega_a - 2\omega_p)} \qquad (21)$$

where A_O is the open loop gain of the amplifier, ω_a is the dominant pole of the amplifier and ω_p is the resonant frequency of the filter. The result is that the trade-off between Q and center frequency (ω_p) can be determined for a given set of amplifier characteristics. When Q_A differs significantly from Q_D excessive dependence on amplifier characteristics is indicated. An estimate of the limitations of an amplifier can be made by arbitrarily allowing approximately a 10% effect on Q_A which results if

$$\frac{2Q_D}{A_O\omega_a}(\omega_a - 2\omega_p) = 0.1$$

or

$$\left(\frac{\omega_p}{\omega_a}\right) = 2.5 \times 10^{-2}\left(\frac{A_O}{Q_D}\right) + 0.5. \qquad (22)$$

As an example, using $A_O = 2800$ for the LM3900 we can estimate the maximum frequency where a $Q_D = 50$ would be reasonable as

$$\frac{f_p}{f_a} = 2.5 \times 10^{-2}\left(\frac{2.8 \times 10^3}{5 \times 10}\right) + 0.5$$

or

$$\frac{f_p}{f_a} = 1.9$$

therefore

$$f_p = 1.9\, f_a.$$

Again, using data of the LM3900, $f_a = 1$ kHz so this upper frequency limit is approximately 2 kHz for the assumed Q of 50. As indicated in equation (26) the value of Q_A can actually exceed the value of Q_D (Q enhancement) and, as expected, the filter can even provide its own input (oscillating). Excess phase shift in the high frequency characteristics of the amplifier typically cause unexpected oscillations. Phase compensation can be used in the Bi-Quad network to reduce this problem (see L.C. Thomas paper).

Designing for large passband gain also increases filter dependency on the characteristics of the amplifier and finally signal to noise ratio can usually be improved by taking gain in an input RC active filter (again see L.C. Thomas paper).

Somewhat larger Q's can be achieved by adding more filter sections in either a synchronously tuned cascade (filters tuned to same center frequency and taking advantage of the bandwidth shrinkage factor which results from the series connection) or as a standard multiple pole filter. All of the conventional filters can be realized and selection is based upon all of the performance requirements which the application demands. The cost advantages of the LM3900, the relatively large bandwidth and the ease of operation on a single power supply voltage make this product an excellent ''building block'' for RC active filters.

7.0 Designing Waveform Generators

The multiple amplifiers of the LM3900 can be used to easily generate a wide variety of waveforms in the low frequency range (f ≤ 10 kHz). Voltage controlled oscillators (VCO)'s) are also possible and are presented in section 8.0 ''Designing Phase-locked Loops and Voltage Controlled

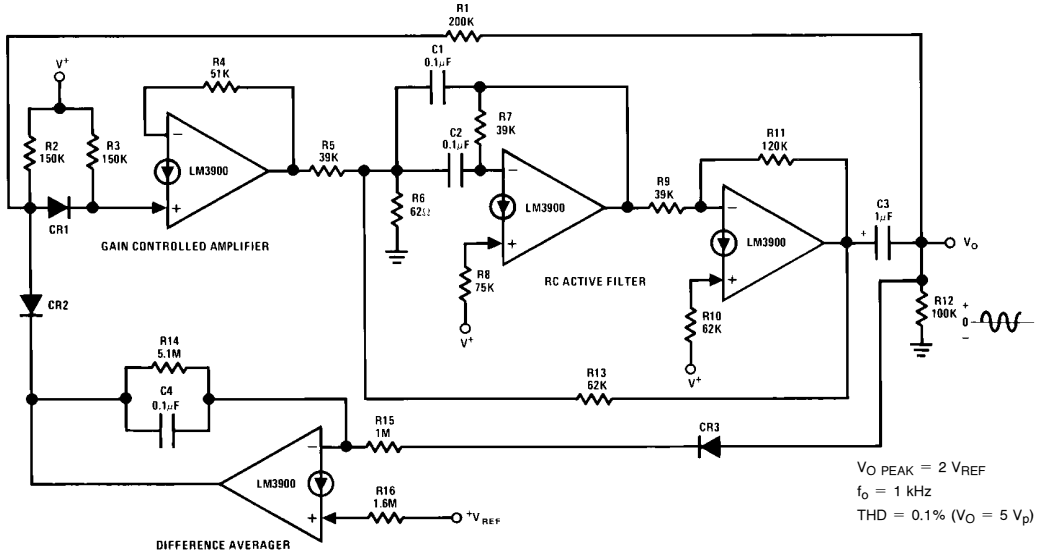

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FIGURE 41. A Sinewave Oscillator

Oscillators.'' In addition, power oscillators (such as noise makers, etc.) are presented in section 10.11.3. The waveform generators which will be presented in this section are mainly of the switching type, but for completeness a sinewave oscillator has been included.

7.1 A SINEWAVE OSCILLATOR

The design of a sinewave oscillator presents problems in both amplitude stability (and predictability) and output waveform purity (THD). If an RC bandpass filter is used as a high Q resonator for the oscillator circuit we can obtain an output waveform with low distortion and eliminate the problem of relative center frequency drift which exists if the active filter were used simply to filter the output of a separate oscillator.

A sinewave oscillator which is based on this principle is shown in *Figure 41*. The two-amplifier RC active filter is used as it requires only two capacitors and provides an overall non-inverting phase characteristic. If we add a non-inverting gain controlled amplifier around the filter we obtain the desired oscillator configuration. Finally, the sinewave output voltage is sensed and regulated as the average value is compared to a DC reference voltage, V_{REF}, by use of a differential averaging circuit. It can be shown that with the values selected for R_{15} and R_{16} (ratio of 0.64/1) that there is first order temperature compensation for CR_3 and the internal input diodes of the IC amplifier which is used for the ''difference averager''. Further, this also provides a simple way to regulate and to predict the magnitude of the output sinewave as

$$V_O \text{ peak} = 2\,V_{REF}$$

which is essentially independent of both temperature and the magnitude of the power supply voltage (if V_{REF} is derived from a stable voltage source).

7.2 SQUAREWAVE GENERATOR

The standard op amp squarewave generator has been modified as shown in *Figure 42*. The capacitor, C_1, alternately

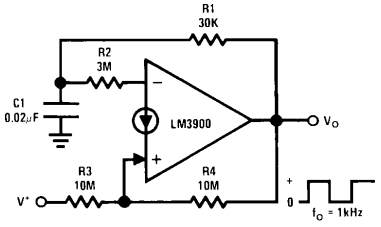

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FIGURE 42. A Squarewave Oscillator

charges and discharges (via R_1) between the voltage limits which are established by the resistors R_2, R_3 and R_4. This combination produces a Schmitt Trigger circuit and the operation can be understood by noticing that when the output is low (and if we neglect the current flow through R_4) the resistor R_2 (3M) will cause the trigger to fire when the current through this resistor equals the current which enters the (+) input (via R_3). This gives a firing voltage of approximately $R_2/(R_3)\ V^+$ (or $V^+/3$). The other trip point, when the output voltage is high, is approximately $[2(R_2/R_3)]\ V^+$, as $R_3 = R_4$, or $\frac{2}{3}(V^+)$. Therefore the voltage across the capacitor, C_1, will be the first one-half of an exponential waveform between these voltage trip limits and will have good symmetry and be essentially independent of the magnitude of the power supply voltage. If an unsymmetrical squarewave is desired, the trip points can be shifted to produce any desired mark/space ratio.

7.3 PULSE GENERATOR

The squarewave generator can be slightly modified to provide a pulse generator. The slew rate limits of the LM3900 (0.5V/μsec) must be kept in mind as this limits the ability to produce a narrow pulse when operating at a high power supply voltage level. For example, with a +15 V_{DC} power supply the rise time, t_r, to change 15V is given by:

$$t_r = \frac{15V}{\text{Slew Rate}} = \frac{15V}{0.5V/\mu\text{sec}}$$

$$t_r = 30\ \mu\text{sec}.$$

The schematic of a pulse generator is shown in *Figure 43*. A diode has been added, CR_1, to allow separating the charge path to C_1 (via R_1) from the discharge path (via R_2). The

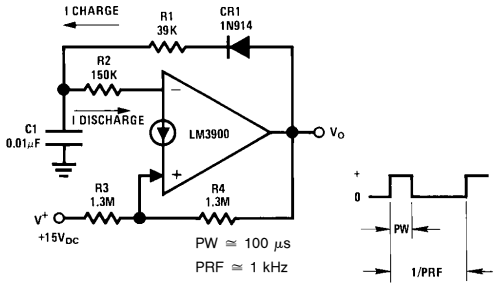

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FIGURE 43. A Pulse Generator

circuit operates as follows: Assume first that the output voltage has just switched low (and we will neglect the current flow through R_4). The voltage across C_1 is high and the magnitude of the discharge current (through R_2) is given by

$$I_{\text{Discharge}} \cong \frac{V_{C_1} - V_{BE}}{R_2}.$$

This current is larger than that entering the (+) input which is given by

$$I_{R_3} = \frac{V^+ - V_{BE}}{R_3}.$$

The excess current entering the (−) input terminal causes the amplifier to be driven to a low output voltage state (saturation). This condition remains for the long time interval (1/Pulse Repetition Frequency) until the R_2C_1 discharge current equals the I_{R_3} value (as CR_1 is OFF during this interval). The voltage across C_1 at the trip point, V_L, is given by

$$V_L = (I_{R_3})\,(R_2),$$

or

$$V_L = (V^+ - V_{BE})\left(\frac{R_2}{R_3}\right). \qquad (1)$$

At this time the output voltage will switch to a high state, V_{OHi}, and the current entering the (+) input will increase to

$$I_{M^+} = \frac{V^+ - V_{BE}}{R_3} + \frac{V_{OHi} - V_{BE}}{R_4}.$$

Also CR_1 goes ON and the capacitor, C_1, charges via R_1. Some of this charge current is diverted via R_2 to ground (the $(-)$ input is at V_{CESAT} during this interval as the current mirror is demanding more current than the $(-)$ input terminal can provide). The high trip voltage, V_H, is given by

$$V_H = (I_M{}^+)\, R_2 \quad \text{or}$$

$$V_H = \left(\frac{V^+ - V_{BE}}{R_3} + \frac{V_{OHi} - V_{BE}}{R_4}\right) R_2. \tag{2}$$

A design proceeds by first choosing the trip points for the voltage across C_1. The resistors R_3 and R_4 are used only for this trip voltage control. The resistor R_2 affects the discharge time (the long interval) and also both of the trip voltages so this resistor is determined first from the required pulse repetition frequency (PRF). The value of R_2 is determined by the RC exponential discharge from V_H to V_L as this time interval, T_1, controls the PRF ($T_1 = 1/\text{PRF}$). If we start with the equation for the RC discharge we have

$$V_L = V_H\, e^{-\frac{T_1}{R_2C_1}}$$

or

$$\ln \frac{V_L}{V_H} = -\frac{T_1}{R_2C_1}$$

or

$$T_1 = R_2C_1 \ln \frac{V_H}{V_L} \tag{3}$$

To provide a low duty cycle pulse train we select small values for both V_H and V_L (such as 3V and 1.5V) and choose a starting value for C_1. Then R_2 is given by

$$R_2 = \frac{T_1}{C_1 \ln \frac{V_H}{V_L}}. \tag{4}$$

If R_2 from (4) is not in the range of approximately 100 kΩ to 1 MΩ, choose another value for C_1. Now equation (1) can be used to find a value for R_3 to provide the V_L which was initially assumed. Similarly equation (2) allows R_4 to be calculated. Finally R_1 is determined by the required pulse width (PW) as the capacitor, C_1, must be charged from V_L to V_H by R_1. This RC charging is given by (neglecting the loading due to R_2)

$$V_H \cong (V_{OHi} - V_D)\left(1 - e^{-\frac{T_2}{R_1C_1}}\right)$$

or

$$T_2 \cong -R_1C_1 \ln\left[1 - \frac{V_H}{V_{OHi} - V_D}\right], \text{ and finally}$$

$$R_1 \cong \frac{T_2}{-C_1 \ln\left[1 - \frac{V_H}{V_{OHi} - V_D}\right]} \tag{5}$$

where T_2 is the pulse width desired and V_D is the forward voltage drop across CR_1.

As a design example:

Required: Provide a 100 μs pulse every 1 ms. The power supply voltage is $+15\ V_{DC}$

1.0 Start by choosing $V_L = 1.5V$

and $V_H = 3.0V$

2.0 Find R_2 from equation (4) assuming $C_1 = 0.01\ \mu F$,

$$R_2 = \frac{10^{-3}}{10^{-8} \ln\left(\frac{3.0}{1.5}\right)}$$

$$R_2 = \frac{10^5}{0.694} = 144\ k\Omega$$

3.0 Find R_3 from equation (1)

$$R_3 = \frac{(V^+ - V_{BE})\, R_2}{V_L}$$

$$R_3 = \frac{(15 - 0.5)\ 1.44 \times 10^5}{1.5}$$

$$R_3 = 1.39\ M\Omega$$

4.0 Find R_4 from equation (2),

$$R_4 = \frac{(V_{OHi} - V_{BE})}{\frac{V_H}{R_2} - \frac{V^+ - V_{BE}}{R_3}}$$

$$R_4 = \frac{(14.2 - 0.5)}{\frac{3}{1.44 \times 10^5} - \frac{15 - 0.5}{1.39 \times 10^6}}$$

$$R_4 = 1.32\ M\Omega$$

5.0 Find R_1 from equation (5),

$$R_1 = \frac{10^{-4}}{-10^{-8} \ln\left(1 - \frac{3}{(14.2 - 0.7)}\right)}$$

$$R_1 = \frac{10^4}{-\ln\left(1 - \frac{3}{13.5}\right)}$$

$$R_1 = \frac{10^4}{0.252} = 39.7\ k\Omega.$$

These values (to the nearest 5% standard) have been added to *Figure 43*.

7.4 TRIANGLE WAVEFORM GENERATOR

Triangle waveforms are usually generated by an integrator which receives first a positive DC input voltage, then a negative DC input voltage. The LM3900 easily provides this operation in a system which operates with only a single power supply voltage by making use of the current mirror which exists at the $(+)$ input. This allows the generation of a triangle waveform without requiring a negative DC input voltage.

The schematic diagram of a triangle waveform generator is shown in *Figure 44*. One amplifier is doing the integration by

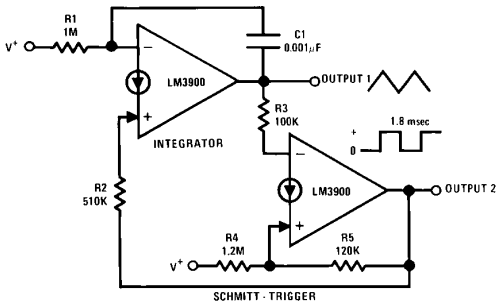

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FIGURE 44. A Triangle Waveform Generator

operating first with the current through R_1 to produce the negative output voltage slope, and then when the output of the second amplifier (the Schmitt Trigger) is high, the current through R_2 causes the output voltage to increase. If $R_1 = 2R_2$, the output waveform will have good symmetry. The timing for one-half of the period (T/2) is given by

$$\frac{T}{2} = \frac{(R_1C_1)\Delta V_O}{V^+ - V_{BE}}$$

or the output frequency becomes

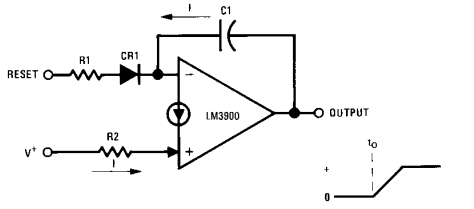
$$f_o = \frac{V^+ - V_{BE}}{2R_1C_1\Delta V_O}$$

where we have assumed $R_1 = 2R_2$, V_{BE} is the DC voltage at the (−) input (0.5 V_{DC}), and ΔV_O is the difference between the trip points of the Schmitt Trigger. The design of the Schmitt Trigger has been presented in the section on Digital and Switching Circuits (9.0) and the trip voltages control the peak-to-peak excursion of the triangle output voltage waveform. The output of the Schmitt circuit provides a squarewave of the same frequency.

7.5 SAWTOOTH WAVEFORM GENERATOR

The previously described triangle waveform generator, *Figure 44*, can be modified to produce a sawtooth waveform. Two types of waveforms can be provided, both a positive ramp and a negative ramp sawtooth waveform by selecting R_1 and R_2. The reset time is also controlled by the ratio of R_1 and R_2. For example, if $R_1 = 10\ R_2$ a positive ramp sawtooth results and if $R_2 = 10\ R_1$ a negative ramp sawtooth can be obtained. Again, the slew rate limits of the amplifier (0.5V/μs) will limit the minimum retrace time, and the increased slew rate of a negative going output will allow a faster retrace for a positive ramp sawtooth waveform.

To provide a gated sawtooth waveform, the circuits shown in *Figure 45* can be used. In *Figure 45(a)*, a positive ramp is generated by integrating the current, I, which is entering the (+) input. Reset is provided via R_1 and CR_1 keeps R_1 from loading at the (−) input during the sweep interval. This will sweep from $V_{O\ MIN}$ to $V_{O\ MAX}$ and will remain at $V_{O\ MAX}$ until reset. The interchange of the input leads, *Figure 45(b)*, will generate a negative ramp, from $V_{O\ MAX}$ to $V_{O\ MIN}$.



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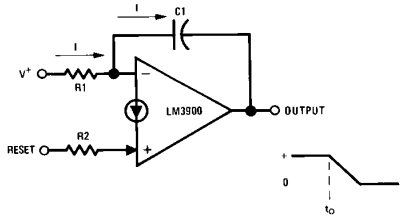
(a) Positive Ramp



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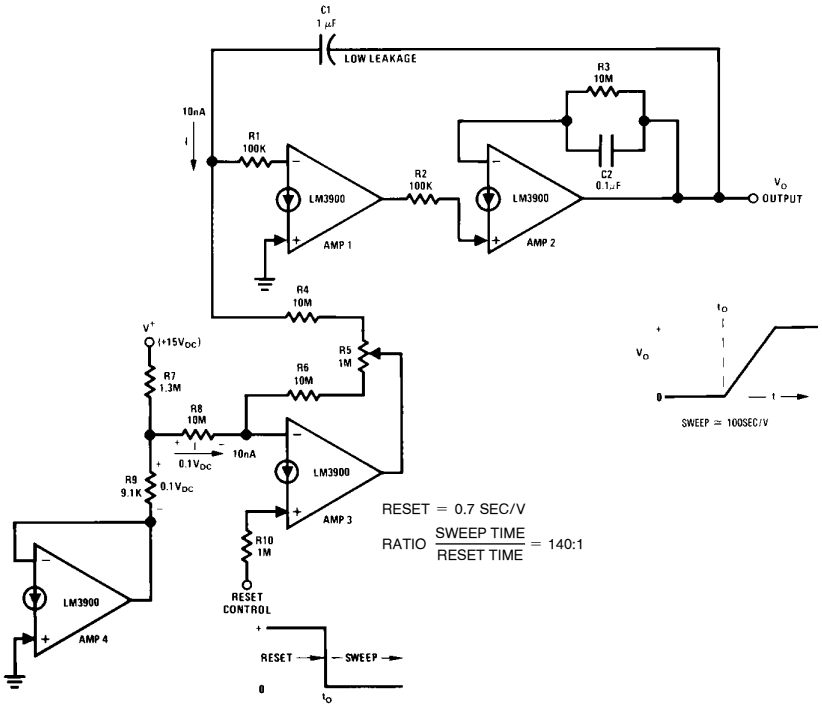
(b) Negative Ramp

FIGURE 45. Gated Sawtooth Generators



RESET = 0.7 SEC/V

RATIO $\frac{\text{SWEEP TIME}}{\text{RESET TIME}}$ = 140:1

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FIGURE 46. Generating Very Slow Sawtooth Waveforms

7.5.1 GENERATING A VERY SLOW SAWTOOTH WAVEFORM

The LM3900 can be used to generate a very slow sawtooth waveform which can be used to generate long time delay intervals. The circuit is shown in *Figure 46* and uses four amplifiers. Amps 1 and 2 are cascaded to increase the gain of the integrator and the output is the desired very slow sawtooth waveform. Amp 3 is used to exactly supply the bias current to Amp 1.

With resistor R_8 opened up and the reset control at zero volts, the potentiometer, R_5, is adjusted to minimize the drift in the output voltage of Amp 2 (this output must be kept in the linear range to insure that Amp 2 is not in saturation). Amp 4 is used to provide a bias reference which equals the DC voltage at the (−) input of Amp 3. The resistor divider, R_7 and R_9 provides a 0.1 V_{DC} reference voltage across R_9 which also appears across R_8. The current which flows through R_8, I, enters the (−) input of Amp 3 and causes the current through R_6 to drop by this amount. This causes an imbalance as now the current flow through R_4 is no longer adequate to supply the input current of Amp 1. The net result is that this same current, I, is drawn from capacitor C_1 and causes the output voltage of Amp 2 to sweep slowly positive. As a result of the high impedance values used, the PC component board used for this circuit must first be cleaned and then coated with silicone rubber to eliminate the effects of leakage currents across the surface of the board. The DC leakage currents of the capacitor, C_1, must also be small compared to the 10 nA charging current. For example, an insulation resistance of 100,000 MΩ will leak 0.1 nA with 10 V_{DC} across the capacitor and this leakage rapidly increases at higher temperatures. Dielectric polarization of the dielectric material may not cause problems if the circuit is not rapidly cycled. The resistor, R_8, and the capacitor, C_1, can be scaled to provide other basic sweep rates. For the values shown on *Figure 46* the 10 nA current and the 1μF capacitor establish a sweep rate of 100 sec/volt. The reset control pulse (Amp 3 (+) input) causes Amp 3 to go to the positive output saturation state and the 10 MΩ (R_4) gives a reset rate of 0.7 sec/volt. The resistor, R_1, prevents a large discharge current of C_1 from overdriving the (−) input and overloading the input clamp device. For larger charging currents, a resistor divider can be placed from the output of Amp 4 to ground and R_8 can tie from this tap point directly to the (−) input of Amp 1.

7.6 STAIRCASE WAVEFORM GENERATORS

A staircase generator can be realized by supplying pulses to an integrator circuit. The LM3900 also can be used with a squarewave input signal and a differentiating network where each transition of the input squarewave causes a step in the output waveform (or two steps per input cycle). This is shown in *Figure 47*. These pulses of current are the charge and discharge currents of the input capacitor, C_1. The charge current, I_C, enters the (+) input and is mirrored about ground and is ''drawn into'' the (−) input. The discharge current, I_D, is drawn through the diode at the input, CR_1, and therefore also causes a step on the output staircase.

A free running staircase generator is shown in *Figure 48*. This uses all four of the amplifiers which are available in one LM3900 package.

Amp 1 provides the input pulses which ''pump up'' the staircase via resistor R_1 (see section 7.3 for the design of this pulse generator). Amp 2 does the integrate and hold function and also supplies the output staircase waveform. Amps 3 and 4 provide both a compare and a one-shot multivibrator function (see the section on Digital and Switching Circuits for the design of this dual function one-shot). Resistor R_4 is used to sample the staircase output voltage and to compare it with the power supply voltage (V^+) via R_3. When the output exceeds approximately 80% of V^+ the connection of Amps 3 and 4 causes a 100 μsec reset pulse to be generated. This is coupled to the integrator (Amp 2) via R_2 and causes the staircase output voltage to fall to approximately zero volts. The next pulse out of Amp 1 then starts a new stepping cycle.

7.7 A PULSE COUNTER AND A VOLTAGE VARIABLE PULSE COUNTER

The basic circuit of *Figure 48* can be used as a pulse counter simply by omitting Amp 1 and feeding input voltage pulses directly to R_1. A simpler one-shot/comparator which requires only one amplifier can also be used in place of Amps 3 and 4 (again, see the section on Digital and Switching Circuits). To extend the time interval between pulses, an additional amplifier can be used to supply base current to Amp 2 to eliminate the tendency for the output voltage to drift up due to the 30 nA input current (see section 7.5.1). The pulse count can be made voltage variable simply by removing the comparator reference (R_3) from V^+ and using this as a control voltage input. Finally, the input could be derived from differentiating a squarewave input as was shown in *Figure 47* and if only one step per cycle were desired, the diode, CR_1 of *Figure 47*, can be eliminated.

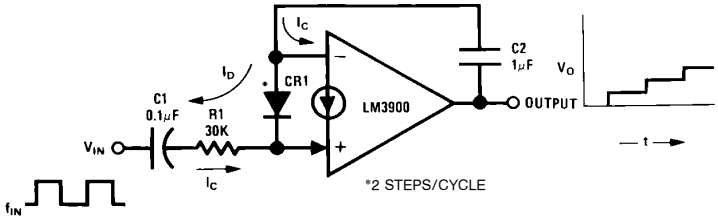

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FIGURE 47. Pumping the Staircase Via Input Differentiator

7.8 AN UP-DOWN STAIRCASE WAVEFORM GENERATOR

A staircase waveform which first steps up and then steps down is provided by the circuit shown in *Figure 49*. An input pulse generator provides the pulses which cause the output to step up or down depending on the conduction of the clamp transistor, Q_1. When this is ON, the ''down'' current pulse is diverted to ground and the staircase then steps ''up''. When the upper voltage trip point of Amp 2 (Schmitt Trigger—see section on Digital and Switching Circuits) is reached, Q_1 goes OFF and as a result of the smaller ''down'' input resistor (one-half the value of the ''up'' resistor, R_1) the staircase steps ''down'' to the low voltage trip point of Amp 2. The output voltage therefore steps up and down between the trip voltages of the Schmitt Trigger.

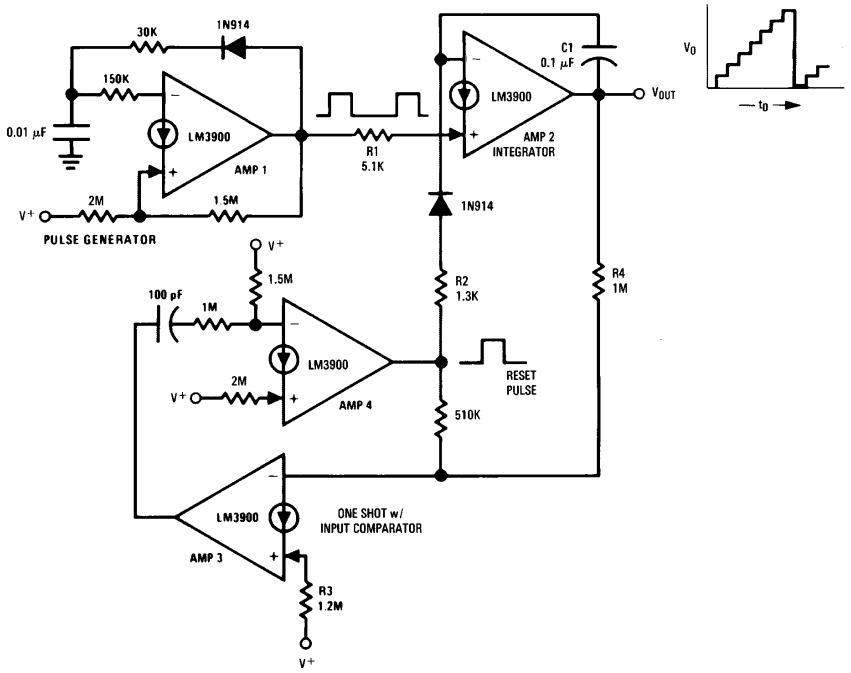

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FIGURE 48. A Free Running Staircase Generator

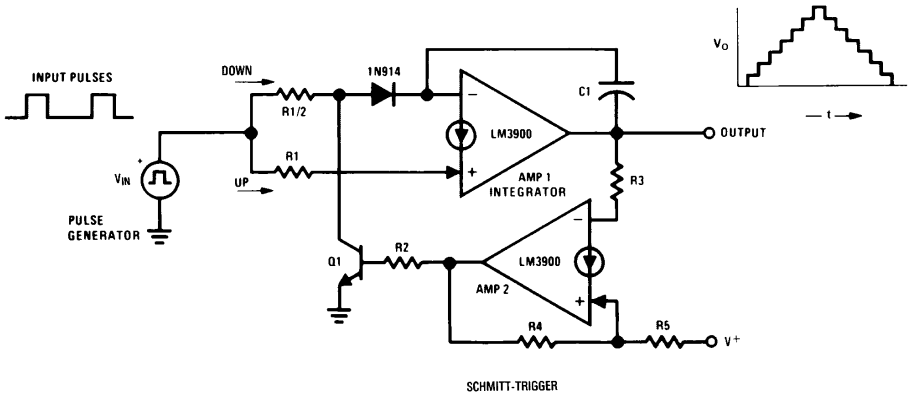

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FIGURE 49. An Up-down Staircase Generator

8.0 Designing Phase-Locked Loops and Voltage Controlled Oscillators

The LM3900 can be connected to provide a low frequency ($f < 10$ kHz) phase-locked loop (PL^2). This is a useful circuit for many control applications. Tracking filters, frequency to DC converters, FM modulators and demodulators are applications of a PL^2.

8.1 VOLTAGE CONTROLLED OSCILLATORS (VCO)

The heart of a PL^2 is the voltage controlled oscillator (VCO). As the PL^2 can be used for many functions, the required linearity of the transfer characteristic (frequency out vs. DC voltage in) depends upon the application. For low distortion demodulation of an FM signal, a high degree of linearity is necessary whereas a tracking filter application would not require this performance in the VCO.

A VCO circuit is shown in *Figure 50*. Only two amplifiers are required, one is used to integrate the DC input control voltage, V_C, and the other is connected as a Schmitt-trigger which monitors the output of the integrator. The trigger circuit is used to control the clamp transistor, Q_1. When Q_1 is conducting, the input current, I_2, is shunted to ground. During this one-half cycle the input current, I_1, causes the output voltage of the integrator to ramp down. At the minimum point of the triangle waveform (output 1), the Schmitt circuit changes state and transistor Q_1 goes OFF. The current, I_2, is exactly twice the value of I_1 ($R_2 = R_1/2$) such that a charge current (which is equal to the magnitude of the discharge current) is drawn through the capacitor, C, to provide the increasing portion of the triangular waveform (output 1).

The output frequency for a given DC input control voltage depends on the trip voltages of the Schmitt circuit (V_H and V_L) and the components R_1 and C_1 (as $R_2 = R_1/2$). The time to ramp down from V_H to V_L corresponds to one-half the period (T) of the output frequency and can be found by starting with the basic equation of the integrator

$$V_O = -\frac{1}{C}\int I_1\,dt \tag{1}$$

as I_1 is a constant (for a given value of V_C) which is given by

$$I_1 = \frac{V_C - V_{BE}}{R_1} \tag{2}$$

equation (1) simplifies to

$$\Delta V_O = -\frac{I_1}{C}(\Delta t)$$

or

$$\frac{\Delta V_O}{\Delta t} = -\frac{I_1}{C} \tag{3}$$

Now the time, Δt, to sweep from V_H to V_L becomes

$$\Delta t_1 = \frac{(V_H - V_L)\,C}{I_1} \quad \text{or}$$

$$T = \frac{2\,(V_H - V_L)\,C}{I_1} \quad \text{and}$$

$$f = \frac{1}{T} = \frac{I_1}{2\,(V_H - V_L)\,C}. \tag{4}$$

Therefore, once V_H, V_L, R_1 and C are fixed in value, the output frequency, f, is a linear function of I_1 (as desired for a VCO).

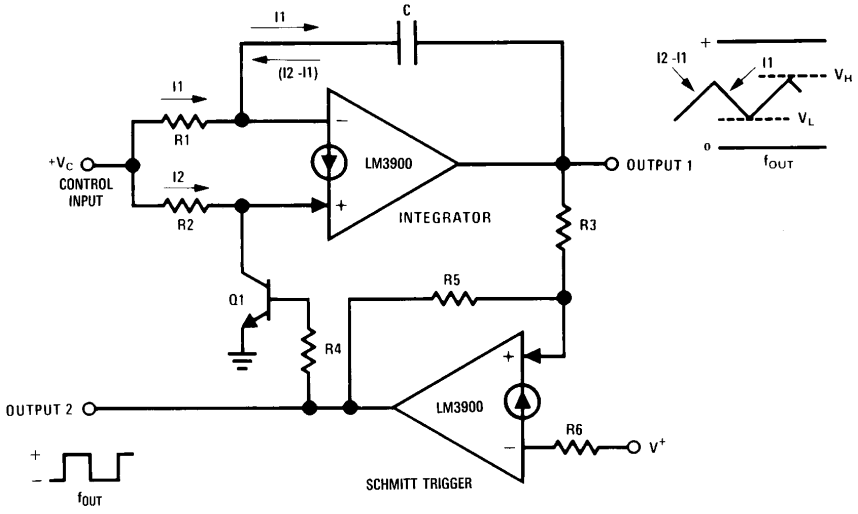

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FIGURE 50. A Voltage Controlled Oscillator

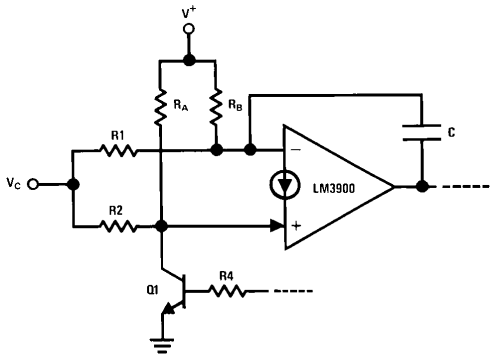

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FIGURE 51. Adding Input Common-mode Biasing Resistors

The circuit shown in *Figure 50* will require $V_C > V_{BE}$ to oscillate. A value of $V_C = 0$ provides $f_{OUT} = 0$, which may or may not be desired. Two common-mode input biasing resistors can be added as shown in *Figure 51* to allow $f_{OUT} = f_{MIN}$ for $V_C = 0$. In general, if these resistors are a factor of 10 larger than their corresponding resistor (R_1 or R_2) a large control frequency ratio can be realized. Actually, V_C could range outside the supply voltage limit of V^+ and this circuit will still function properly.

The output frequency of this circuit can be increased by reducing the peak-to-peak excursion of the triangle waveform (output 1) by design of the trip points of the Schmitt circuit. A limit is reached when the triangular sweep output waveform exceeds the slew rate limit of the LM3900 (0.5 V/μs). Note that the output of the Schmitt circuit has to move up only one V_{BE} to bring the clamp transistor, Q_1, ON, and therefore output slew rate of this circuit is not a limit.

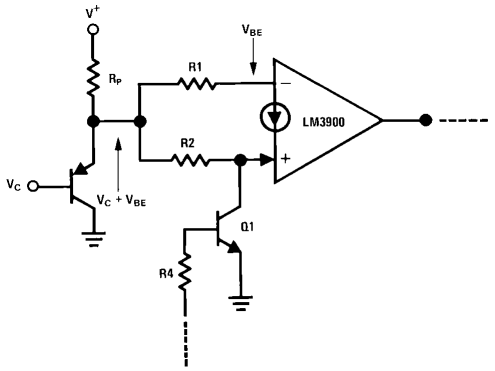

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FIGURE 52. Reducing Temperature Drift

To improve the temperature stability of the VCO, a PNP emitter follower can be used to give approximate compensation for the V_{BE}'s at the inputs to the amplifier (see *Figure 52*). Finally to improve the mark to space ratio accuracy over temperature and at low control voltages, an additional amplifier can be added such that both reference currents are applied to the same type of (inverting) inputs of the LM3900. The circuit to accomplish this is shown within dotted lines in *Figure 53*.

8.2 PHASE COMPARATOR

A basic phase comparator is shown in *Figure 54*. This circuit provides a pulse-width modulated output voltage waveform, V_O[1], which must be filtered to provide a DC output voltage (this filter can be the same as the one needed in the PL[2]). The resistor R_2 is made smaller than R_1 so the (+) input serves to inhibit the (−) input signal. The center of the

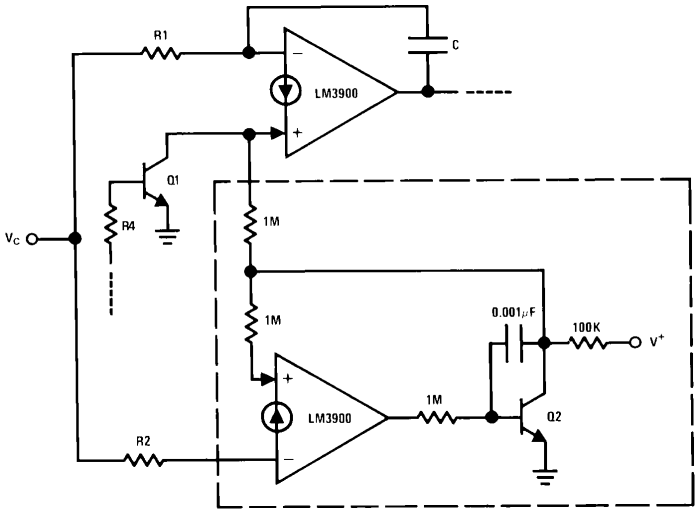

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FIGURE 53. Improving Mark/Space Ratio

dynamic range is indicated by the waveforms shown on the figure (90° phase difference between f_{IN} and f_{VCO}).

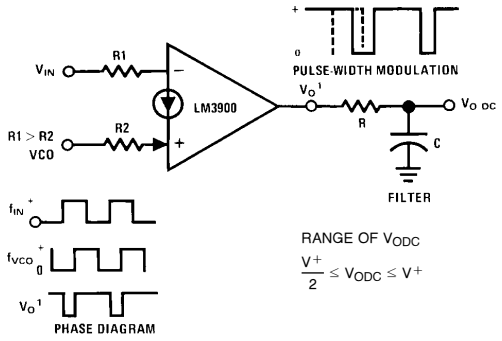

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FIGURE 54. Phase Comparator

The filtered DC output voltage will center at $3V^+/4$ and can range from $V^+/2$ to V^+ as the phase error ranges from 0 degrees to 180 degrees.

8.3 A COMPLETE PHASE-LOCKED LOOP

A phase-locked loop can be realized with three of the amplifiers as shown in *Figure 55*. This has a center frequency of approximately 3 kHz. To increase the lock range, DC gain can be added at the input to the VCO by using the fourth amplifier of the LM3900. If the gain is inverting, the limited DC dynamic range out of the phase detector can be increased to improve the frequency lock range. With inverting gain, the input to the VCO could go to zero volts. This will cause the output of the VCO to go high (V^+) and will latch if applied to the (+) input of the phase comparator. Therefore apply the VCO signal to the (−) input of the phase comparator or add the common-mode biasing resistors of *Figure 51.*

8.4 CONCLUSIONS

One LM3900 package (4 amplifiers) can provide all of the operations necessary to make a phase-locked loop. In addition, a VCO is a generally useful component for other system applications.

9.0 Designing Digital and Switching Circuits

The amplifiers of the LM3900 can be over-driven and used to provide a large number of low speed digital and switching circuit applications for control systems which operate off of single power supply voltages larger than the standard +5 V_{DC} digital limit. The large voltage swing and slower speed are both advantages for most industrial control systems. Each amplifier of the LM3900 can be thought of as "a super transistor" with a β of 1,000,000 (25 nA input current and 25 mA output current) and with a non-inverting input feature. In addition, the active pull-up and pull-down which exists at the output will supply larger currents than the simple resistor pull-ups which are used in digital logic gates. Finally, the low input currents allow timing circuits which minimize the capacitor values as large impedance levels can be used with the LM3900.

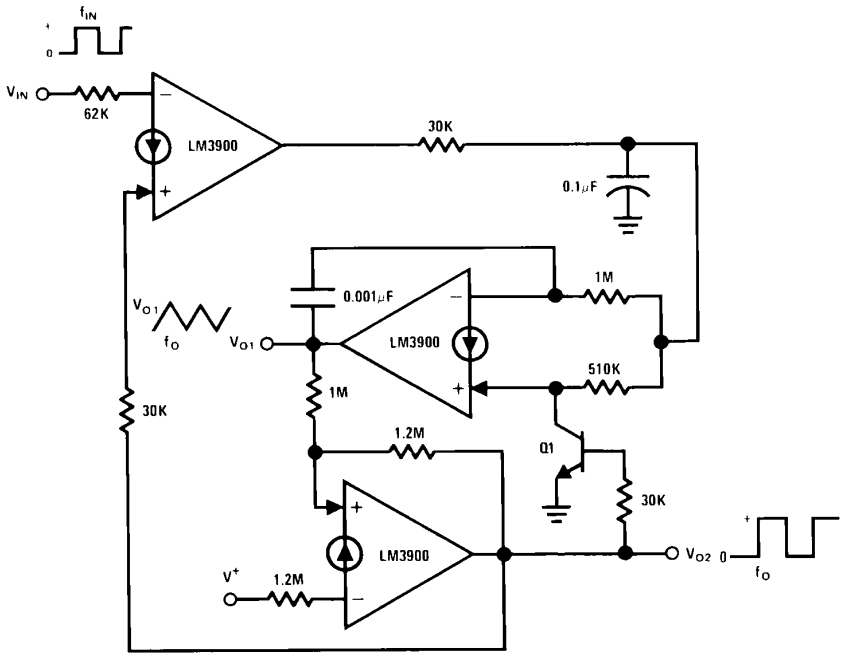

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FIGURE 55. A Phase-locked Loop

9.1 AN "OR" GATE

An OR gate can be realized by the circuit shown in *Figure 56*. A resistor (150 kΩ) from V^+ to the (−) input keeps the output of the amplifier in a low voltage saturated state for all inputs A, B, and C at 0V. If any one of the input signals were to go high ($\cong V^+$) the current flow through the 75 kΩ input resistor will cause the amplifier to switch to the positive output saturation state ($V_O \cong V^+$). The current loss through the other input resistors (which have an input in the low voltage state) represents an insignificant amount of the total input current which is provided by the, at least one, high voltage input. More than three inputs can be OR'ed if desired.

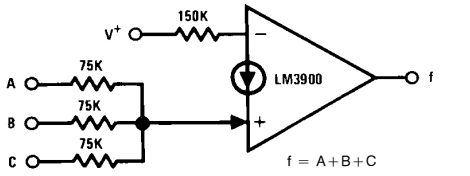

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FIGURE 56. An "OR" Gate

The "fan-out" or logical drive capability is large (50 gates if each gate input has a 75 kΩ resistor) due to the 10 mA output current capability of the LM3900. A NOR gate can be obtained by interchanging the inputs to the LM3900.

9.2 AN "AND" GATE

A three input AND gate is shown in *Figure 57*. This gate requires all three inputs to be high in order to have sufficient current entering the (+) input to cause the output of the amplifier to switch high. The addition of R_2 causes a smaller current to enter the (+) input when only two of the inputs are high. (A two input AND gate would not require a resistor

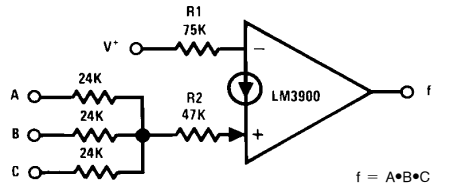

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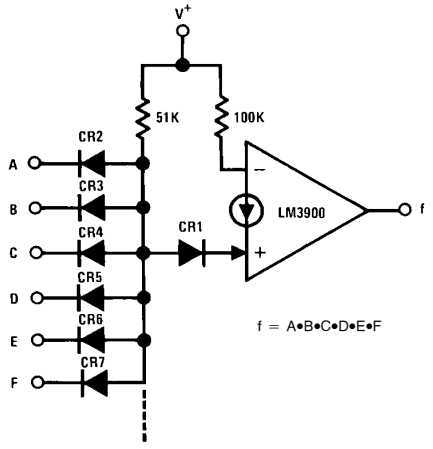
FIGURE 57. An "AND" Gate

as R_2). More than three inputs becomes difficult with this resistor summing approach as the (+) input is too close to having the necessary current to switch just prior to the last input going high. For a larger fan-in an input diode network (similar to DTL) is recommended as shown in *Figure 58*. Interchange the inputs for a NAND gate.

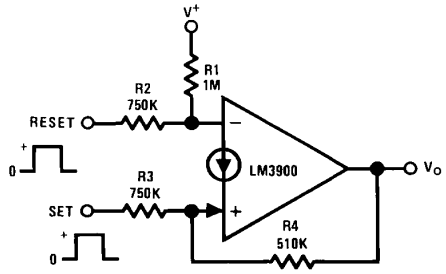


All Diodes 1N914 or Equiv. TL/H/7383–65

FIGURE 58. A Large Fan-in "AND" Gate

9.3 A BI-STABLE MULTIVIBRATOR

A bi-stable multivibrator (as asynchronous RS flip-flop) can be realized as shown in *Figure 59*. Positive feedback is provided by resistor R_4 which causes the latching. A positive pulse at the "set" input causes the output to go high and a "reset" positive pulse will return the output to essentially $0V_{DC}$.



TL/H/7383–66

FIGURE 59. A Bi-stable Multivibrator

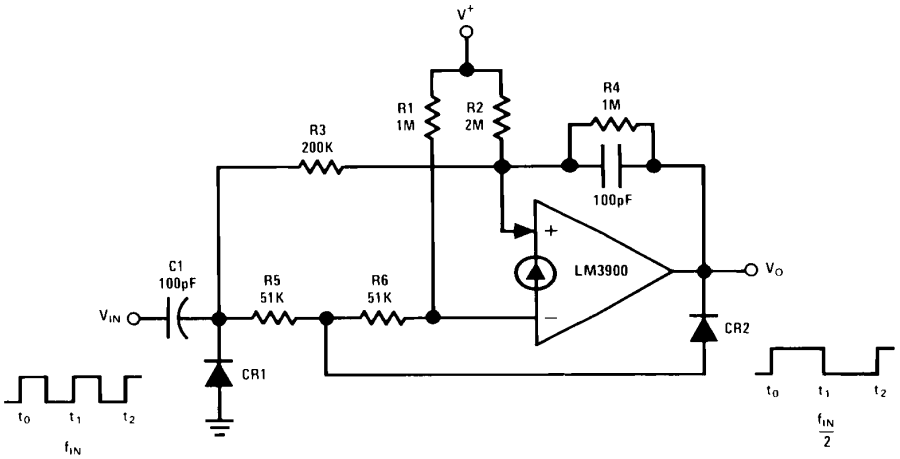
9.4 TRIGGER FLIP FLOPS

Trigger flip flops are useful to divide an input frequency as each input pulse will cause the output of a trigger flip flop to change state. Again, due to the absence of a clocking signal input, this is for an asynchronous logic application. A circuit which uses only one amplifier is shown in *Figure 60*. Steering of the differentiated positive input trigger is provided by the diode CR2. For a low output voltage state, CR2 shunts the trigger away from the (−) input and resistor R_3 couples this positive input trigger to the (+) input terminal. This causes the output to switch high. The high voltage output state now keeps CR2 OFF and the smaller value of (R_5 + R_6) compared with R_3 causes a larger positive input trigger to be coupled to the (−) input which causes the output to switch to the low voltage state.

A second trigger flip flop can be made which consists of two amplifiers and also provides a complementary output. This connection is shown in *Figure 61*.

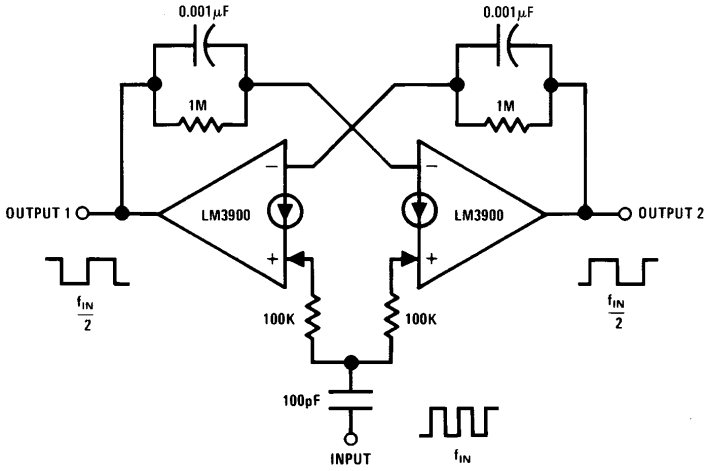
9.5 MONOSTABLE MULTIVIBRATORS (ONE-SHOTS)

Monostable multivibrators can be made using one or two of the amplifiers of the LM3900. In addition, the output can be designed to be either high or low in the quiescent state. Further, to increase the usefulness, a one-shot can be designed which triggers at a particular DC input voltage level to serve the dual role of providing first a comparator and then a pulse generator.



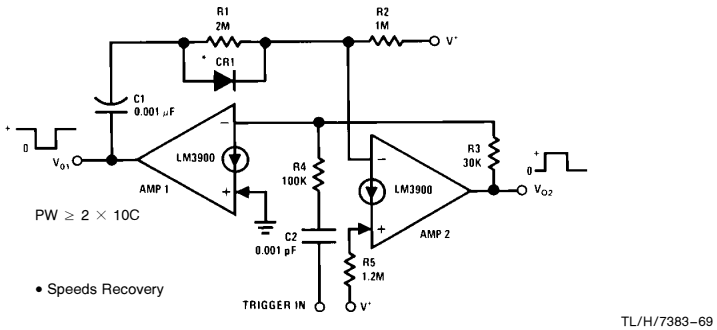
TL/H/7383–67

FIGURE 60. A Trigger Flip Flop



TL/H/7383–68

FIGURE 61. A Two-amplifier Trigger Flip Flop



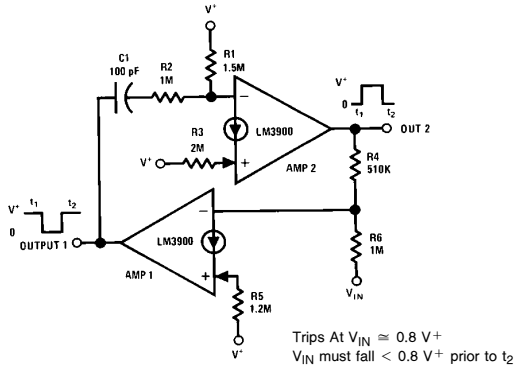
TL/H/7383–69

FIGURE 62. A One-shot Multivibrator

9.5.1 A TWO-AMPLIFIER ONE-SHOT

A circuit for a two-amplifier one-shot is shown in *Figure 62*. As the resistor, R_2, from V^+ to the (−) input is smaller than R_5 (from V^+ to the (+) input), amplifier 2 will be biased to a low-voltage output in the quiescent state. As a result, no current is supplied to the (−) input of amplifier 1 (via R_3) which causes the output of this amplifier to be in the high voltage state. Capacitor C_1 therefore has essentially the full V^+ supply voltage across it ($V^+ - 2\ V_{BE}$). Now when a differentiated trigger (due to C_2) causes amplifier 1 to be driven ON (output voltage drops to essentially zero volts) this negative transient is coupled (via C_1) to the (−) input of amplifier 2 which causes the output of this amplifier to be driven high (to positive saturation). This condition remains while C_1 discharges via (R_1) from approximately V^+ to approximately $V^+/2$. This time interval is the pulse width (PW). After C_1 no longer diverts sufficient current of R_2 away from the (−) input of amplifier 2 (i.e., C_1 is discharged to approximately $V^+/2$ V) the stable DC state is restored—amplifier 2 output low and amplifier 1 output high.

This circuit can be rapidly re-triggered due to the action of the diode, CR_1. This re-charges C_1 as amplifier 1 drives full output current capability (approximately 10 mA) through C_1, CR_1 and into the saturated (−) input of amplifier 2 to ground. The only time limit is the 10 mA available from amplifier 1 and the value of C_1. If a rapid reset is not required, CR_1 can be omitted.



TL/H/7383–70

FIGURE 63. A One-shot Multivibrator with an Input Comparator

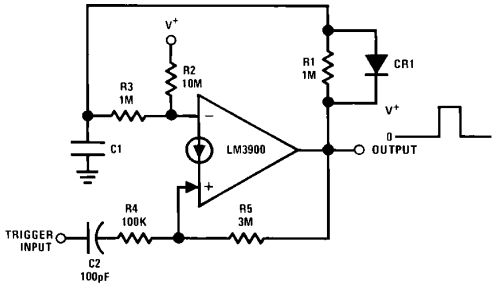
9.5.2 A COMBINATION ONE-SHOT/COMPARATOR CIRCUIT

In many applications a pulse is required if a DC input signal exceeds a predetermined value. This exists in free-running oscillators where after a particular output level has been reached a reset pulse must be generated to recycle the oscillator. This double function is provided with the circuit of *Figure 63*. The resistors R_5 and R_6 of amplifier 1 provide the inputs to a comparator and, as shown, an input signal, V_{IN}, is compared with the supply voltage, V^+. The output voltage of amplifier 1 is normally in a high voltage state and will fall and initiate the generation of the output pulse when V_{IN} is $R_6/R_5\ V^+$ or approximately 80% of V^+. To keep V_{IN} from disturbing the pulse generation it is required that V_{IN} fall to less than the trip voltage prior to the termination of the output pulse. This is the case when this circuit is used to generate a reset pulse and therefore this causes no problems.

9.5.3 A ONE-AMPLIFIER ONE-SHOT (POSITIVE PULSE)

A one-shot circuit can be realized using only one amplifier as shown in *Figure 64*.

The resistor R_2 keeps the output in the low voltage state. A differentiated positive trigger causes the output to switch to the high voltage state and resistor R_5 latches this state. The capacitor, C_1, charges from essentially ground to approximately $V^+/4$ where the circuit latches back to the quiescent state. The diode, CR_1, is used to allow a rapid re-triggering.

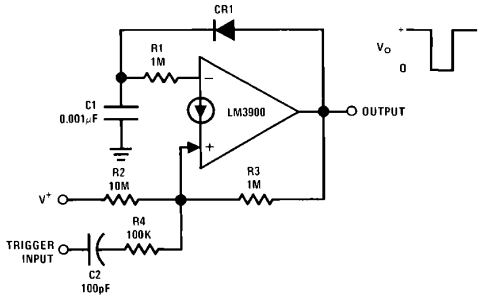


TL/H/7383–71

FIGURE 64. A One-amplifier One-shot (Positive Output)

9.5.4 A ONE-AMPLIFIER ONE-SHOT (NEGATIVE PULSE)

A one-amplifier one-shot multivibrator which has a quiescent state with the output high and which falls to zero volts for the pulse duration is shown in *Figure 65*.



TL/H/7383–72

FIGURE 65. A One-Amplifier One-Shot (Negative Output)

The sum of the currents through R_2 and R_3 keeps the (−) input at essentially ground. This causes V_O to be in the high voltage state. A differentiated negative trigger waveform causes the output to switch to the low voltage state. The large voltage across C_1 now provides input current via R_1 to keep the output low until C_1 is discharged to approximately $V^+/10$. At this time the output switches to the stable high voltage state.

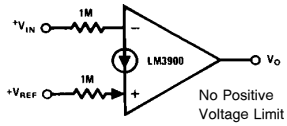
If the R_4C_2 network is moved to the (−) input terminal, the circuit will trigger on a differentiated positive trigger waveform.

9.6 COMPARATORS

The voltage comparator is a function required for most system operations and can easily be performed by the LM3900. Both an inverting and a non-inverting comparator can be obtained.

9.6.1 A COMPARATOR FOR POSITIVE INPUT VOLTAGES

The circuit in *Figure 66* is an inverting comparator. To insure proper operation, the reference voltage must be larger than



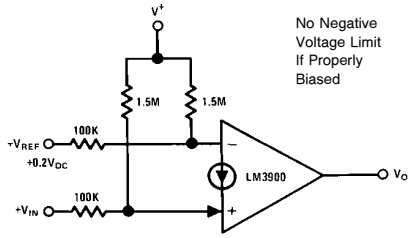
TL/H/7383–73

FIGURE 66. An Inverting Voltage Comparator

V_{BE}, but there is no upper limit as long as the input resistor is large enough to guarantee that the input current will not exceed 200 μA.

9.6.2 A COMPARATOR FOR NEGATIVE INPUT VOLTAGES

Adding a common-mode biasing network to the comparator in *Figure 66* makes it possible to compare voltages between zero and one volt as well as the comparison of rather large negative voltages, *Figure 67*. When working with negative voltages, the current supplied by the common-mode network must be large enough to satisfy both the current drain demands of the input voltages and the bias current requirement of the amplifier.

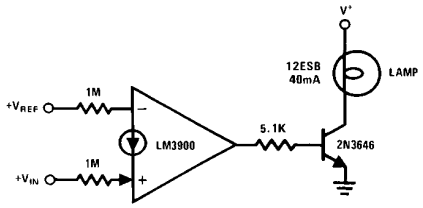


TL/H/7383–74

FIGURE 67. A Non-inverting Low-voltage Comparator

9.6.3 A POWER COMPARATOR

When used in conjunction with an external transistor, this power comparator will drive loads which require more current than the IC amplifier is capable of supplying. *Figure 68* shows a non-inverting comparator which is capable of driving a 12V, 40 mA panel lamp.

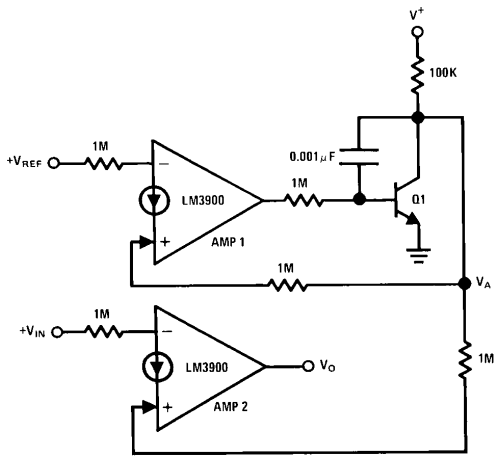


TL/H/7383–75

FIGURE 68. A Non-inverting Power Comparator

9.6.4 A MORE PRECISE COMPARATOR

A more precise comparator can be designed by using a second amplifier such that the input voltages of the same type of inputs are compared. The (−) input voltages of two amplifiers are naturally more closely matched initially and track well with temperature changes. The comparator of *Figure 69* uses this concept.



TL/H/7383–76

FIGURE 69. A More Precise Comparator

The current established by V_{REF} at the inverting input of amplifier 1 will cause transistor Q_1 to adjust the value of V_A to supply this current. This value of V_A will cause an equal current to flow into the non-inverting input of amplifier 2. This current corresponds more exactly to the reference current of amplifier 1.

A differential input stage can also be added to the LM3900 (see section 10.16) and the resulting circuit can provide a precision comparator circuit.

9.7 SCHMITT TRIGGERS

Hysteresis may be designed into comparators which use the LM3900 as shown in *Figure 70*.

The lower switch point for the inverting Schmitt-Trigger is determined by the amount of current flowing into the positive input with the output voltage low. When the input current, I_3, drops below the level required by the current mirror, the output will switch to the high limit. With V_O high, the current demanded by the mirror is increased by a fixed amount, I_2. As a result, the I_3 required to switch the output increases this same amount. Therefore, the switch points are determined by selecting resistors which will establish the required currents at the desired input voltages. Reference current (I_1) and feedback current (I_2) are set by the following equation.

$$I_1 = \frac{V^+ - \phi}{R_B}$$

$$I_2 = \frac{V_{O\,MAX} - \phi}{R_F}$$

By adjusting the values of R_B, R_F, and R_{IN}, the switching values of V_{IN} may be set to any levels desired.

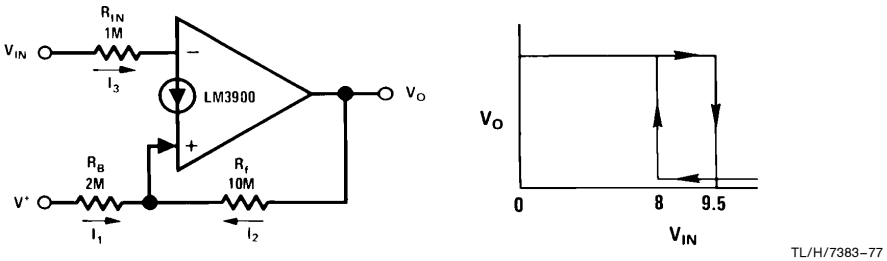
The non-inverting Schmitt Trigger works in the same way except that the input voltage is applied to the (+) input. The range of V_{IN} may be very large when compared with the operating voltage of the amplifier.

10.0 Some Special Circuit Applications

This section contains various special circuits which did not fit the order of things or which are one-of-a-kind type of applications.

10.1 CURRENT SOURCES AND SINKS

The amplifiers of the LM3900 can be used in feedback loops which regulate the current in external PNP transistors to provide current sources or in external NPN transistors to provide current sinks. These can be multiple sources or single sources which are fixed in value or made voltage variable.



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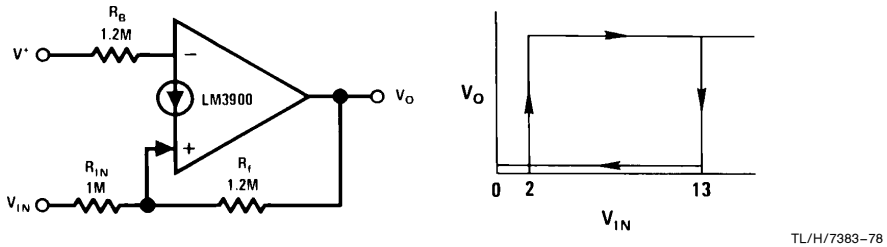
(a) Inverting



TL/H/7383–78

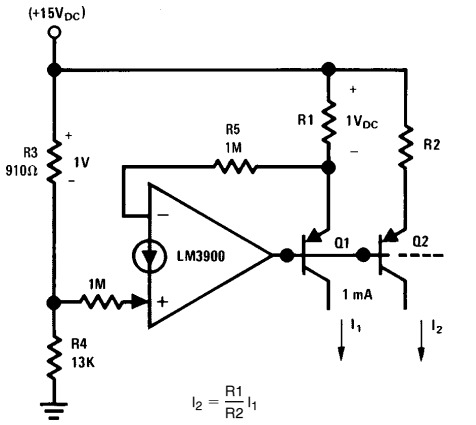
(b) Non-inverting

FIGURE 70. Schmitt Triggers

10.1.1 A FIXED CURRENT SOURCE

A multiple fixed current source is provided by the circuit of *Figure 71*. A reference voltage (1 V_{DC}) is established across resistor R_3 by the resistive divider (R_3 and R_4). Negative feedback is used to cause the voltage drop across R_1 to also be 1 V_{DC}. This controls the emitter current of transistor Q_1 and if we neglect the small current diverted into the (−) input via the 1M input resistor (13.5 μA) and the base current of Q_1 and Q_2 (an additional 2% loss if the β of these transistors is 100), essentially this same current is available out of the collector of Q_1.

Larger input resistors can be used to reduce current loss and a Darlington connection can be used to reduce errors due to the β of Q_1.



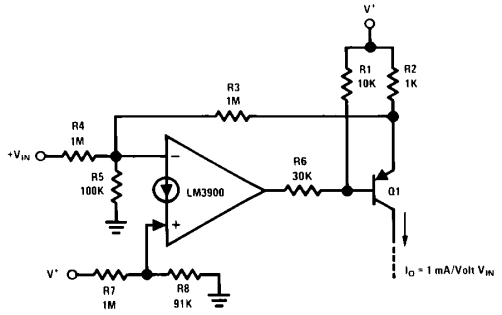
TL/H/7383–79

FIGURE 71. Fixed Current Sources

The resistor, R_2, can be used to scale the collector current of Q_2 either above or below the 1 mA reference value.

10.1.2 A VOLTAGE VARIABLE CURRENT SOURCE

A voltage variable current source is shown in *Figure 72*. The transconductance is $-(1/R_2)$ as the voltage gain from the input terminal to the emitter of Q_1 is -1. For a $V_{IN} = 0$ V_{DC} the output current is essentially zero mA DC. The resistors R_1 and R_6 guarantee that the amplifier can turn OFF transistor Q_1.

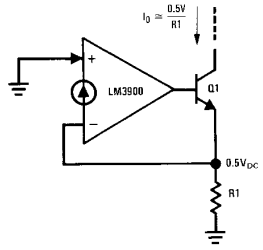


TL/H/7383–80

FIGURE 72. A Voltage Controlled Current Source

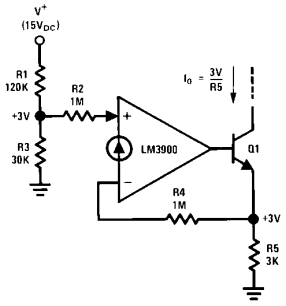
10.1.3 A FIXED CURRENT SINK

Two current sinks are shown in *Figure 73*. The circuit of *Figure 73(a)* requires only one resistor and supplies an output current which is directly proportional to this R value. A negative temperature coefficient will result due to the 0.5 V_{DC} reference being the base-emitter junction voltage of the (−) input transistor. If this temperature coefficient is objectionable, the circuit of *Figure 73(b)* can be employed.



TL/H/7383–81

(a) A Simple Current Sink



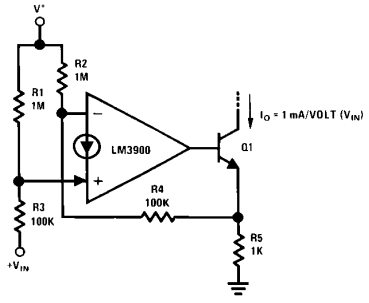
TL/H/7383–82

(b) Reducing Temperature Drift Of I_O

FIGURE 73. Fixed Current Sinks

10.1.4 A VOLTAGE VARIABLE CURRENT SINK

A voltage variable current sink is shown in *Figure 74*. The output current is 1 mA per volt of V_{IN} (as $R_5 = 1$ kΩ and the gain is $+1$). This circuit provides approximately 0 mA output current for $V_{IN} = 0$ V_{DC}.



TL/H/7383–83

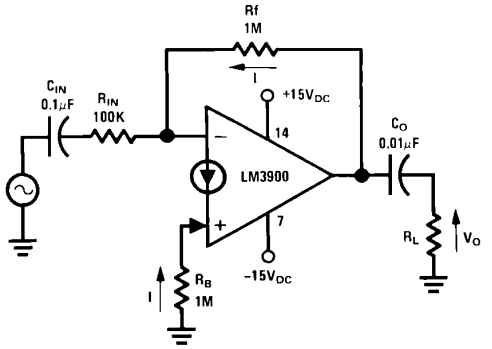
FIGURE 74. A Voltage Controlled Current Sink

10.2 OPERATION FROM ±15 V_{DC} POWER SUPPLIES

If the ground pin (no. 7) is returned to a negative voltage and some changes are made in the biasing circuits, the LM3900 can be operated from ±15 V_{DC} power supplies.

10.2.1 AN AC AMPLIFIER OPERATING WITH ±15 V_{DC} POWER SUPPLIES

An AC coupled amplifier is shown in *Figure 75*. The biasing resistor, R_B, is now returned to ground and both inputs bias at one V_{BE} above the $-V_{EE}$ voltage (approximately -15 V_{DC}).



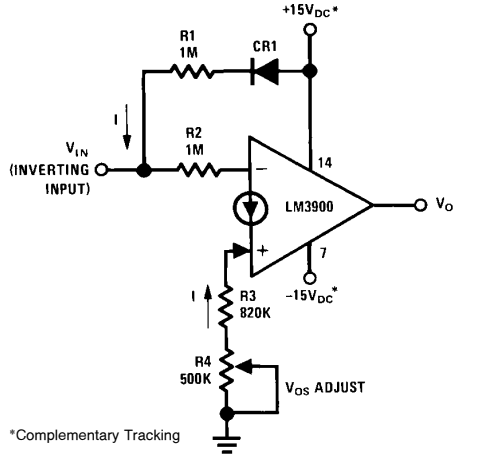
TL/H/7383–84

FIGURE 75. An AC Amplifier Operating With ±15 V_{DC}

With $R_f = R_B$, V_O will bias at approximately 0 V_{DC} to allow a maximum output voltage swing. As pin 7 is common to all four of the amplifiers which are in the same package, the other amplifiers are also biased for operation off of ±15 V_{DC}.

10.2.2 A DC AMPLIFIER OPERATING WITH ±15 V_{DC} POWER SUPPLIES

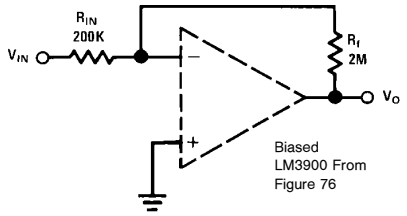
Biasing a DC amplifier is more difficult and requires that the ± power supplies be complementary tracking (i.e., $|+V_{CC}| = |-V_{EE}|$). The operation of this biasing can be understood if we start by first considering the amplifier without including the feedback resistors, as shown in *Figure 76*. If $R_1 = R_2 = R_3 + R_4 = 1\ M\Omega$ and $|+V_{CC}| = |-V_{EE}|$,



TL/H/7383–85

FIGURE 76. DC Biasing for ±15 V_{DC} Operation

then the current, I, will bias V_{IN} at zero volts DC (resistor R_4 can be used to adjust this). The diode, CR_1, has been added for temperature compensation of this biasing. Now, if we include these biasing resistors, we have a DC amplifier with the input biased at approximately zero volts. If feedback resistors are added around this biased amplifier we get the schematic shown in *Figure 77*.



TL/H/7383–86

FIGURE 77. A DC Amplifier Operating with ±15 V_{DC}

This is a standard inverting DC amplifier connection. The (+) input is "effectively" at ground and the biasing shown in *Figure 76* is used to take care of DC levels at the inputs.

10.3 TACHOMETERS

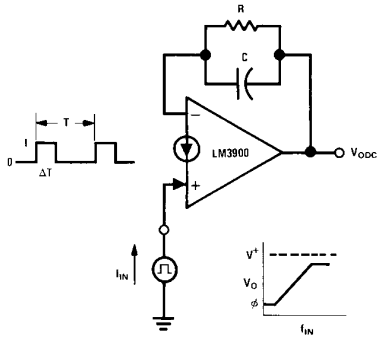
Many pulse averaging tachometers can be built using the LM3900. Inputs can be voltage pulses, current pulses or the differentiated transitions of squarewaves. The DC output voltage can be made to increase with increasing input frequency, can be made proportional to twice the input frequency (frequency doubling for reduced output ripple), and can also be made proportional to either the sum or the difference between two input frequencies. Due to the small bias current and the high gain of the LM3900, the transfer function is linear between the saturation states of the amplifier.

10.3.1 A BASIC TACHOMETER

If an RC averaging network is added from the output to the (−) input, the basic tachometer of *Figure 78* results. Current pulse inputs will provide the desired transfer function shown on the figure. Each input current pulse causes a small change in the output voltage. Neglecting the effects of R we have

$$\Delta V_O \cong \frac{I\Delta t}{C}$$

The inclusion of R gives a discharge path so the output voltage does not continue to integrate, but rather provides the time dependency which is necessary to average the input pulses. If an additional signal source is simply placed in parallel with the one shown, the output becomes proportional to the sum of these input frequencies. If this additional source were applied to the (−) input, the output voltage would be proportional to the difference between these input frequencies. Voltage pulses can be converted to current pulses by using an input resistor. A series isolating diode should be used if a signal is applied to the (−) input to prevent loading during the low voltage state of this input signal.

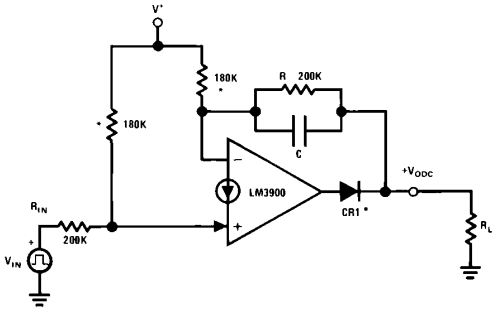


TL/H/7383–87

FIGURE 78. A Basic Tachometer

10.3.2 EXTENDING V_{OUT} (MINIMUM) TO GROUND

The output voltage of the circuit of *Figure 78* does not go to ground level but has a minimum value which is equal to the V_{BE} of the (−) input (0.5 V_{DC}). If it is desired that the output voltage go exactly to ground, the circuit of *Figure 79* can be used. Now with V_{IN} = 0 V_{DC}, V_O = 0 V_{DC} due to the addition of the common-mode biasing resistors (180 kΩ).



TL/H/7383–88

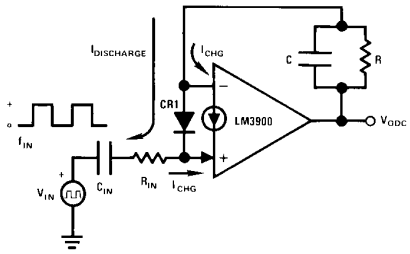
FIGURE 79. Adding Biasing to Provide V_O = 0 V_{DC}

The diode, CR_1, allows the output to go below $V_{CE\ SAT}$ of the output, if desired (a load is required to provide a DC path for the biasing current flow via the R of the averaging network).

10.3.3 A FREQUENCY DOUBLING TACHOMETER

To reduce the ripple on the DC output voltage, the circuit of *Figure 80* can be used to effectively double the input frequency. Input pulses are not required, a squarewave is all that is needed. The operation of the circuit is to average the charge and discharge transient currents of the input capacitor, C_{IN}. The resistor, R_{IN}, is used to convert the voltage pulses to current pulses and to limit the surge currents (to approximately 200 μA peak—or less if operating at high temperatures).

When the input voltage goes high, the charging current of C_{IN}, I_{CHG} enters the (+) input, is mirrored about ground and is drawn from the RC averaging network into the (−) input terminal. When the input voltage goes back to ground, the discharge current of C_{IN}, $I_{DISCHARGE}$ will also be drawn from the RC averaging network via the now conducting diode, CR_1. This full wave action causes two current pulses to be drawn through the RC averaging network for each cycle of the input frequency.

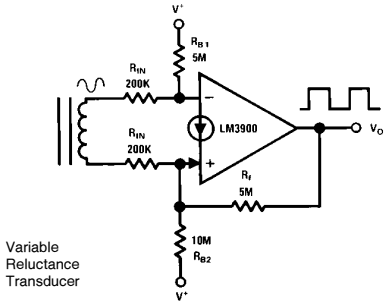


TL/H/7383–89

FIGURE 80. A Frequency Doubling Tachometer

10.4 A SQUARING AMPLIFIER

A squaring amplifier which incorporates symmetrical hysteresis above and below the zero output state (for noise immunity) is often needed to amplify the low level signals which are provided by variable reluctance transducers. In addition, a high frequency roll-off (low pass characteristic) is desirable both to reduce the natural voltage buildup at high frequencies and to also filter high frequency input noise disturbances. A simple circuit which accomplishes this function is shown in *Figure 81*. The input voltage is converted to



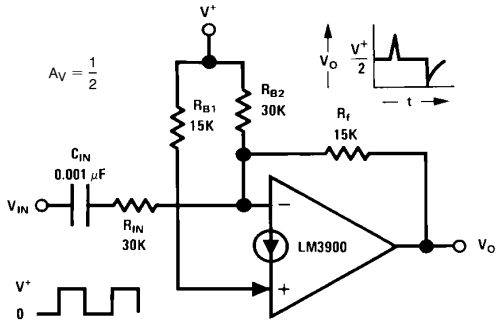
TL/H/7383–90

FIGURE 81. A Squaring Amplifier with Hysteresis

input currents by using the input resistors, R_{IN}. Common-mode biasing is provided by R_{B1} and R_{B2}. Finally positive feedback (hysteresis) is provided by R_f. The large source resistance, R_{IN}, provides a low pass filter due to the "Miller-effect" input capacitance of the amplifier (approximately 0.002 μF). The amount of hysteresis and the symmetry about the zero volt input are controlled by the positive feedback resistor, R_f, and R_{B1} and R_{B2}. With the values shown in *Figure 81* the trip voltages are approximately ±150 mV centered about the zero output voltage state of the transducer (at low frequencies where the low pass filter is not attenuating the input signal).

10.5 A DIFFERENTIATOR

An input differentiating capacitor can cause the input of the LM3900 to swing below ground and actuate the input clamp circuit. Again, common-mode biasing can be used to prevent this negative swing at the input terminals of the LM3900. The schematic of a differentiator circuit is shown in *Figure 82*. Common-mode biasing is provided by R_{B1} and



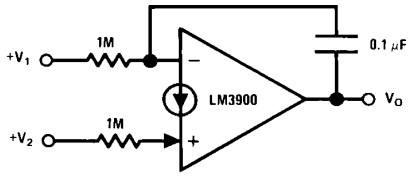
TL/H/7383–91

FIGURE 82. A Differentiator Circuit

R_{B2}. The feedback resistor, R_f, is one-half the value of R_{IN} so the gain is 1/2. The output voltage will bias at $V^+/2$ which thereby allows both a positive and a negative swing above and below this bias point. The resistor, R_{IN}, keeps the negative swing isolated from the (−) input terminal and therefore both inputs remain biased at $+V_{BE}$.

10.6 A DIFFERENCE INTEGRATOR

A difference integrator is the basis of many of the sweep circuits which can be realized using the LM3900 operating on only a single power supply voltage. This circuit can also be used to provide the time integral of the difference between two input waveforms. The schematic of the difference integrator is shown in *Figure 83*.



TL/H/7383–92

FIGURE 83. A Difference Integrator

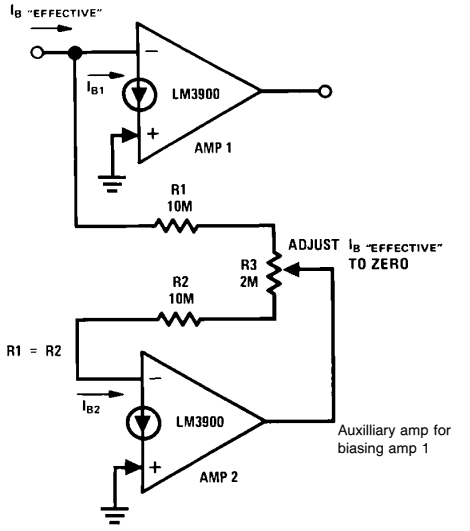
This is a useful component for DC feedback loops as both the comparison to a reference and the integration take place in one amplifier.

10.7 A LOW DRIFT SAMPLE AND HOLD CIRCUIT

In sample and hold applications a very low input biasing current is required. This is usually achieved by using a FET transistor or a special low input current IC op amp. The existence of many matched amplifiers in the same package allows the LM3900 to provide some interesting low ''equivalent'' input biasing current applications.

10.7.1 REDUCING THE ''EFFECTIVE'' INPUT BIASING CURRENT

One amplifier can be used to bias one or more additional amplifiers as shown in *Figure 84*.



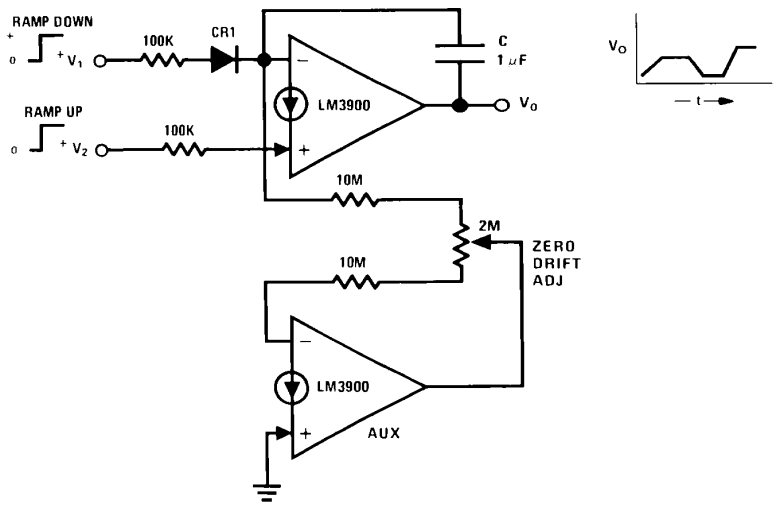
TL/H/7383–93

FIGURE 84. Reducing I_B ''Effective'' to Zero

The input terminal of Amp. 1 will only need to supply the signal current if the DC biasing current, I_{B1}, is accurately supplied via R_1. The adjustment, R_3, allows a zeroing of ''I_B effective'' but simply omitting R_3 and letting $R_1 = R_2$ (and relying on amplifier symmetry) can cause I_B ''effective'' to be less than $I_B/10$ (3 nA). This is useful in circuit applications such as sample and hold, where small values of I_B ''effective'' are desirable.

10.7.2 A LOW DRIFT RAMP AND HOLD CIRCUIT

The input current reduction technique of the previous section allows a relatively simple ramp and hold circuit to be built which can be ramped up or down or allowed to remain at any desired output DC level in a ''hold'' mode. This is shown in *Figure 85*. If both inputs are at 0 V_{DC} the circuit is in a hold mode. Raising either input will cause the DC output voltage to ramp either up or down depending on which one goes positive. The slope is a function of the magnitude of the input voltage and additional inputs can be placed in parallel, if desired, to increase the input control variables.

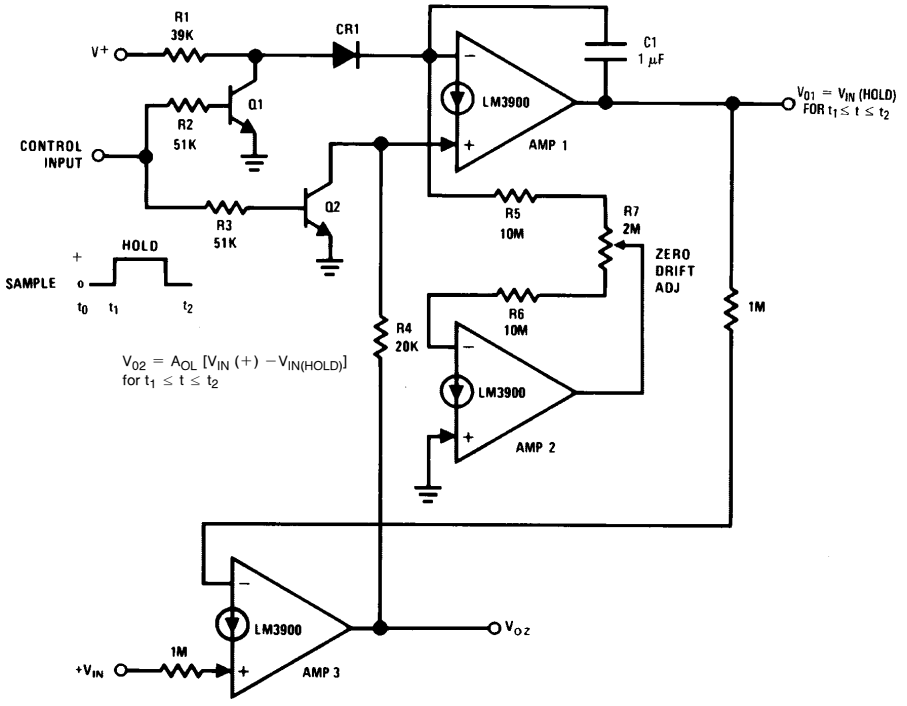


TL/H/7383–94

FIGURE 85. A Low-Drift Ramp and Hold Circuit

10.7.3 SAMPLE-HOLD AND COMPARE WITH NEW $+V_{IN}$

An example of using the circuit of the previous section is shown in *Figure 86* where clamping transistors, Q_1 and Q_2, put the circuit in a hold mode when they are driven ON. When OFF the output voltage of Amp. 1 can ramp either up or down as needed to guarantee that the output voltage of Amp. 1 is equal to the DC input voltage which is applied to Amp. 3. Resistor R_1 provides a fixed "down" ramp current which is balanced or controlled via the comparator, Amp. 3, and the resistor R_4. When Q_1 and Q_2 are OFF a feedback loop guarantees that V_{01} (from Amp. 1) is equal to $+V_{IN}$ (to Amp. 3). Amplifier 2 is used to supply the input biasing current to Amp. 1.



TL/H/7383–95

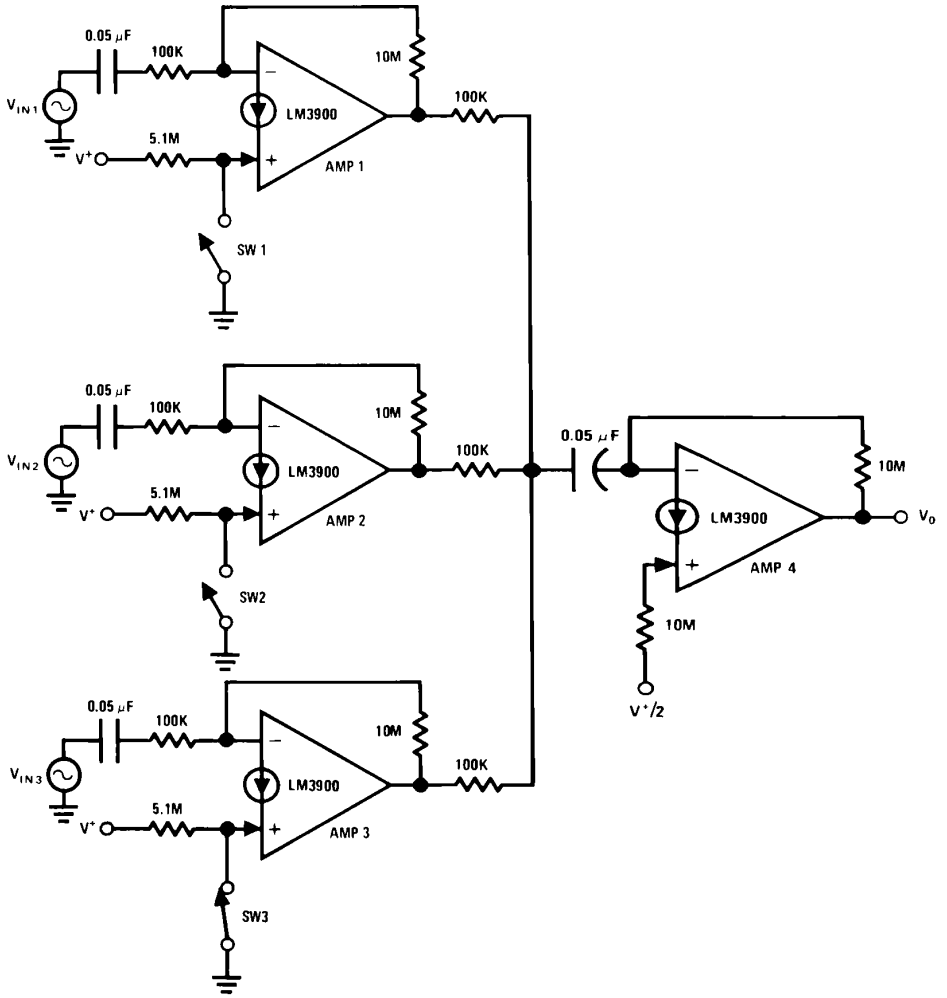
FIGURE 86. Sample-Hold and Compare with New $+V_{IN}$

The stored voltage appears at the output, V_{01} of Amp. 1, and as Amp. 3 is active, a continued comparison is made between V_{01} and V_{IN} and the output of Amp. 3 fully switches based on this comparison. A second loop could force V_{IN} to be maintained at the stored value (V_{01}) by making use of V_{02} as an error signal for this second loop. Therefore, a control system could be manually controlled to bring it to a particular operating condition; then, by exercising the hold control, the system would maintain this operating condition due to the analog memory provided by V_{01}.

10.8 AUDIO MIXER OR CHANNEL SELECTOR

The multiple amplifiers of the LM3900 can be used for audio mixing (many amplifiers simultaneously providing signals which are added to generate a composite output signal) or for channel selection (only one channel enabled at a time). Three amplifiers are shown being summed into a fourth amplifier in *Figure 87*.

If a power amplifier were available, all four amplifiers could feed the single input of the power amplifier. For audio mixing all amplifiers are simultaneously active. Particular amplifiers can be gated OFF by making use of DC control signals which are applied to the (+) inputs to provide a channel select feature. As shown on *Figure 87*, Amp. 3 is active (as sw 3 is closed) and Amps. 1 and 2 are driven to positive output voltage saturation by the 5.1M which is applied to the (+) inputs. The DC output voltage bias level of the active amplifier is approximately 0.8 V_{DC} and could be raised if larger signal levels were to be accommodated. Frequency shaping networks can be added either to the individual amplifiers or to the common amplifier, as desired. Switching transients may need to be filtered at the DC control points if the output amplifier is active during the switching intervals.

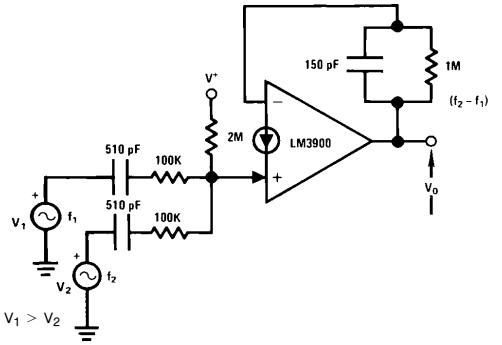


TL/H/7383–96

FIGURE 87. Audio Mixing or Selection

10.9 A LOW FREQUENCY MIXER

The diode which exists at the (+) input can be used for nonlinear signal processing. An example of this is a mixer which allows two input frequencies to produce a sum and difference frequency (in addition to other high frequency components). Using the amplifier of the LM3900, gain and filtering can also be accomplished with the same circuit in addition to the high input impedance and low output impedance advantages. The schematic of *Figure 88* shows a mixer with a gain of 10 and a low pass single pole filter (1M and 150 pF feedback elements) with a corner frequency of 1 kHz. With one signal larger in amplitude, to serve as the local oscillator input (V_1), the transconductance of the input diode is gated at this rate (f_1). A small signal (V_2) can now be added at the second input and the difference frequency is filtered from the composite resulting waveform and is made available at the output. Relatively high frequencies can be applied at the inputs as long as the desired difference frequency is within the bandwidth capabilities of the amplifier and the RC low pass filter.



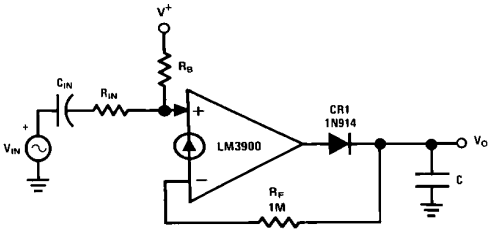
TL/H/7383–97

FIGURE 88. A Low Frequency Mixer

10.10 A PEAK DETECTOR

A peak detector is often used to rapidly charge a capacitor to the peak value of an input waveform. The voltage drop across the rectifying diode is placed within the feedback loop of an op amp to prevent voltage losses and temperature drifts in the output voltage. The LM3900 can be used as a peak detector as shown in *Figure 89*. The feedback resistor, R_f, is kept small (1 MΩ) so that the 30 nA base current will cause only a +30 mV error in V_O. This feedback resistor is constantly loading C in addition to the current drawn by the circuitry which samples V_O. These loading effects must be considered when selecting a value for C.

The biasing resistor, R_B, allows a minimum DC voltage to exist across the capacitor and the input resistor, R_{IN}, can be selected to provide gain to the input signal.



TL/H/7383–98

FIGURE 89. A Peak Detector

10.11 POWER CIRCUITS

The amplifier of the LM3900 will source a maximum current of approximately 10 mA and will sink maximum currents of approximately 80 mA (if overdriven at the (−) input). If the output is driven to a saturated state to reduce device dissipation, some interesting power circuits can be realized. These maximum values of current are typical values for the unit operating at 25°C and therefore have to be de-rated for reliable operation. For fully switched operation, amplifiers can be paralleled to increase current capability.

10.11.1 LAMP AND/OR RELAY DRIVERS (≤ 30 mA)

Low power lamps and relays (as reed relays) can be directly controlled by making use of the larger value of sink current than source current. A schematic is shown in *Figure 90* where the input resistor, R, is selected such that V_{IN} supplies at least 0.1 mA of input current.

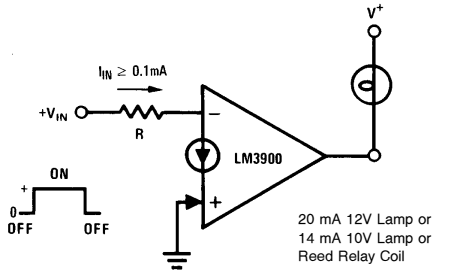


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FIGURE 90. Sinking 20 to 30 mA Loads

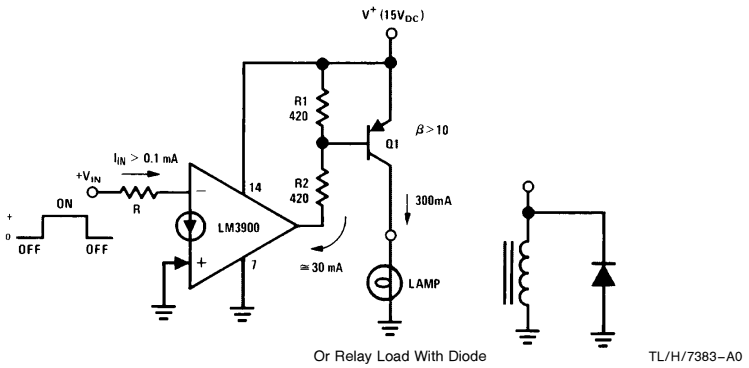


FIGURE 91. Boosting to 300 mA Loads

10.11.2 LAMP AND/OR RELAY DRIVERS ($\leq$ 300 mA)

To increase the power capability, an external transistor can be added as shown in *Figure 91*. The resistors R_1 and R_2 hold Q_1 OFF when the output of the LM3900 is high. The resistor, R_2, limits the base drive when Q_1 goes ON. It is required that pin 14 tie to the same power supply as the emitter of Q_1 to guarantee that Q_1 can be held OFF. If an inductive load is used, such as a relay coil, a backswing diode should be added to prevent large inductive voltage kicks during the switching interval, ON to OFF.

10.11.3 POSITIVE FEEDBACK OSCILLATORS

If the LM3900 is biased into the active region and a resonant circuit is connected from the output to the (+) input, a positive feedback oscillator results. A driver for a piezoelectric transducer (a warning type of noise maker) is shown in *Figure 92*. The resistors R_1 and R_2 bias the output voltage at $V^+/2$ and keep the amplifier active. Large currents can be entered into the (+) input and negative currents (or currents out of this terminal) are provided by the epi-substrate diode of the IC fabrication.

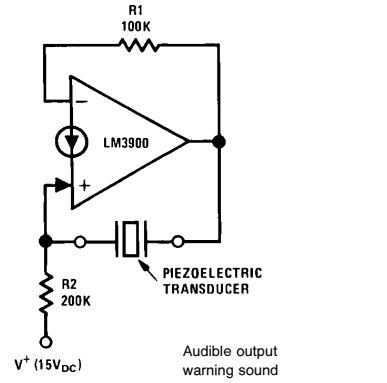


FIGURE 92. Positive Feedback Power Oscillators

When one of the amplifiers is operated in this large negative input current mode, the other amplifiers will be disturbed due to interaction. Multiple sounds may be generated as a result of using two or more transducers in various combinations, but this has not been investigated. Other two-terminal RC, RLC or piezoelectric resonators can be connected in this circuit to produce an oscillator.

10.12 HIGH VOLTAGE OPERATION

The amplifiers of the LM3900 can drive an external high voltage NPN transistor to provide a larger output voltage swing (as for an electrostatic CRT deflection system) or to operate off of an existing high voltage power supply (as the +98 V_{DC} rectified line). Examples of both types of circuits are presented in this section.

10.12.1 A HIGH VOLTAGE INVERTING AMPLIFIER

An inverting amplifier with an ouput voltage swing from essentially 0 V_{DC} to +300 V_{DC} is shown in *Figure 93*. The transistor, Q_1, must be a high breakdown device as it will have the full HV supply across it. The biasing resistor R_3 is used to center the transfer characteristic and the gain is the ratio of R_2 to R_1. The load resistor, R_L, can be increased, if desired, to reduce the HV current drain.

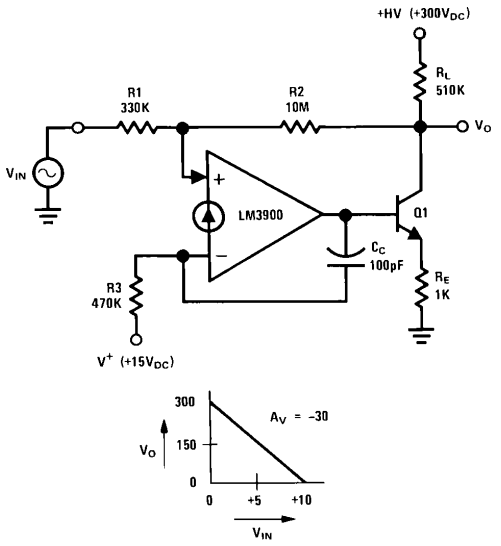
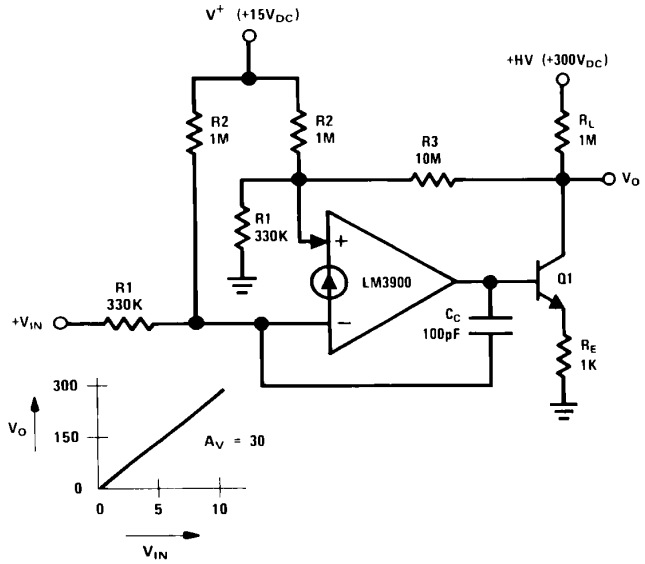


FIGURE 93. A High Voltage Inverting Amplifier



TL/H/7383–A3

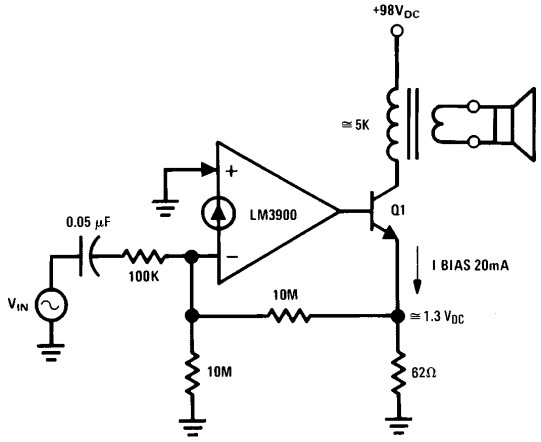
FIGURE 94. A High Voltage Non-Inverting Amplifier

10.12.2 A HIGH VOLTAGE NON-INVERTING AMPLIFIER

A high voltage non-inverting amplifier is shown in *Figure 94*. Common-mode biasing resistors (R_2) are used to allow V_{IN} to go to 0 V_{DC}. The output voltage, V_O, will not actually go to zero due to R_E, but should go to approximately 0.3 V_{DC}. Again, the gain is 30 and a range of the input voltage of from 0 to $+10$ V_{DC} will cause the output voltage to range from approximately 0 to $+300$ V_{DC}.

10.12.3 A LINE OPERATED AUDIO AMPLIFIER

An audio amplifier which operates off a $+98$ V_{DC} power supply (the rectified line voltage) is often used in consumer products. The external high voltage transistor, Q_1 of *Figure 95*, is biased and controlled by the LM3900. The magnitude of the DC biasing voltage which appears across the emitter resistor of Q_1 is controlled by the resistor which is placed from the $(-)$ input to ground.



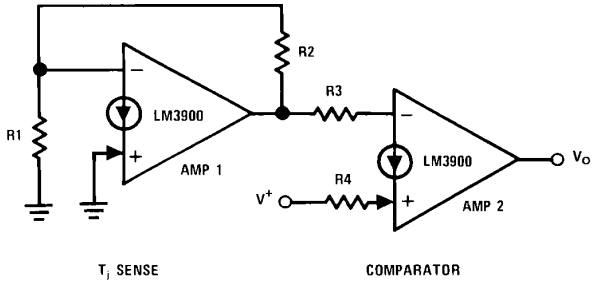
TL/H/7383–A4

FIGURE 95. A Line Operated Audio Amplifier

10.13 TEMPERATURE SENSING

The LM3900 can be used to monitor the junction temperature of the monolithic chip as shown in *Figure 96(a)*. Amp. 1 will generate an output voltage which can be designed to undergo a large negative temperature change by design of R_1 and R_2. The second amplifier compares this temperature dependent voltage with the power supply voltage and goes high at a designed maximum T_j of the IC.

For remote sensing, an NPN transistor, Q_1 of *Figure 96(b)*, is connected as an N V_{BE} generator (with R_3 and R_5) and biased via R_1 from the power supply voltage, V^+. The LM3900 again compares this temperature dependent voltage with the supply voltage and can be designed to have V_O go high at a maximum temperature of the remote temperature sensor, Q_1.



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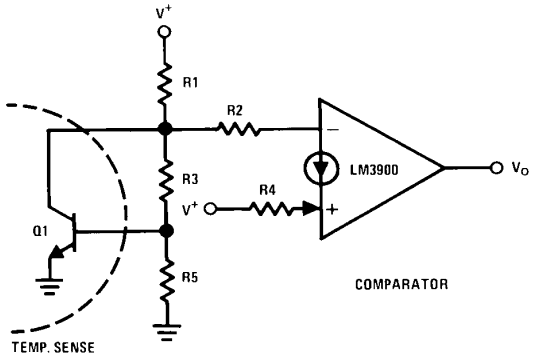
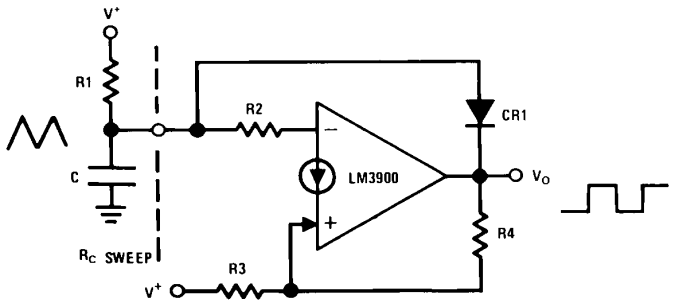
(a) IC T_j Monitor



TL/H/7383–A7

(b) Remote Temperature Sense

FIGURE 96. Temperature Sensing



TL/H/7383–A8

FIGURE 97. A "Programmable Unijunction"

10.14 A "PROGRAMMABLE UNIJUNCTION"

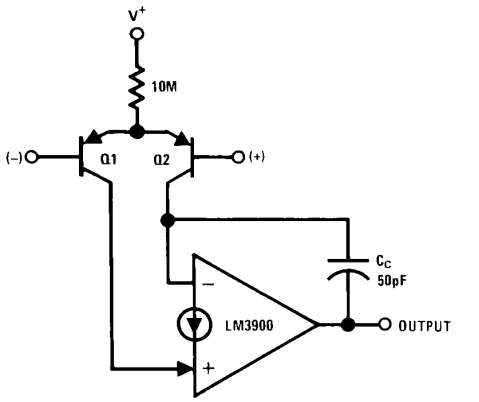
If a diode is added to the Schmitt Trigger, a "programmable unijunction" function can be obtained as shown in *Figure 97*. For a low input voltage, the output voltage of the LM3900 is high and CRI is OFF. When the input voltage rises to the high trip voltage, the output falls to essentially 0V and CRI goes ON to discharge the input capacitor, C.

The low trip voltage must be larger than approximately 1V to guarantee that the forward drop of CRI added to the output voltage of the LM3900 will be less than the low trip voltage. The discharge current can be increased by using smaller values for R_2 to provide pull-down currents larger than the 1.3 mA bias current source. The trip voltages of the Schmitt Trigger are designed as shown in section 9.7.

10.15 ADDING A DIFFERENTIAL INPUT STAGE

A differential amplifier can be added to the input of the LM3900 as shown in *Figure 98*. This will increase the gain and reduce the offset voltage. Frequency compensation can be added as shown. The BV_{EBO} limit of the input transistors must not be exceeded during a large differential input condition, or diodes and input limiting resistors should be added to restrict the input voltage which is applied to the bases of Q_1 and Q_2 to $\pm V_D$.

The input common-mode voltage range does not go exactly to ground as a few tenths of a volt are needed to guarantee that Q_1 or Q_2 will not saturate and cause a phase change (and a resulting latch-up). The input currents will be small, but could be reduced further, if desired, by using FETS for Q_1 and Q_2. This circuit can also be operated off of $\pm 15\ V_{DC}$ supplies.



TL/H/7383–A9

FIGURE 98. Adding a Differential Input Stage

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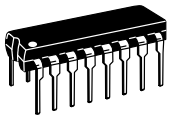
- Low Drain Current (3.0 mA (Typical) @ V_{CC} = 6.0 Vdc)
- Excellent Sensitivity: Input Limiting Voltage – (– 3.0 dB) = 5.0 μV (Typical)
- Low Number of External Parts Required
- Recommend MC3372 for Replacement/Upgrade

LOW POWER FM IF

SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 648

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

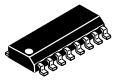
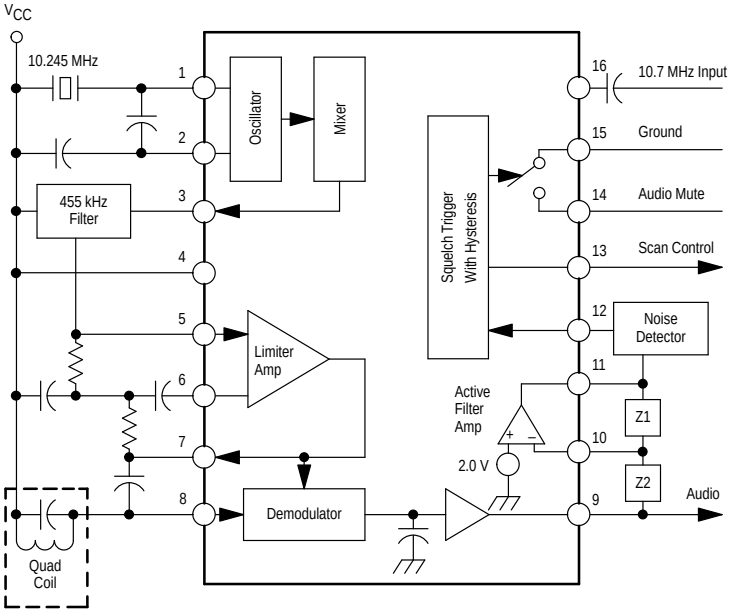
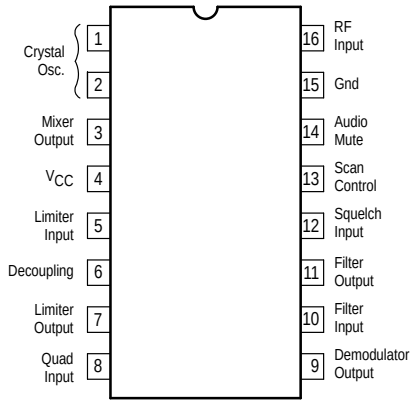


Figure 1. Representative Block Diagram



PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3357D	T_A = – 30 to +70°C	SO–16
MC3357P		Plastic DIP

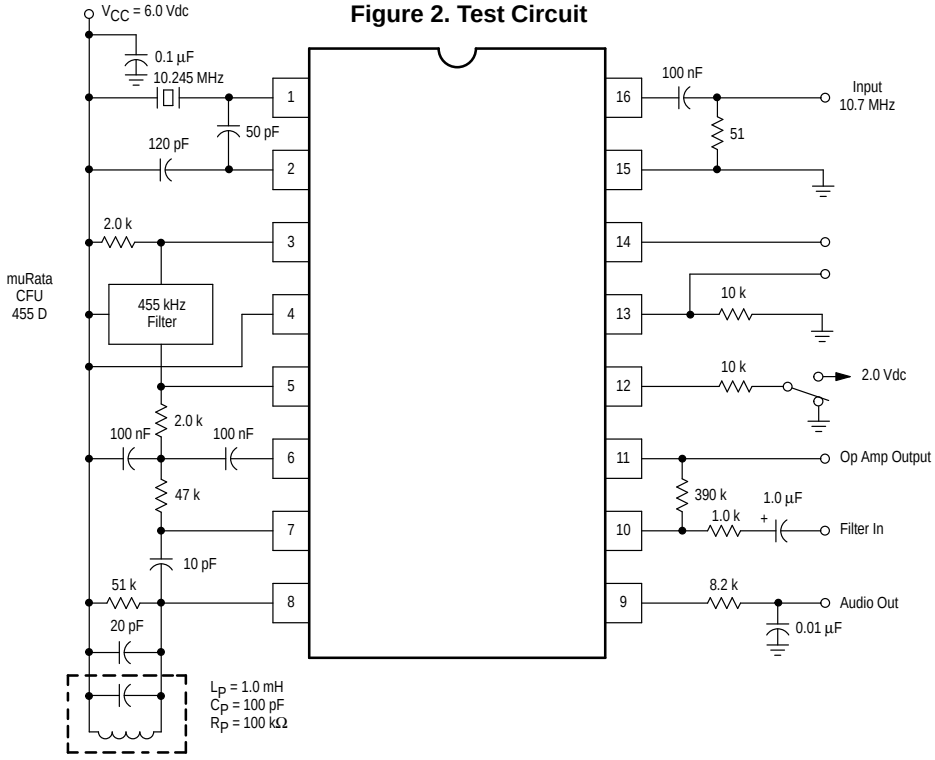
MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}(max)	12	Vdc
Operating Supply Voltage Range	4	V_{CC}	4 to 8	Vdc
Detector Input Voltage	8	–	1.0	Vp–p
Input Voltage ($V_{CC} \geqslant$ 6.0 Volts)	16	V_{16}	1.0	V_{RMS}
Mute Function	14	V_{14}	–0.5 to 5.0	V_{pk}
Junction Temperature	–	T_J	150	°C
Operating Ambient Temperature Range	–	T_A	– 30 to + 70	°C
Storage Temperature Range	–	T_{stg}	– 65 to + 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 6.0 Vdc, fo = 10.7 MHz, $\Delta f = \pm$ 3.0 kHz, f_{mod} = 1.0 kHz, T_A = 25°C, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Drain Current Squelch Off Squelch On	4	– –	2.0 3.0	– 5.0	mA
Input Limiting Voltage (– 3 dB Limiting)	16	–	5.0	10	µV
Detector Output Voltage	9	–	3.0	–	Vdc
Detector Output Impedance	–	–	400	–	Ω
Recovered Audio Output Voltage (V_{in} = 10 mV)	9	200	350	–	mVrms
Filter Gain (10 kHz) (V_{in} = 5 mV)	–	40	46	–	dB
Filter Output Voltage	11	1.8	2.0	2.5	Vdc
Trigger Hysteresis	–	–	100	–	mV
Mute Function Low	14	–	15	50	Ω
Mute Function High	14	1.0	10	–	MΩ
Scan Function Low (Mute Off) (V_{12} = 2 Vdc)	13	–	0	0.5	Vdc
Scan Function High (Mute On) (V_{12} = Gnd)	13	5.0	–	–	Vdc
Mixer Conversion Gain	3	–	20	–	dB
Mixer Input Resistance	16	–	3.3	–	kΩ
Mixer Input Capacitance	16	–	2.2	–	pF

Figure 2. Test Circuit



CIRCUIT DESCRIPTION

The MC3357 is a low power FM IF circuit designed primarily for use in voice communication scanning receivers.

The mixer–oscillator combination converts the input frequency (e.g., 10.7 MHz) down to 455 kHz, where, after external bandpass filtering, most of the amplification is done. The audio is recovered using a conventional quadrature FM detector. The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This “noise band” is monitored by an active filter and a detector. A squelch trigger circuit indicates the presence of a noise (or a tone) by an output which can be used to control scanning. At the same time, an internal switch is operated which can be used to mute the audio.

The oscillator is an internally–biased Colpitts type with the collector, base, and emitter connections at Pins 4, 1, and 2 respectively. A crystal can be used in place of the usual coil.

The mixer is doubly–balanced to reduce spurious responses. The input impedance at Pin 16 is set by a 3.0 kΩ internal biasing resistor and has low capacitance, allowing the circuit to be preceded by a crystal filter. The collector output at Pin 3 must be dc connected to B +, below which it can swing 0.5 V.

After suitable bandpass filtering (ceramic or LC), the signal goes to the input of a five–stage limiter at Pin 5. The output of the limiter at Pin 7 drives a multiplier, both internally directly, and externally through a quadrature coil, to detect the FM. The output at Pin 7 is also used to supply dc feedback to Pin 5. The other side of the first limiter stage is decoupled at Pin 6.

The recovered audio is partially filtered, then buffered, giving an impedance of around 400 Ω at Pin 9. The signal still requires de–emphasis, volume control and further amplification before driving a loudspeaker.

A simple inverting op amp is provided with an output at Pin 11 providing dc bias (externally) to the input at Pin 10 which is referred internally to 2.0 V. A filter can be made with external impedance elements to discriminate between frequencies. With an external AM detector, the filtered audio signal can be checked for the presence of noise above the normal audio band, or a tone signal. This information is applied to Pin 12.

An external positive bias to Pin 12 sets up the squelch trigger circuit such that Pin 13 is low at an impedance level of around 60 kΩ, and the audio mute (Pin 14) is open circuit. If Pin 12 is pulled down to 0.7 V by the noise or tone detector, Pin 13 will rise to approximately 0.5 Vdc below supply where it can support a load current of around 500 µA and Pin 14 is internally short–circuited to ground. There is 100 mV of hysteresis at Pin 12 to prevent jitter. Audio muting is accomplished by connecting Pin 14 to a high–impedance ground–reference point in the audio path between Pin 9 and the audio amplifier.

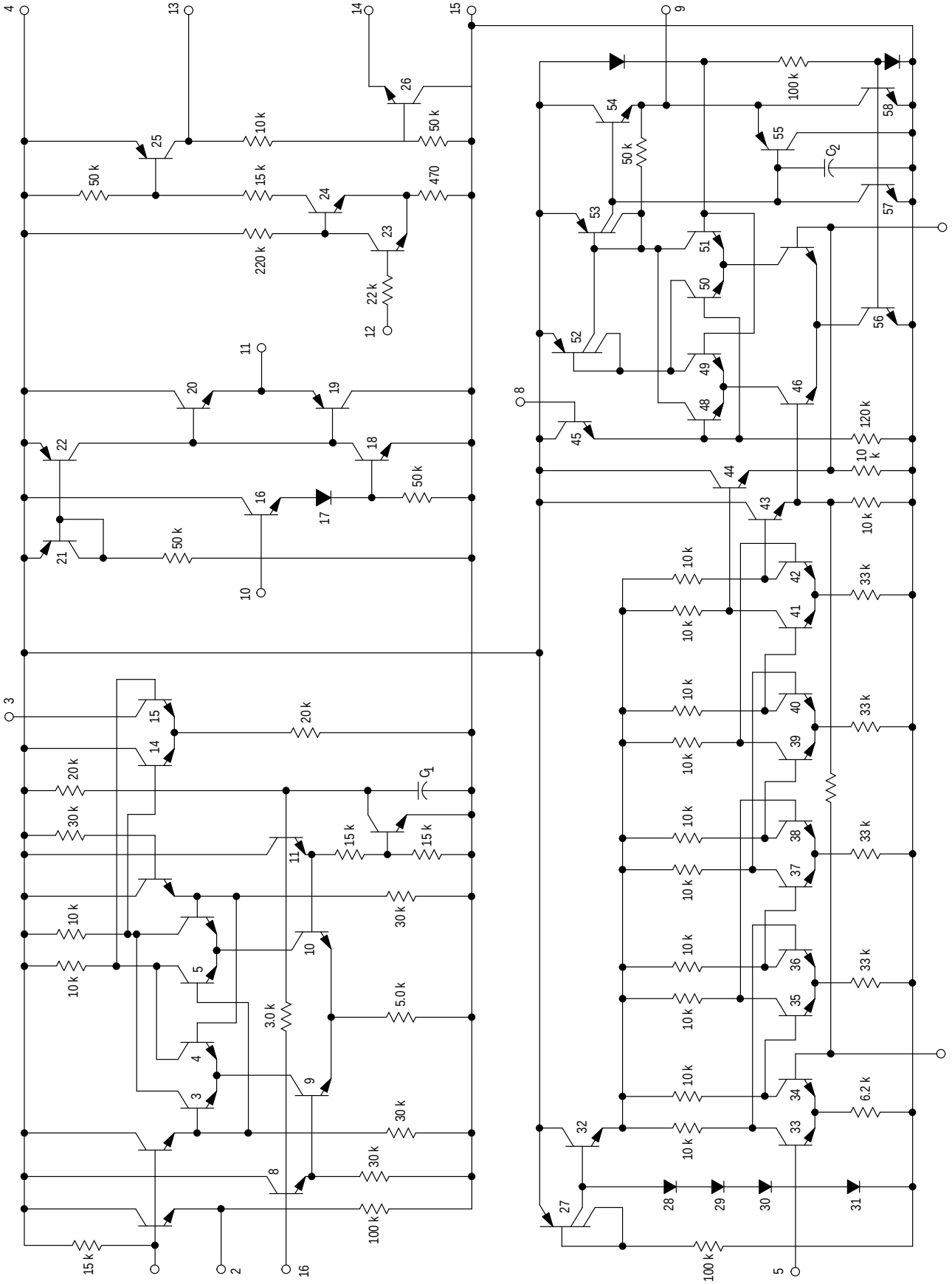
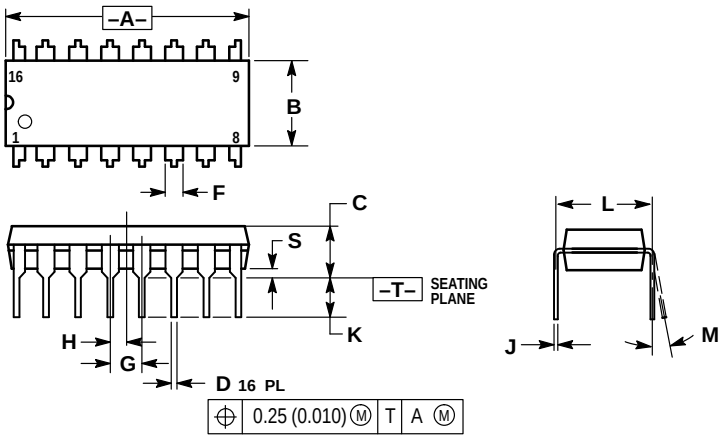


Figure 3. Circuit Schematic

OUTLINE DIMENSIONS

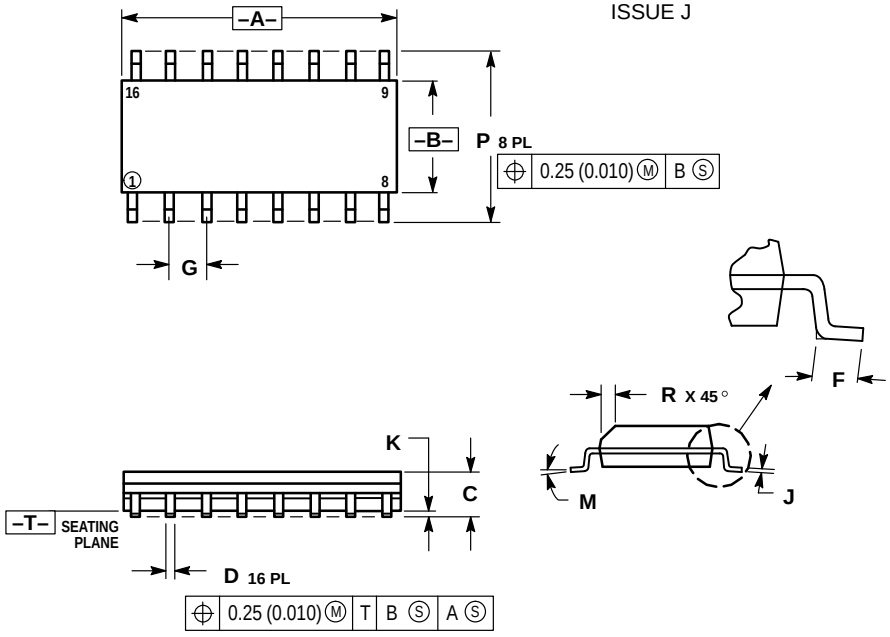
P SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

D SUFFIX
PLASTIC PACKAGE
CASE 751B–05
(SO–16)
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

How to reach us:
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MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

Technical Data

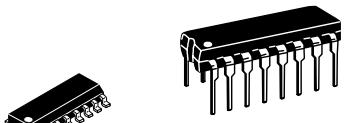
MC145170-2/D
Rev. 4, 02/2003

PLL Frequency Synthesizer with Serial Interface

MOTOROLA
intelligence everywhere™

digital dna™

MC145170-2



D SUFFIX
CASE 751B

P SUFFIX
CASE 648

DT SUFFIX
CASE 948C

Ordering Information

Device	Operating Temp Range	Package
MC145170P2	T_A = -40 to 85°C	Plastic DIP
MC145170D2		SOG-16
MC145170DT2		TSSOP-16

Contents:

1 Introduction

The new MC145170-2 is pin-for-pin compatible with the MC145170-1. A comparison of the two parts is shown in the table below. The MC145170-2 is recommended for new designs and has a more robust power-on reset (POR) circuit that is more responsive to momentary power supply interruptions. The two devices are actually the same chip with mask options for the POR circuit. The more robust POR circuit draws approximately 20 µA additional supply current. Note that the maximum specification of 100 µA quiescent supply current has not changed.

The MC145170-2 is a single-chip synthesizer capable of direct usage in the MF, HF, and VHF bands. A special architecture makes this PLL easy to program. Either a bit- or byte-oriented format may be used. Due to the patented BitGrabber™ registers, no address/steering bits are required for *random access* of the three registers. Thus, tuning can be accomplished via a 2-byte serial transfer to the 16-bit N register.

The device features fully programmable R and N counters, an amplifier at the f_{in} pin, on-chip support of an external crystal, a programmable reference output, and both single- and double-ended phase detectors with linear transfer functions (no dead zones). A configuration (C) register allows the part to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing noise and interference.

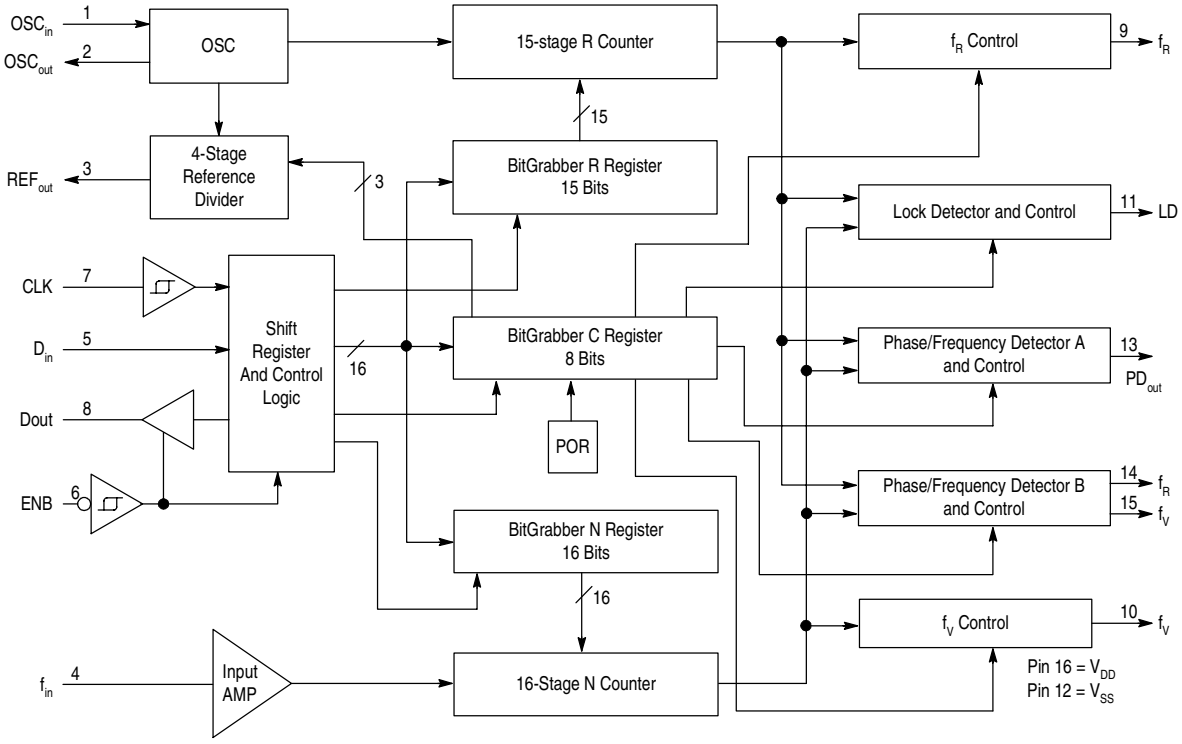
In order to reduce lock times and prevent erroneous data from being loaded into the counters, a patented jam-load feature is included. Whenever a new divide ratio is loaded into the N register, both the N and R counters are jam-loaded with their respective values and begin counting down together. The phase detectors are also initialized during the jam load.

- Operating Voltage Range: 2.7 to 5.5 V

- Maximum Operating Frequency:
  185 MHz @ V_{in} = 500 mVpp, 4.5 V Minimum Supply
  100 MHz @ V_{in} = 500 mVpp, 3.0 V Minimum Supply
- Operating Supply Current:
  0.6 mA @ 3.0 V, 30 MHz
  1.5 mA @ 3.0 V, 100 MHz
  3.0 mA @ 5.0 V, 50 MHz
  5.8 mA @ 5.0 V, 185 MHz
- Operating Temperature Range: -40 to 85°C
- R Counter Division Range: 1 and 5 to 32,767
- N Counter Division Range: 40 to 65,535
- Direct Interface to Motorola SPI Serial Data Port
- See Application Notes AN1207/D and AN1671/D
- Contact Motorola for MC145170 control software.

Table 1. Comparision of the PLL Frequency Synthesizers

Parameter	MC145170-2	MC145170-1
Minimum Supply Voltage	2.7 V	2.5 V
Maximum Input Current, f_{in}	150 µA	120 µA
Dynamic Characteristics, f_{in} (Figure 26)	Unchanged	-
Power-On Reset Circuit	Improved	-



This device contains 4,800 active transistors.

Figure 1. Block Diagram

2 Electrical Characteristics

Table 2. Maximum Ratings (Voltages Referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to 5.5	V
DC Input Voltage	V_{in}	-0.5 to V_{DD} + 0.5	V
DC Output Voltage	V_{out}	-0.5 to V_{DD} + 0.5	V
DC Input Current, per Pin	I_{in}	±10	mA
DC Output Current, per Pin	I_{out}	±20	mA
DC Supply Current, V_{DD} and V_{SS} Pins	I_{DD}	±30	mA
Power Dissipation, per Package	P_D	300	mW
Storage Temperature	T_{stg}	-65 to 150	°C
Lead Temperature, 1 mm from Case for 10 seconds	T_L	260	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.
2. ESD data available upon request.

Electrical Characteristics

Table 3. Electrical Characteristics (Voltages Referenced to V_{SS}, T_A = -40 to 85°C)

Parameter	Test Condition	Symbol	V_{DD} V	Guaranteed Limit	Unit
Power Supply Voltage Range		V_{DD}	-	2.7 to 5.5	V
Maximum Low-Level Input Voltage [Note 1] (D_{in}, CLK, $\overline{ENB}$, f_{in})	dc Coupling to f_{in}	V_{IL}	2.7 4.5 5.5	0.54 1.35 1.65	V
Minimum High-Level Input Voltage [Note 1] (D_{in}, CLK, $\overline{ENB}$, f_{in})	dc Coupling to f_{in}	V_{IH}	2.7 4.5 5.5	2.16 3.15 3.85	V
Minimum Hysteresis Voltage (CLK, $\overline{ENB}$)		V_{Hys}	2.7 5.5	0.15 0.20	V
Maximum Low-Level Output Voltage (Any Output)	I_{out} = 20 μA	V_{OL}	2.7 5.5	0.1 0.1	V
Minimum High-Level Output Voltage (Any Output)	I_{out} = - 20 μA	V_{OH}	2.7 5.5	2.6 5.4	V
Minimum Low-Level Output Current (PD_{out}, REF_{out}, f_R, f_V, LD, ϕ_R, ϕ_V)	V_{out} = 0.3 V V_{out} = 0.4 V V_{out} = 0.5 V	I_{OL}	2.7 4.5 5.5	0.12 0.36 0.36	mA
Minimum High-Level Output Current (PD_{out}, REF_{out}, f_R, f_V, LD, ϕ_R, ϕ_V)	V_{out} = 2.4 V V_{out} = 4.1 V V_{out} = 5.0 V	I_{OH}	2.7 4.5 5.5	-0.12 -0.36 -0.36	mA
Minimum Low-Level Output Current (D_{out})	V_{out} = 0.4 V	I_{OL}	4.5	1.6	mA
Minimum High-Level Output Current (D_{out})	V_{out} = 4.1 V	I_{OH}	4.5	-1.6	mA
Maximum Input Leakage Current (D_{in}, CLK, $\overline{ENB}$, OSC_{in})	V_{in} = V_{DD} or V_{SS}	I_{in}	5.5	±1.0	μA
Maximum Input Current (f_{in})	V_{in} = V_{DD} or V_{SS}	I_{in}	5.5	±150	μA
Maximum Output Leakage Current (PD_{out}) (D_{out})	V_{in} = V_{DD} or V_{SS}, Output in High-Impedance State	I_{OZ}	 5.5 5.5	 ±100 ±5.0	 nA μA
Maximum Quiescent Supply Current	V_{in} = V_{DD} or V_{SS}; Outputs Open; Excluding f_{in} Amp Input Current Component	I_{DD}	5.5	100	μA

NOTES: 1. When dc coupling to the OSC_{in} pin is used, the pin must be driven rail-to-rail. In this case, OSC_{out} should be floated.

2. The nominal values at 3.0 V are 0.6 mA @ 30 MHz, and 1.5 mA @ 100 MHz. The nominal values at 5.0 V are 3.0 mA @ 50 MHz, and 5.8 mA @ 185 MHz. These are not guaranteed limits.

Table 3. Electrical Characteristics (Continued) (Voltages Referenced to V_{SS}, T_A = -40 to 85°C)

Parameter	Test Condition	Symbol	V_{DD} V	Guaranteed Limit	Unit
Maximum Operating Supply Current	f_{in} = 500 mVpp; OSC_{in} = 1.0 MHz @ 1.0 Vpp; LD, f_R, f_V, REF_{out} = Inactive and No Connect; OSC_{out}, ϕ_V, ϕ_R, PD_{out} = No Connect; D_{in}, ENB, CLK = V_{DD} or V_{SS}	I_{dd}	-	[Note 2]	mA

NOTES: 1. When dc coupling to the OSC_{in} pin is used, the pin must be driven rail-to-rail. In this case, OSC_{out} should be floated.
2. The nominal values at 3.0 V are 0.6 mA @ 30 MHz, and 1.5 mA @ 100 MHz. The nominal values at 5.0 V are 3.0 mA @ 50 MHz, and 5.8 mA @ 185 MHz. These are not guaranteed limits.

Table 4. AC Interface Characteristics

(T_A = -40 to 85°C, C_L = 50 pF, Input tr = t_f = 10 ns, unless otherwise noted.)

Parameter	Symbol	Figure No.	V_{DD} V	Guaranteed Limit	Unit
Serial Data Clock Frequency (Note: Refer to Clock t_w Below)	f_{clk}	2	2.7 4.5 5.5	dc to 3.0 dc to 4.0 dc to 4.0	MHz
Maximum Propagation Delay, CLK to D_{out}	t_{PLH}, t_{PHL}	2, 6	2.7 4.5 5.5	150 85 85	ns
Maximum Disable Time, D_{out} Active to High Impedance	t_{PLZ}, t_{PHZ}	3, 7	2.7 4.5 5.5	300 200 200	ns
Access Time, D_{out} High Impedance to Active	t_{PZL}, t_{PZH}	3, 7	2.7 4.5 5.5	0 to 200 0 to 100 0 to 100	ns
Maximum Output Transition Time, D_{out} CL = 50 pF	t_{TLH}, t_{THL}	2, 6	2.7 4.5 5.5	150 50 50	ns
CL = 200 pF		2, 6	2.7 4.5 5.5	900 150 150	ns
Maximum Input Capacitance - D_{in}, $\overline{ENB}$, CLK	C_{in}		-	10	pF
Maximum Output Capacitance - D_{out}	C_{out}		-	10	pF

Table 5. Timing Requirements (T_A = -40 to 85°C, Input $t_r = t_f$ = 10 ns, unless otherwise noted.)

Parameter	Symbol	Figure No.	V_{DD} V	Guaranteed Limit	Unit
Minimum Setup and Hold Times, D_{in} vs CLK	t_{su}, t_h	4	2.7 4.5 5.5	55 40 40	ns
Minimum Setup, Hold, and Recovery Times, $\overline{ENB}$ vs CLK	t_{su}, t_h, t_{rec}	5	2.7 4.5 5.5	135 100 100	ns
Minimum Inactive-High Pulse Width, $\overline{ENB}$	$t_{w(H)}$	5	2.7 4.5 5.5	400 300 300	ns
Minimum Pulse Width, CLK	t_w	2	2.7 4.5 5.5	166 125 125	ns
Maximum Input Rise and Fall Times, CLK	t_r, t_f	2	2.7 4.5 5.5	100 100 100	µs

2.1 Switching Waveforms

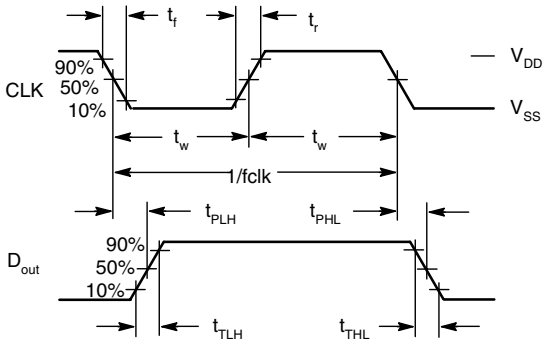


Figure 2.

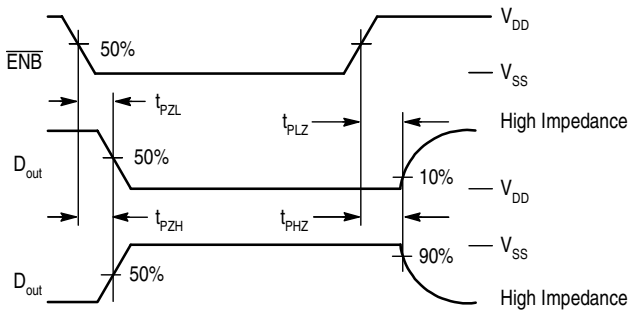


Figure 3.

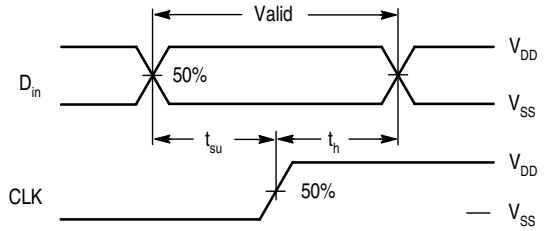


Figure 4.

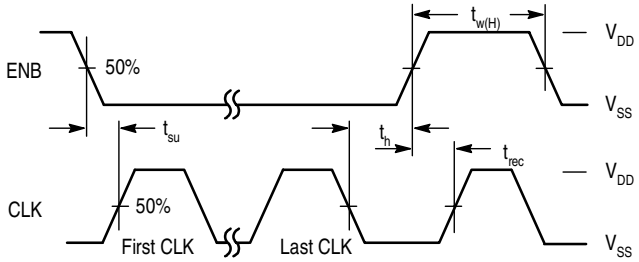
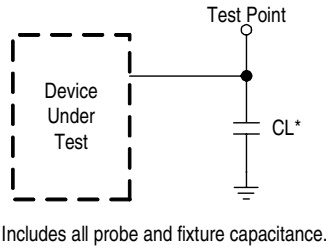
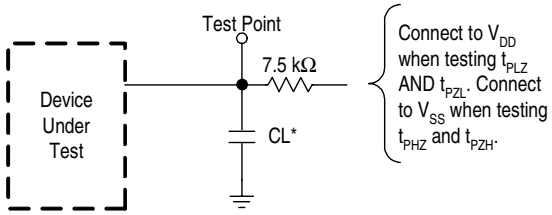


Figure 5.



* Includes all probe and fixture capacitance.

Figure 6. Test Circuit



*Includes all probe and fixture capacitance.

Figure 7. Test Circuit

Table 6. Loop Specifications (T_A = -40 to 85°C)

Parameter	Test Condition	Symbol	Figure No.	V_{DD} V	Guaranteed Range		Unit
					Min	Max	
Input Frequency, f_{in} [Note}	$V_{in} \geq$ 500 mVpp Sine Wave, N Counter Set to Divide Ratio Such that $f_V \leq$ 2.0 MHz	f	8	2.7 3.0 4.5 5.5	5.0 5.0 25 45	80 100 185 185	MHz
Input Frequency, OSC_{in} Externally Driven with ac-coupled Signal	$V_{in} \geq$ 1.0 V_{pp} Sine Wave, OSC_{out} = No Connect, R Counter Set to Divide Ratio Such that $f_R \leq$ 2 MHz	f	9	2.7 3.0 4.5 5.5	1.0* 1.0* 1.0* 1.0*	22 25 30 35	MHz
Crystal Frequency, OSC_{in} and OSC_{out}	C1 ≤ 30 pF C2 ≤ 30 pF Includes Stray Capacitance	f_{XTAL}	11	2.7 3.0 4.5 5.5	2.0 2.0 2.0 2.0	12 12 15 15	MHz
Output Frequency, REF_{out}	C_L = 30 pF	f_{out}	12, 14	2.7 4.5 5.5	dc dc dc	- 10 10	MHz
Operating Frequency of the Phase Detectors		f		2.7 4.5 5.5	dc dc dc	- 2.0 2.0	MHz
Output Pulse Width, ϕ_R, ϕ_V, and LD	f_R in Phase with f_V C_L = 50 pF	t_w	13, 14	2.7 4.5 5.5	- 20 16	- 100 90	ns
Output Transition Times, ϕ_R, ϕ_V, LD, f_R, and f_V	C_L = 50 pF	t_{TLH}, t_{THL}	13, 14	2.7 4.5 5.5	- - -	- 65 60	ns
Input Capacitance f_{in} OSC_{in}		C_{in}	- -	- -	- -	7.0 7.0	pF

* IF lower frequency is desired, use wave shaping or higher amplitude sinusoidal signal in ac-coupled case. Also, see Figure 25 for dc coupling.

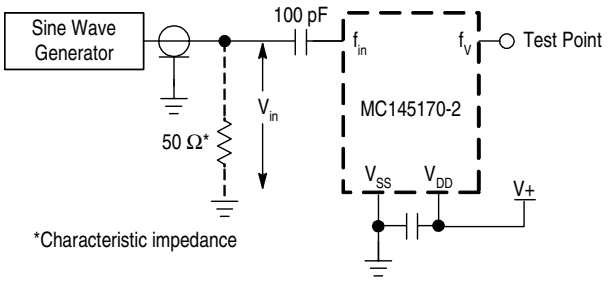


Figure 8. Test Circuit, f_{in}

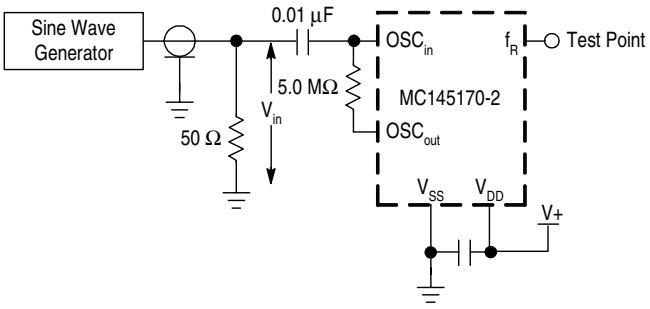


Figure 9. Test Circuit, OSC Circuitry Externally Driven [Note]

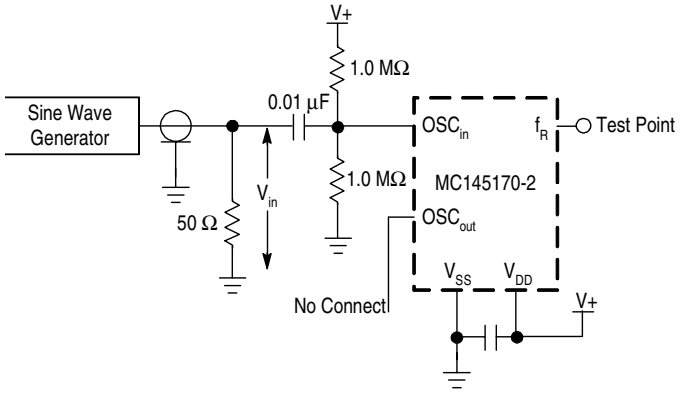


Figure 10. Circuit to Eliminate Self-Oscillation, OSC Circuitry Externally Driven [Note]

NOTE: Use the circuit of Figure 10 to eliminate self-oscillation of the OSCin pin when the MC145170-2 has power applied with no external signal applied at Vin. (Self-oscillation is not harmful to the MC145170-2 and does not damage the IC.)

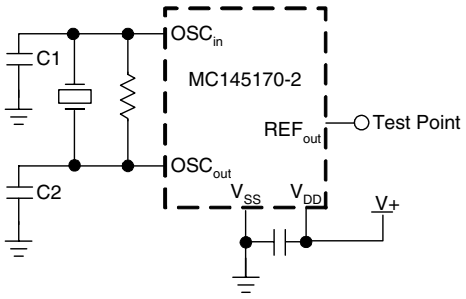


Figure 11. Test Circuit, OSC Circuit with Crystal

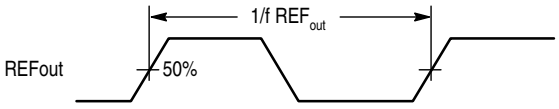


Figure 12. Test Circuit

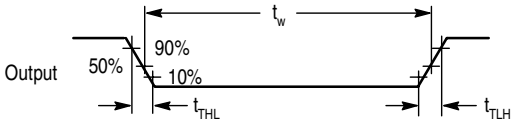


Figure 13. Switching Waveform

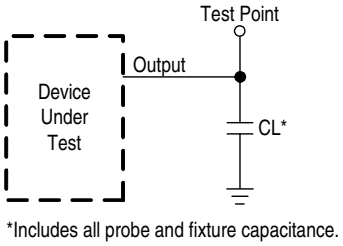


Figure 14. Test Load Circuit

3 Pin Connections

3.1 Digital Interface Pins

D_{in}
Serial Data Input (Pin 5)

The bit stream begins with the most significant bit (MSB) and is shifted in on the low-to-high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the N register, or 3 bytes (24 bits) to access the R register. Additionally, the R register can be accessed with a 15-bit transfer (see Table 7). An optional pattern which resets the device is shown in Figure 15. The values in the C, N, and R registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{ENB}$.

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided (i.e., the registers may be accessed in any sequence). Data is retained in the registers over a supply range of 2.7 to 5.5 V. The formats are shown in Figures 15, 16, 17, and 18.

D_{in} typically switches near 50% of V_{DD} to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail-to-rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull-up resistor of 1 to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst-case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 7. Register Access
(MSBs are shifted in first, C0, N0, and R0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
9 to 13	See Figure 15	(Reset)
8	C Register	C7, C6, C5, …, C0
16	N Register	N15, N14, N13, …, N0
15 or 24	R Register	R14, R13, R12, …, R0
Other Values ≤ 32	None	
Values > 32	See Figures 27 to 34	

CLK
Serial Data Clock Input (Pin 7)

Low-to-high transitions on Clock shift bits available at D_{in}, while high-to-low transitions shift bits from D_{out}. The chip's 16-1/2-stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Four to eight clock cycles followed by five clock cycles are needed to reset the device; this is optional. Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the N register. Either 15 or 24 cycles can be used to access the R register (see Table 7 and Figures 15, 16, 17, and 18). For cascaded devices, see Figures 27 to 34.

CLK typically switches near 50% of V_{DD} and has a Schmitt-triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of **D_{in}** for more information.

NOTE: To guarantee proper operation of the power-on reset (POR) circuit, the CLK pin must be held at the potential of either the V_{SS} or V_{DD} pin during power up. That is, the CLK input should not be floated or toggled while the V_{DD} pin is ramping from 0 to at least 2.7 V. If control of the CLK pin is not practical during power up, the initialization sequence shown in Figure 15 must be used.

$\overline{ENB}$
Active-Low Enable Input (Pin 6)

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{ENB}$ is in an inactive high state, shifting is inhibited, D_{out} is forced to the high-impedance state, and the port is held in the initialized state. To transfer data to the device, $\overline{ENB}$ (which must start inactive high) is taken low, a serial transfer is made via Din and CLK, and ENB is taken back high. The low-to-high transition on $\overline{ENB}$ transfers data to the C, N, or R register depending on the data stream length per Table 7.

NOTE: Transitions on $\overline{ENB}$ must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs when $\overline{ENB}$ is high and CLK is low.

This input is also Schmitt-triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of D_{in} for more information.

D_{out}
Three-State Serial Data Output (Pin 8)

Data is transferred out of the 16-1/2-stage shift register through Dout on the high-to-low transition of CLK. This output is a No Connect, unless used in one of the manners discussed below.

Dout could be fed back to an MCU/MPU to perform a wrap-around test of serial data. This could be part of a system check conducted at power up to test the integrity of the system's processor, PC board traces, solder joints, etc.

The pin could be monitored at an in-line QA test during board manufacturing.

Finally, D_{out} facilitates troubleshooting a system and permits cascading devices.

3.2 Reference Pins

OSC_{in}/OSC_{out}
Reference Oscillator Input/Output (Pins 1, 2)

These pins form a reference oscillator when connected to terminals of an external parallel-resonant crystal. Frequency-setting capacitors of appropriate values as recommended by the crystal supplier are connected from each pin to ground (up to a maximum of 30 pF each, including stray capacitance). An external feedback resistor of 1.0 to 5.0 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The required connections for the components are shown in Figure 11.

5 MΩ is required across the OSC_{in} and OSC_{out} pins in the ac-coupled case (see Figure 9 or alternate circuit Figure 10). *OSC_{out} is an internal node on the device and should not be used to drive any loads* (i.e., OSC_{out} is unbuffered). However, the buffered REF_{out} is available to drive external loads.

The external signal level must be at least 1 Vpp; the maximum frequencies are given in the **Loop Specifications** table. These maximum frequencies apply for R Counter divide ratios as indicated in the table. For very small ratios, the maximum frequency is limited to the divide ratio times 2 MHz. (Reason: the phase/frequency detectors are limited to a maximum input frequency of 2 MHz.)

If an external source is available which swings virtually rail-to-rail (V_{DD} to V_{SS}), then dc coupling can be used. In the dc-coupled case, no external feedback resistor is needed. OSC_{out} must be a No Connect to avoid loading an internal node on the device, as noted above. *For frequencies below 1 MHz, dc coupling must be used.* The R counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the OSC_{in} pin. See Figure 25.

Each rising edge on the OSC_{in} pin causes the R counter to decrement by one.

REF_{out}
Reference Frequency Output (Pin 3)

This output is the buffered output of the crystal-generated reference frequency or externally provided reference source. This output may be enabled, disabled, or scaled via bits in the C register (see Figure 16).

REF_{out} can be used to drive a microprocessor clock input, thereby saving a crystal. Upon power up, the on-chip power-on-initialize circuit forces REF_{out} to the OSC_{in} divided-by-8 mode.

REF_{out} is capable of operation to 10 MHz; see the **Loop Specifications** table. Therefore, divide values for the reference divider are restricted to two or higher for OSC_{in} frequencies above 10 MHz.

If unused, the pin should be floated and should be disabled via the C register to minimize dynamic power consumption and electromagnetic interference (EMI).

3.3 Counter Output Pins

f_R
R Counter Output (Pin 9)

This signal is the buffered output of the 15-stage R counter. f_R can be enabled or disabled via the C register (patented). The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The f_R signal can be used to verify the R counter's divide ratio. This ratio extends from 5 to 32,767 and is determined by the binary value loaded into the R register. Also, direct access to the phase detector via the OSC_{in} pin is allowed by choosing a divide value of 1 (see Figure 17). The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of f_R must not exceed 2 MHz.

When activated, the f_R signal appears as normally low and pulses high. The pulse width is 4.5 cycles of the OSC_{in} pin signal, except when a divide ratio of 1 is selected. When 1 is selected, the OSC_{in} signal is buffered and appears at the f_R pin.

f_V
N Counter Output (Pin 10)

This signal is the buffered output of the 16-stage N counter. f_V can be enabled or disabled via the C register (patented). The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The f_V signal can be used to verify the N counter's divide ratio. This ratio extends from 40 to 65,535 and is determined by the binary value loaded into the N register. The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of f_V must not exceed 2 MHz.

When activated, the f_V signal appears as normally low and pulses high.

3.4 Loop Pins

f_{in}
Frequency Input (Pin 4)

This pin is a frequency input from the VCO. This pin feeds the on-chip amplifier which drives the N counter. This signal is normally sourced from an external voltage-controlled oscillator (VCO), and is ac-coupled into f_{in}. A 100 pF coupling capacitor is used for measurement purposes and is the minimum size recommended for applications (see Figure 25). The frequency capability of this input is dependent on the supply voltage as listed in Table 6, Loop Specifications. For small divide ratios, the maximum frequency is limited to the divide ratio times 2 MHz. (Reason: the phase/frequency detectors are limited to a maximum frequency of 2 MHz.)

For signals which swing from at least the V_{IL} to V_{IH} levels listed in the **Electrical Characteristics** table, dc coupling may be used. Also, for low frequency signals (less than the minimum frequencies shown in the **Loop Specifications** table), dc coupling is a requirement. The N counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the f_{in} pin. See Figure 25.

Each rising edge on the f_{in} pin causes the N counter to decrement by 1.

PD_{out}
Single-Ended Phase/Frequency Detector Output (Pin 13)

This is a three-state output for use as a loop error signal when combined with an external low-pass filter. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/ frequency detector is described below and is shown in Figure 19.

POL bit (C7) in the C register = low (see Figure 16)

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: negative pulses from high impedance

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: positive pulses from high impedance

Frequency and Phase of $f_V = f_R$: essentially high-impedance state; voltage at pin determined by loop filter

POL bit (C7) = high

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: positive pulses from high impedance

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: negative pulses from high impedance

Frequency and Phase of $f_V = f_R$: essentially high-impedance state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD_{out} can be forced to the high-impedance state by utilization of the disable feature in the C register (patented).

ϕ_R and ϕ_V
Double-Ended Phase/Frequency Detector Outputs
(Pins 14, 15)

These outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 19.

POL bit (C7) in the C register = low (see Figure 16)

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

POL bit (C7) = high

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via the C register (patented).

LD
Lock Detector Output (Pin 11)

This output is essentially at a high level with narrow low-going pulses when the loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies (see Figure 19).

This output can be enabled and disabled via the C register (patented). Upon power up, on-chip initialization circuitry disables LD to a static low logic level to prevent a false “lock” signal. If unused, LD should be disabled and left open.

3.5 Power Supply

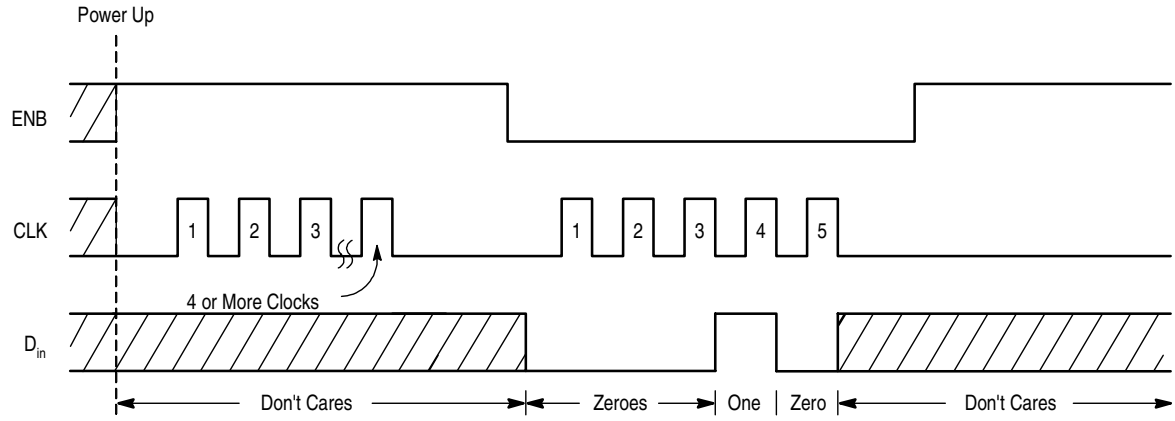
V_{DD}
Most Positive Supply Potential (Pin 16)

This pin may range from 2.7 to 5.5 V with respect to V_{SS}.

For optimum performance, V_{DD} should be bypassed to V_{SS} using low-inductance capacitor(s) mounted very close to the device. Lead lengths on the capacitor(s) should be minimized. (The very fast switching speed of the device causes current spikes on the power leads.)

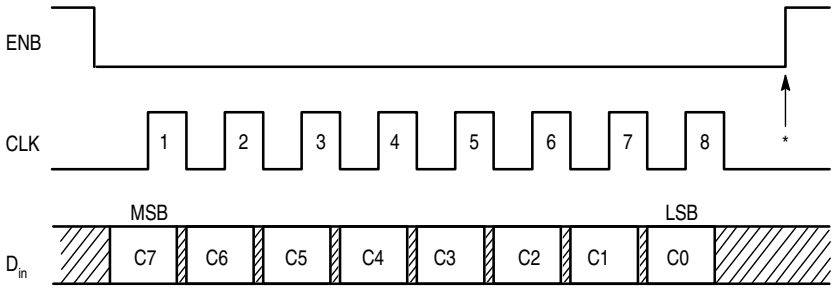
V_{SS}
Most Negative Supply Potential (Pin 12)

This pin is usually ground. For measurement purposes, the V_{SS} pin is tied to a ground plane.



NOTE: This initialization sequence is usually not necessary because the on-chip power-on reset circuit performs the initialization function. However, this initialization sequence must be used immediately after power up if control of the CLK pin is not possible. That is, if CLK (Pin 7) toggles or floats upon power up, use the above sequence to reset the device. Also, use this sequence if power is momentarily interrupted such that the supply voltage to the device is reduced to below 2.7 V, but not down to at least 1 V (for example, the supply drops down to 2 V). This is necessary because the on-chip power-on reset is only activated when the supply ramps up from a voltage below approximately 1.0 V.

Figure 15. Reset Sequence



* At this point, the new byte is transferred to the C register and stored. No other registers are affected.

C7 - POL:

Select the output polarity of the phase/frequency detectors. When set high, this bit inverts PD_{out} and interchanges the ϕ_R function with ϕ_V as depicted in Figure 19. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

C6 - PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A (PD_{out}) and disables phase/frequency detector B by forcing ϕ_R and ϕ_V to the static high state. When cleared low, phase/frequency detector B is enabled (ϕ_R and ϕ_V) and phase/frequency detector A is disabled with PD_{out} forced to the high-impedance state. This bit is cleared low at power up.

C5 - LDE: Enables the lock detector output when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power up.

C4 - C2, OSC2 - OSC0:

Reference output controls which determines the REF_{out} characteristics as shown below. Upon power up, the bits are initialized such that $OSC_{in}/8$ is selected.

C4	C3	C2	REF_{out} Frequency
0	0	0	dc (Static Low)
0	0	1	OSC_{in}
0	1	0	$OSC_{in}/2$
0	1	1	$OSC_{in}/4$
1	0	0	$OSC_{in}/8$ (POR Default)
1	0	1	$OSC_{in}/16$
1	1	0	$OSC_{in}/8$
1	1	1	$OSC_{in}/16$

C1 - f_VE: Enables the f_V output when set high. When cleared low, the f_V output is forced to a static low level. The bit is cleared low upon power up.

C0 - f_RE: Enables the f_R output when set high. When cleared low, the f_R output is forced to a static low level. The bit is cleared low upon power up.

Figure 16. C Register Access and Format (8 Clock Cycles are Used)

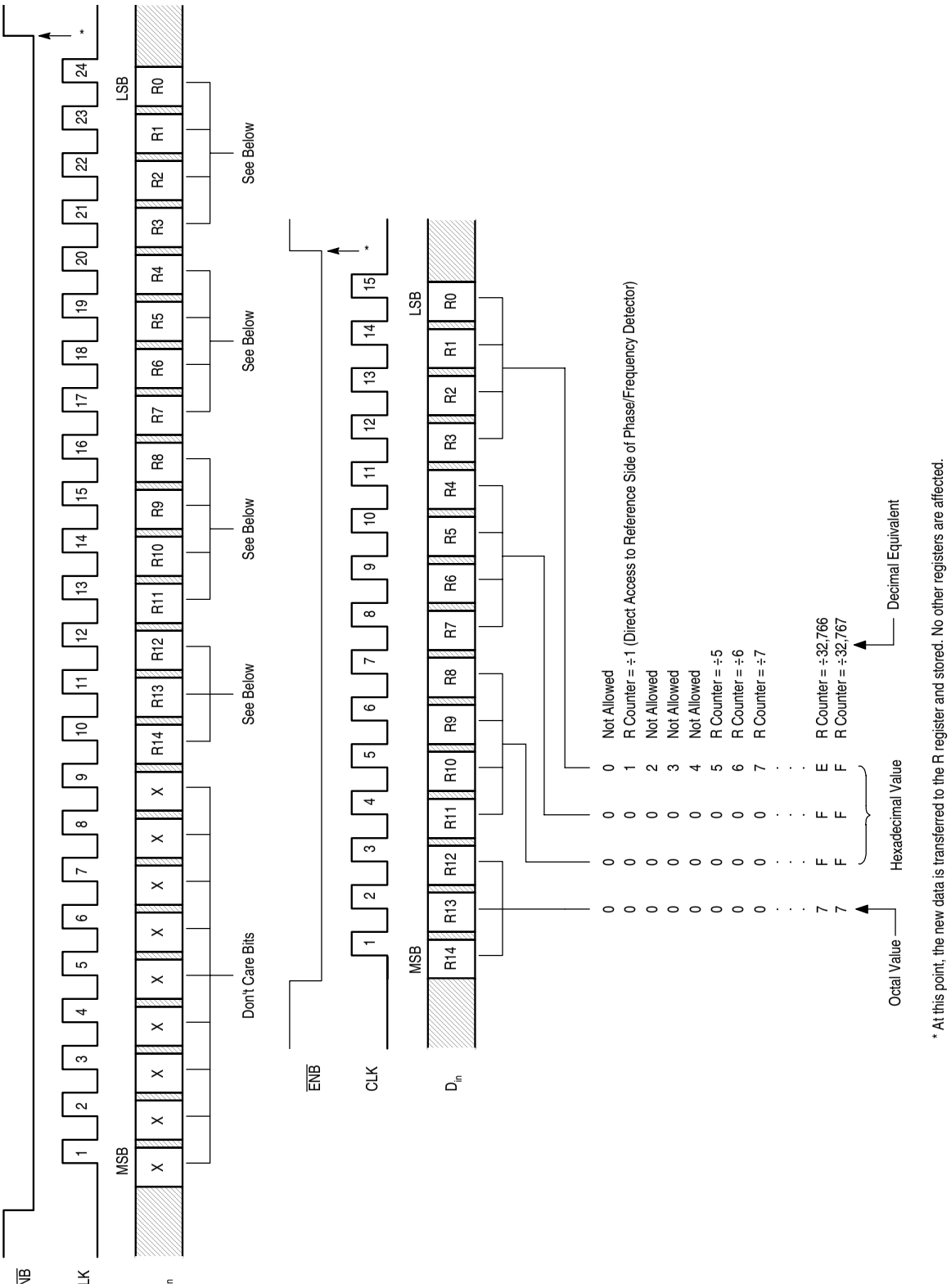
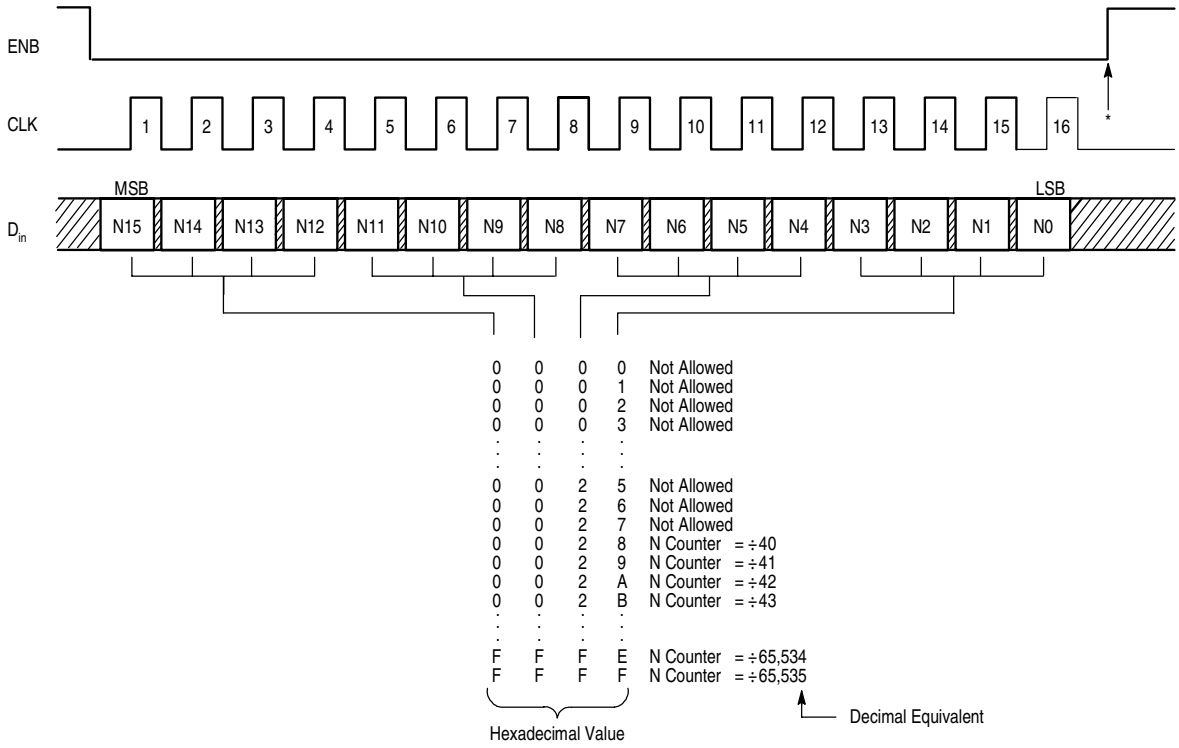
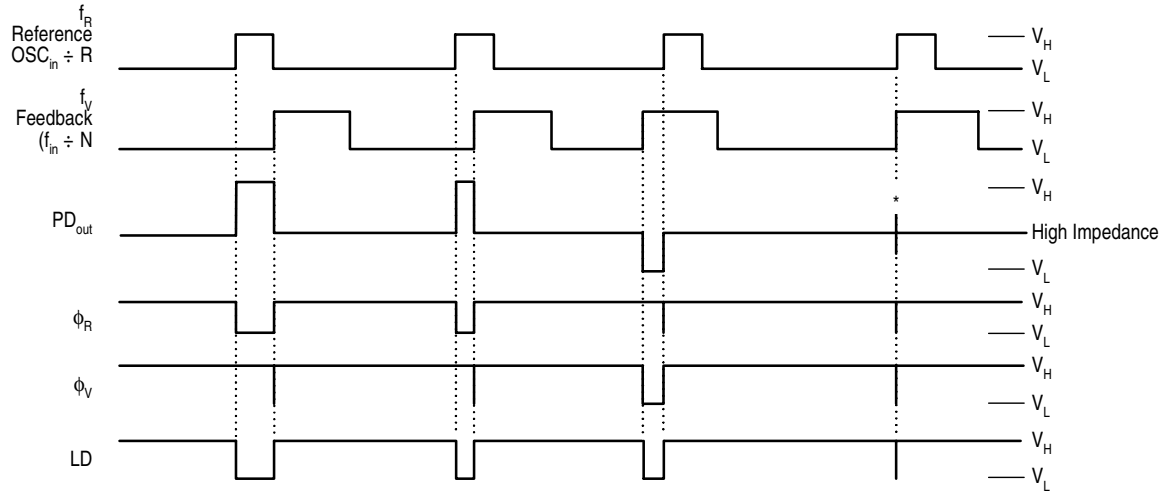


Figure 17. R Register Access and Formats (Either 24 or 15 Clock Cycles Can Be Used)



*At this point, the two new bytes are transferred to the N register and stored. No other registers are affected. In addition, the N and R counters are jam-loaded and begin counting down together.

Figure 18. N Register Access and Format (16 Clock Cycles Are Used)



V_H = High voltage level
V_L = Low voltage level
*At this point, when both f_R and f_V are in phase, both the sinking and sourcing output FETs are turned on for a very short internal.

NOTE: The PD_{out} generates error pulses during out-of-lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low-pass filter capacitor. PDout, ϕ_R and ϕ_V are shown with the polarity bit (POL) = low; see Figure 16 for POL.

Figure 19. Phase/Frequency Detector and Lock Detector Output Waveforms

4 Design Considerations

4.1 Crystal Oscillator Considerations

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

4.1.1 Use of a Hybrid Crystal Oscillator

Commercially available temperature-compensated crystal oscillators (TCXOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to OSC_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used (see Figures 9 and 10).

For additional information about TCXOs, visit *motorola.com* on the world wide web.

4.1.2 Use of the On-Chip Oscillator Circuitry

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 20.

The crystal should be specified for a loading capacitance (C_L) which does not exceed 20 pF when used at the highest operating frequencies listed in Table 6, **Loop Specifications**. Larger C_L values are possible for lower frequencies. Assuming R1 = 0 Ω, the shunt load capacitance (C_L) presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C1 ¥ C2}{C1 + C2}$$

where

C_{in} = 5.0 pF (see Figure 21)
C_{out} = 6.0 pF (see Figure 21)
C_a = 1.0 pF (see Figure 21)
C1 and C2 = external capacitors (see Figure 21)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be “trimmed” on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes 0 in the above expression for C_L.

A good design practice is to pick a small value for C1, such as 5 to 10 pF. Next, C2 is calculated. C1 < C2 results in a more robust circuit for start-up and is more tolerant of crystal parameter variations.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 22. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 20. limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency at the REF_{out} pin (OSC_{out} is not used because loading impacts the oscillator). The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 8).

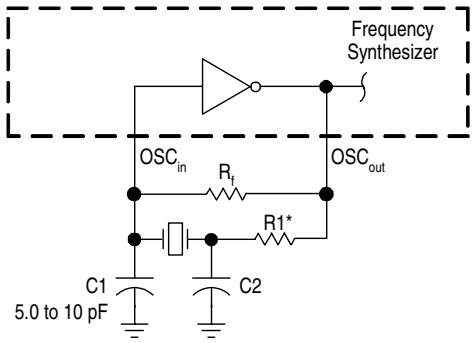


Figure 20. Pierce Crystal Oscillator Circuit

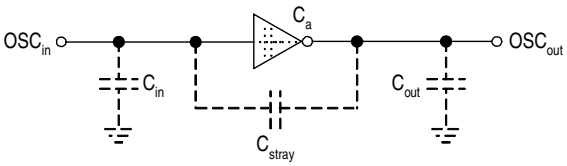
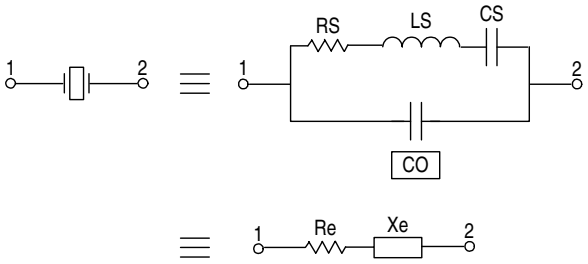


Figure 21. Parasitic Capacitances of the Amplifier and C_{stray}



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 22. Equivalent Crystal Networks

Recommended Reading

Technical Note TN-24, Statek Corp.

Technical Note TN-7, Statek Corp.

E. Hafner, “The Piezoelectric Crystal Unit-Definitions and Method of Measurement”, *Proc. IEEE,* Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, “Quartz Crystals for Frequency Control”, *Electro-Technology*, June 1969.

P. J. Ottowitz, “A Guide to Crystal Selection”, *Electronic Design*, May 1966.

D. Babin, “Designing Crystal Oscillators”, *Machine Design*, March 7, 1985.

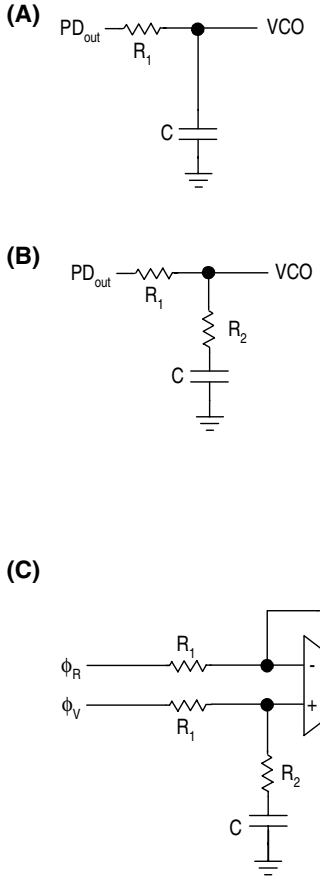
D. Babin, “Guidelines for Crystal Oscillator Design”, *Machine Design*, April 25, 1985.

Contact Motorola for MC145170-2 control software.

Table 8. Partial List of Crystal Manufacturers

CTS Corp.
United States Crystal Corp.
Crystek Crystal
Statek Corp.
Fox Electronics

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}} \qquad \zeta = \frac{N\omega_n}{2K_\phi K_{VCO}} \qquad F(s) = \frac{1}{R_1sC+1}$$

$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1+R_2)}} \qquad \zeta = 0.5\omega_n\left(R_2C + \frac{N}{K_\phi K_{VCO}}\right) \qquad F(s) = \frac{R_2sC+1}{(R_1+R_2)sC+1}$$

$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}} \qquad \zeta = \frac{\omega_n R_2 C}{2} \qquad F(s) = \frac{R_2sC+1}{R_1sC}$$

Notes:

1. For (C), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.
2. The ϕ_R and ϕ_V outputs swing rail-to-rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp.
3. For the latest information on MC33077 or equivalent, see the Motorola IC web site at *http://www.motorola.com/semiconductors*.

Denifitions:

N = Total Division Ratio in Feedback Loop

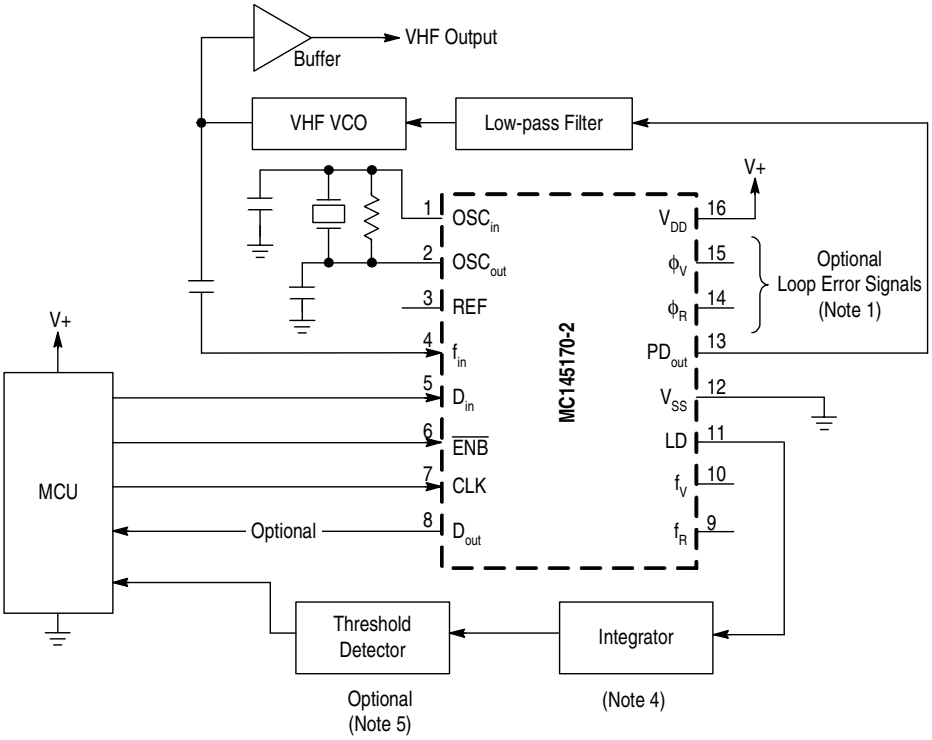
K_ϕ (Phase Detector Gain) = VDD/4p volts per radian for PDout

K_ϕ (Phase Detector Gain) - VDD/2p volts per radian for fV and fR

$$K_{VCO}(\text{VCO Gain}) = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

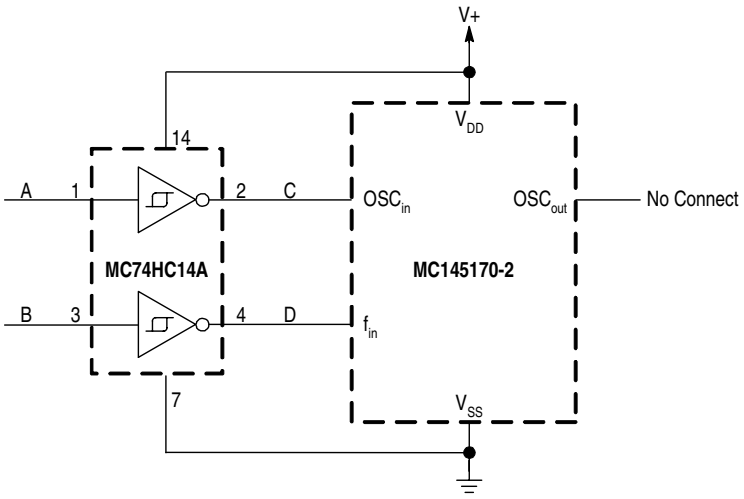
For a nominal design starting point, the user might consider a damping factor $\zeta = 0.7$ and a natural loop frequency $\omega_n = (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R-related VCO standards.

Figure 23. Phase-Locked Loop - Low Pass Filter Design



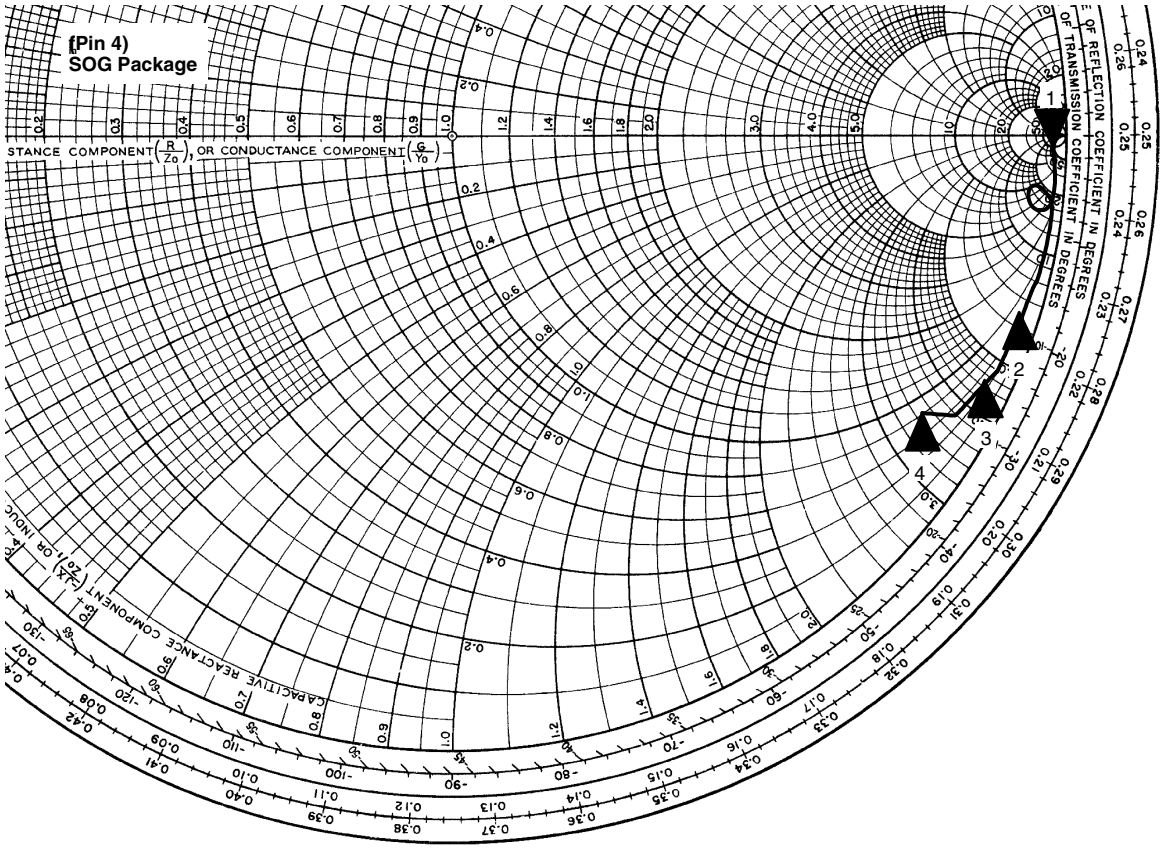
NOTES:
1. The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase-Locked Loop — Low-Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail-to-rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used inthe combiner/loop filter.
2. For optimum performance, bypass the V_{DD} pin to V_{SS} (GND) with one or more low-inductance capacitors.
3. The R counter is programmed for a divide value = OSC_{in}/f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by f_R = N, wher e N is the divide value of the N counter.
4. May be an R-C low-pass filter.
5. May be a bipolar transistor.

Figure 24. Example Application



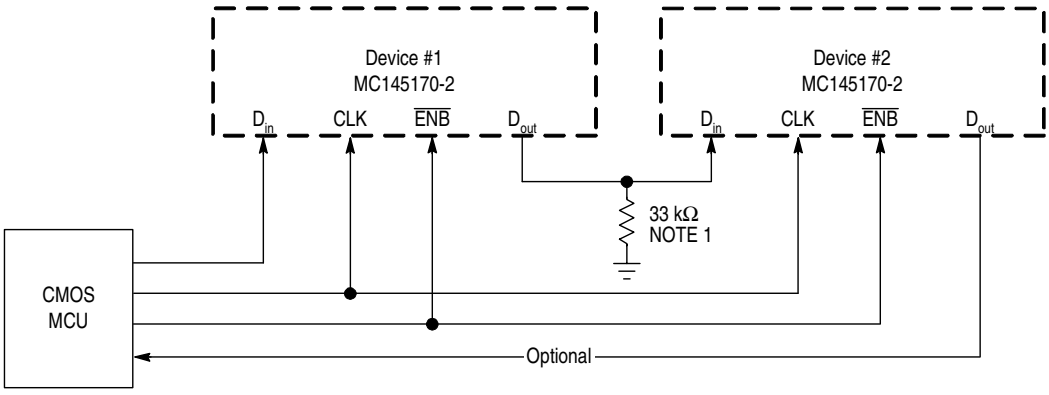
NOTE:
The signals at Points A and B may be low-frequency sinusoidal or square waves with slow edge rates or noisy signal edges. At Points C and D, the signals are cleaned up, have sharp edge rates, and rail-to-rail signal swings. With signals as described at Points C and D, the MC145170-2 is guaranteed to operate down to a frequency as low as dc.
Refer to the MC74HC14A data sheet for input switching levels and hysteresis voltage range.

Figure 25. Low Frequency Operation Using DC Coupling



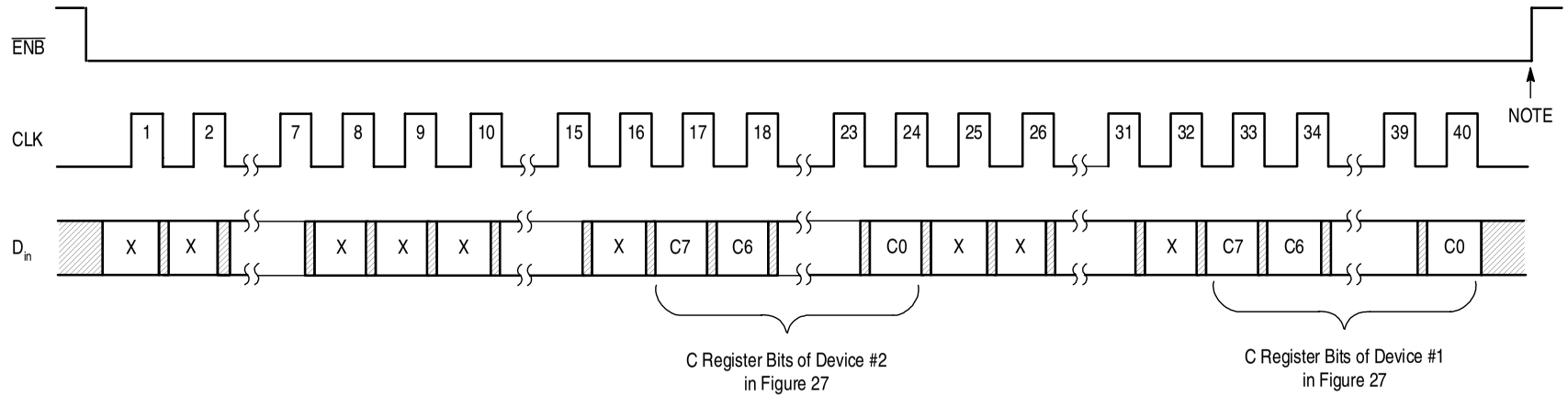
Marker	Frequency (MHz)	Resistance (Ω)	Reactance (Ω)	Capacitance (pF)
1	5	2390	-5900	5.39
2	100	39.2	-347	4.58
3	150	25.8	-237	4.48
4	185	42.6	-180	4.79

Figure 26. Input Impedance at f_{in} - Series Format (R + jX) (5.0 MHz to 185 MHz)



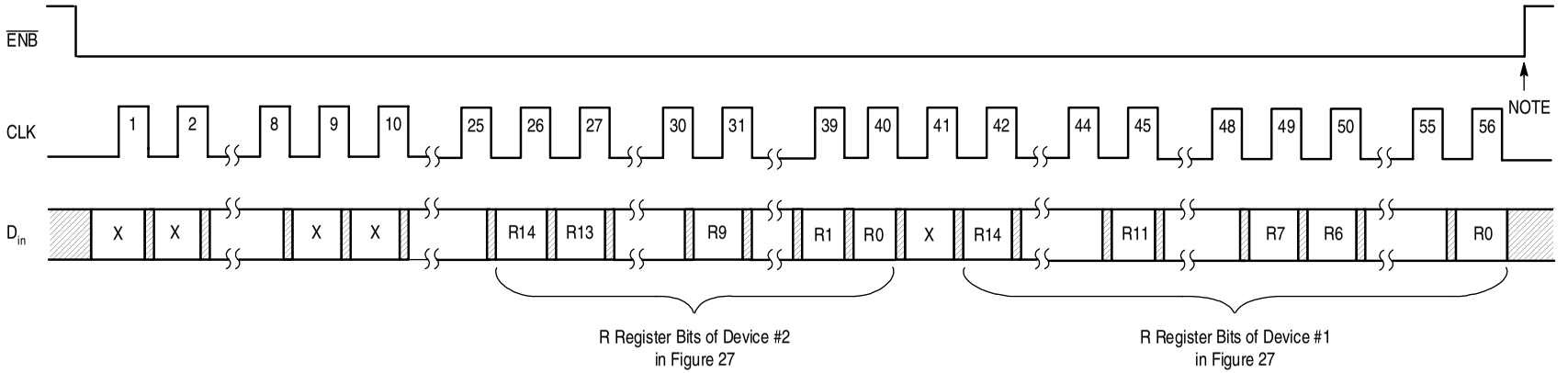
NOTES:
1. The 33 kΩ resistor is needed to prevent the D_{in} pin from floating. (The D_{out} pin is a three-state output.)
2. See related Figures 28, 29, and 30.

Figure 27. Cascading Two MC145170-2 Devices



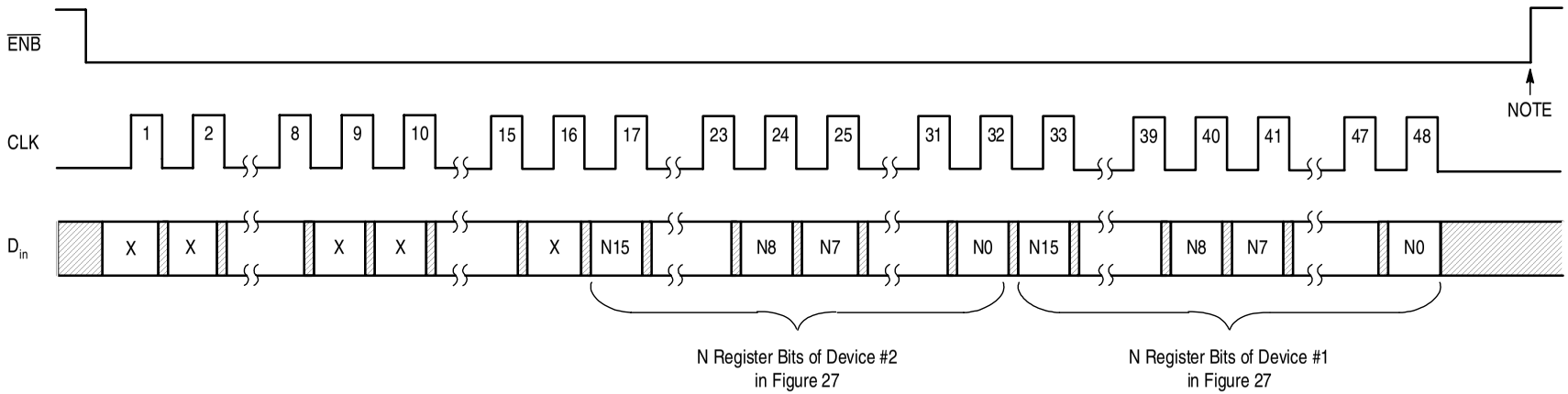
NOTE: At this point, the new data is transferred to the C registers of both devices and stored. No other registers are affected.

Figure 28. Accessing the C Registers of Two Cascaded MC145170-2 Devices



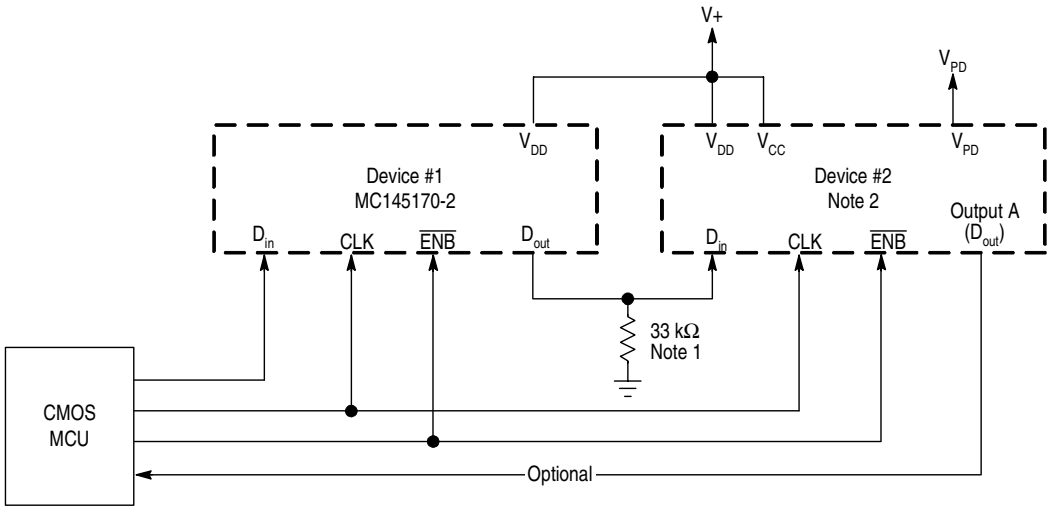
NOTE: At this point, the new data is transferred to the R registers of both devices and stored. No other registers are affected.

Figure 29. Accessing the R Registers of Two Cascaded MC145170-2 Devices



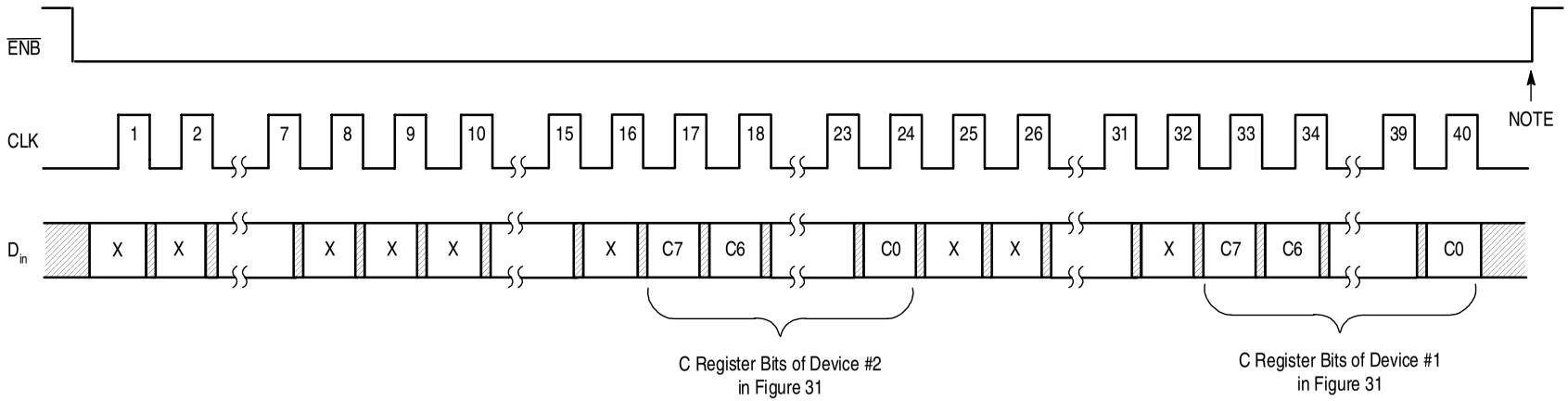
NOTE: At this point, the new data is transferred to the N registers of both devices and stored. No other registers are affected.

Figure 30. Accessing the N Registers of Two Cascaded MC145170-2 Devices



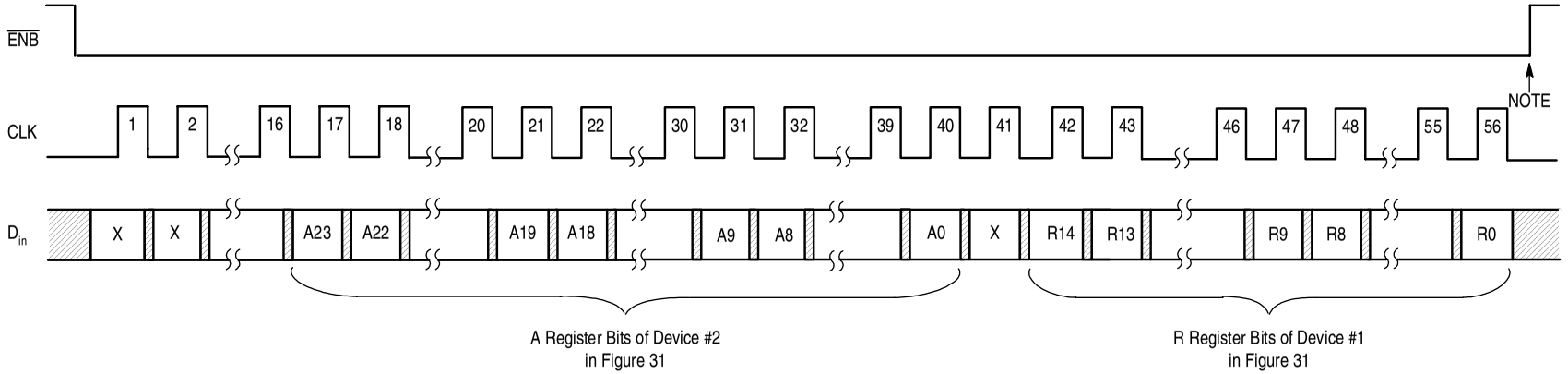
NOTES:
1. The 33 kΩ resistor is needed to prevent the D_{in} pin from floating. (The D_{out} pin is a three-state output.)
2. This PLL Frequency Synthesizer may be a MC145190, MC145191, MC145192, MC145200, or MC145201.
3. See related Figures 32, 33, and 34.

Figure 31. Cascading Two Different Device Types



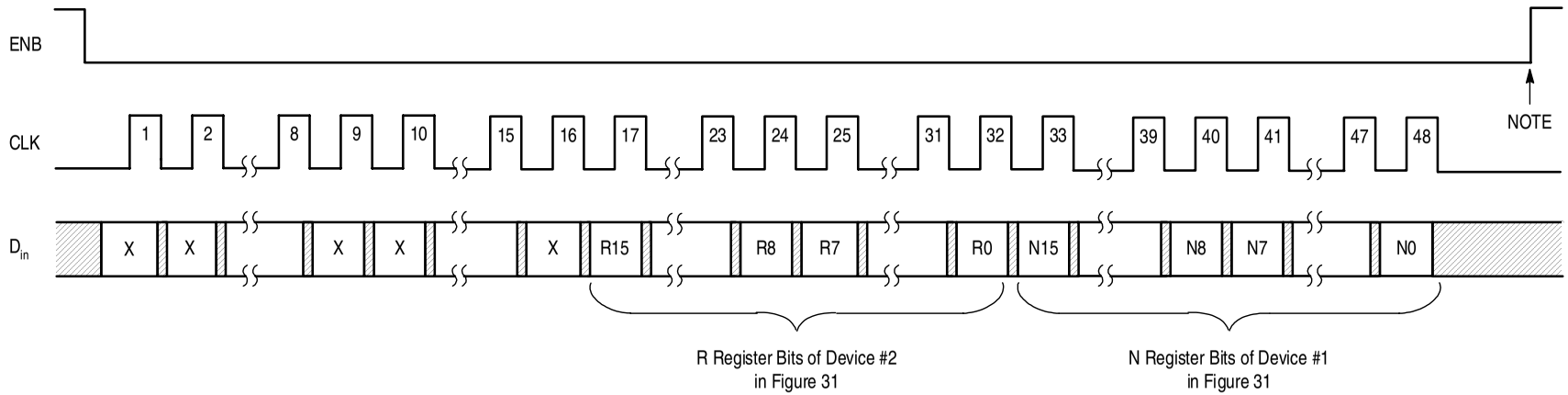
NOTE: At this point, the new data is transferred to the C registers of both devices and stored. No other registers are affected.

Figure 32. Accessing the C Registers of Two Different Device Types



NOTE: At this point, the new data is transferred to the A register of Device #2 and R register of Device #1 and stored. No other registers are affected.

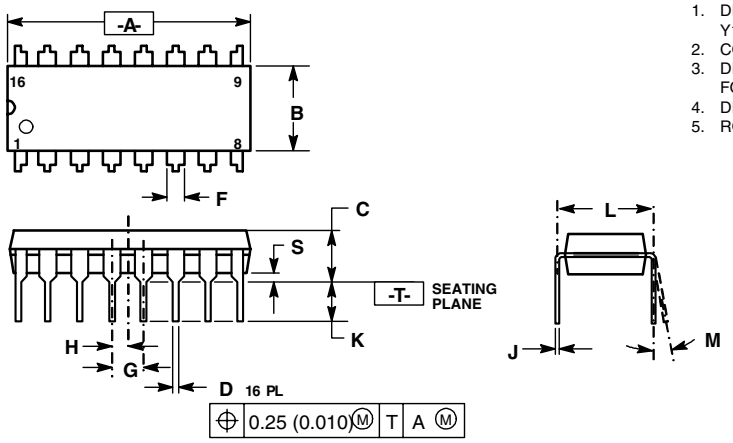
Figure 33. Accessing the A and R Registers of Two Different Device Types



NOTE: At this point, the new data is transferred to the R register of Device #2 and N register of Device #1 and stored. No other registers are affected.

Figure 34. Accessing the R and N Registers of Two Different Device Types

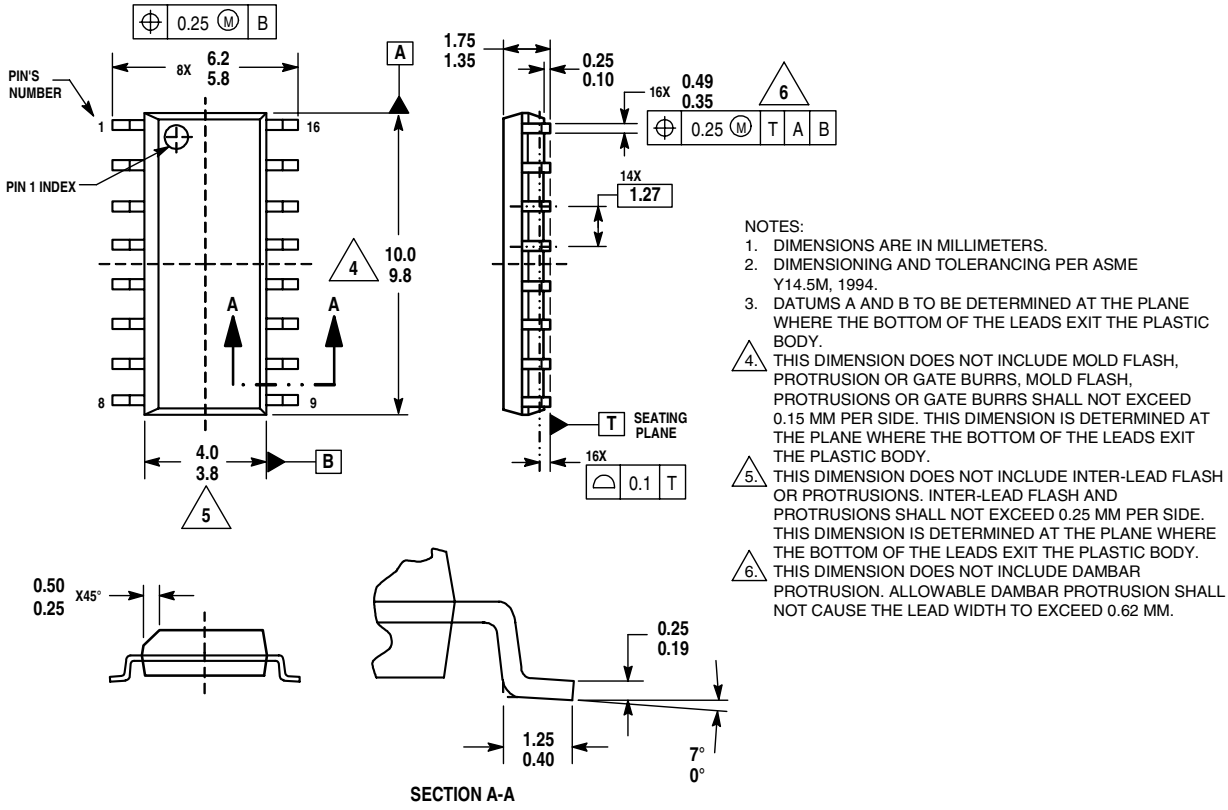
5 Packaging



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

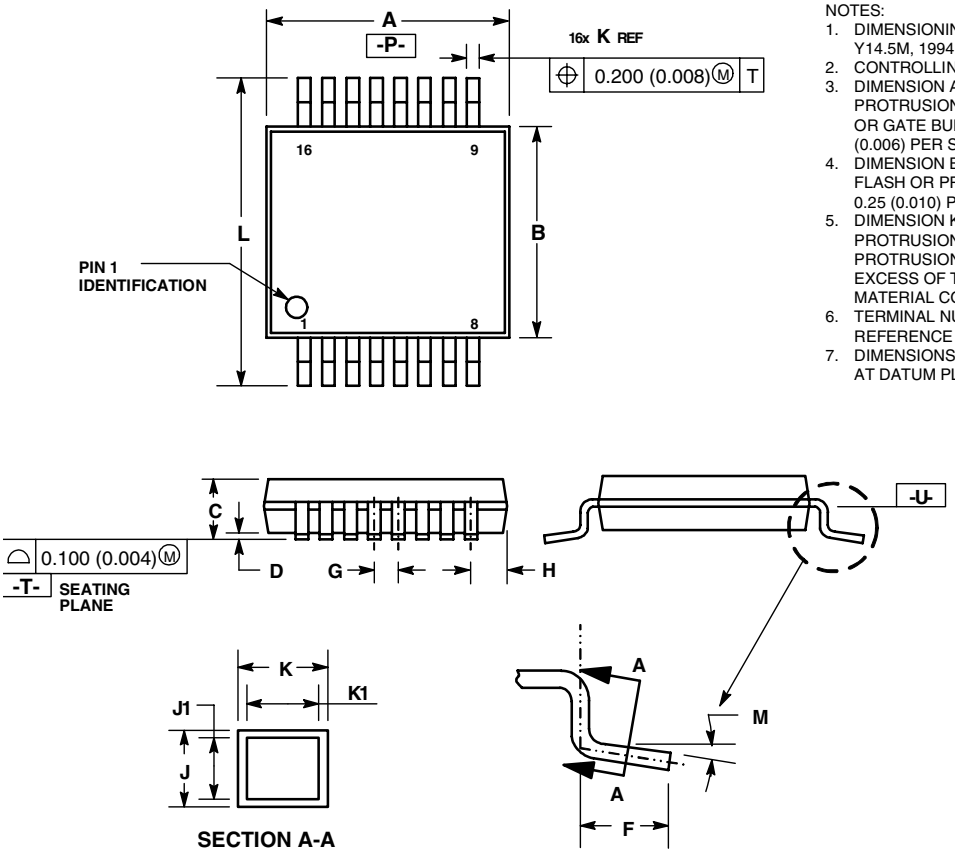
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0	10	0	10
S	0.020	0.040	0.51	1.01

Figure 35. Outline Dimensions for P Suffix, DIP-16
(Case 648-08, Issue R)



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS, MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62 MM.

Figure 36. Outline Dimensions for D Suffix, SOG-16
(Case 751B-05, Issue J)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE -U-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	5.10	---	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0047
D	0.05	0.25	0.002	0.010
F	0.45	0.55	0.018	0.022
G	0.65 BSC		0.026 BSC	
H	0.22	0.23	0.009	0.010
J	0.09	0.24	0.004	0.009
J1	0.09	0.18	0.004	0.007
K	0.16	0.32	0.006	0.013
K1	0.16	0.26	0.006	0.010
L	6.30	6.50	0.248	0.256
M	5	15	5	15

Figure 37. Outline Dimensions for DT Suffix, TSSOP-16
(Case 948C-03, Issue B)

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MC145170-2/D

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The MC145170 in Basic HF and VHF Oscillators

Prepared by: David Babin and Mark Clark

Phase–locked loop (PLL) frequency synthesizers are commonly found in communication gear today. The carrier oscillator in a transmitter and local oscillator (LO) in a receiver are where PLL frequency synthesizers are utilized. In some cellular phones, a synthesizer can also be used to generate 90 MHz for an offset loop. In addition, synthesizers can be used in computers and other digital systems to create different clocks which are synchronized to a master clock.

The MC145170 is available to address some of these applications. The frequency capability of the newest version, the MC145170–2, is very broad — from a few hertz to 185 MHz.

ADVANTAGES

Frequency synthesizers, such as the MC145170, use digital dividers which can be placed under MCU control. Usually, all that is required to change frequencies is to change the divide ratio of the N Counter. Tuning in less than a millisecond is achievable.

The MC145170 can generate many frequencies based on the accuracy of a single reference source. For example, the reference can be a low–cost basic crystal oscillator or a temperature–compensated crystal oscillator (TCXO). Therefore, high tuning accuracies can be achieved. Boosting of the reference frequency by 100x or more is achievable.

ELEMENTS IN THE LOOP

The components used in the PLL frequency synthesizer of Figure 1 are the MC145170 PLL chip, low–pass filter, and voltage–controlled oscillator (VCO). Sometimes a voltage–controlled multivibrator (VCM) is used in place of the VCO. The output of a VCM is a square wave and is usually integrated before being fed to other sections of the radio. The VCM output can be directly used in computers and other digital equipment. The output of a VCO or VCM is typically buffered, as shown.

As shown in Figure 2, the MC145170 contains a reference oscillator, reference counter (R Counter), VCO/VCM counter (N Counter), and phase detector. A more detailed block diagram is shown in the data sheet.

HF SYNTHESIZER

The basic information required for designing a stable high–frequency PLL frequency synthesizer is the frequencies required, tuning resolution, lock time, and overshoot. For the example design of Figure 3, the frequencies needed are 9.20 MHz to 12.19 MHz. The resolution (usually the same as the frequency steps or channel spacing) is 230 kHz. The lock time is 8 ms and a maximum overshoot of approximately 15% is targeted. For purposes of this example, lock is considered to be when the frequency is within about 1% of the final value.

HF SYNTHESIZER LOW–PASS FILTER

In this design, assume a square wave output is acceptable. To generate a square wave, a MC1658 VCM chip is chosen. Per the transfer characteristic given in the data sheet, the MC1658 transfer function, K_{VCM}, is approximately 1×10^8 radians/second/volt. The loading presented by the MC1658 control input is large; the maximum input current is 350 μA. Therefore, an active low–pass filter is used so that loading does not affect the filter's response. See Figure 3. In the filter, a 2N7002 FET is chosen because it has very high transconductance (80 mmhos) and low input leakage (100 nA).

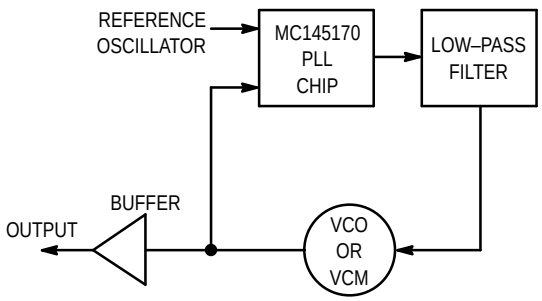

Figure 1. PLL Frequency Synthesizer

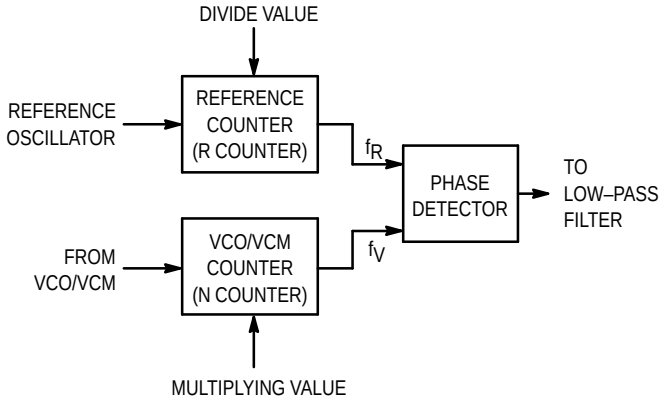

Figure 2. Detail of the MC145170

REV 2
1/98 TN98011500

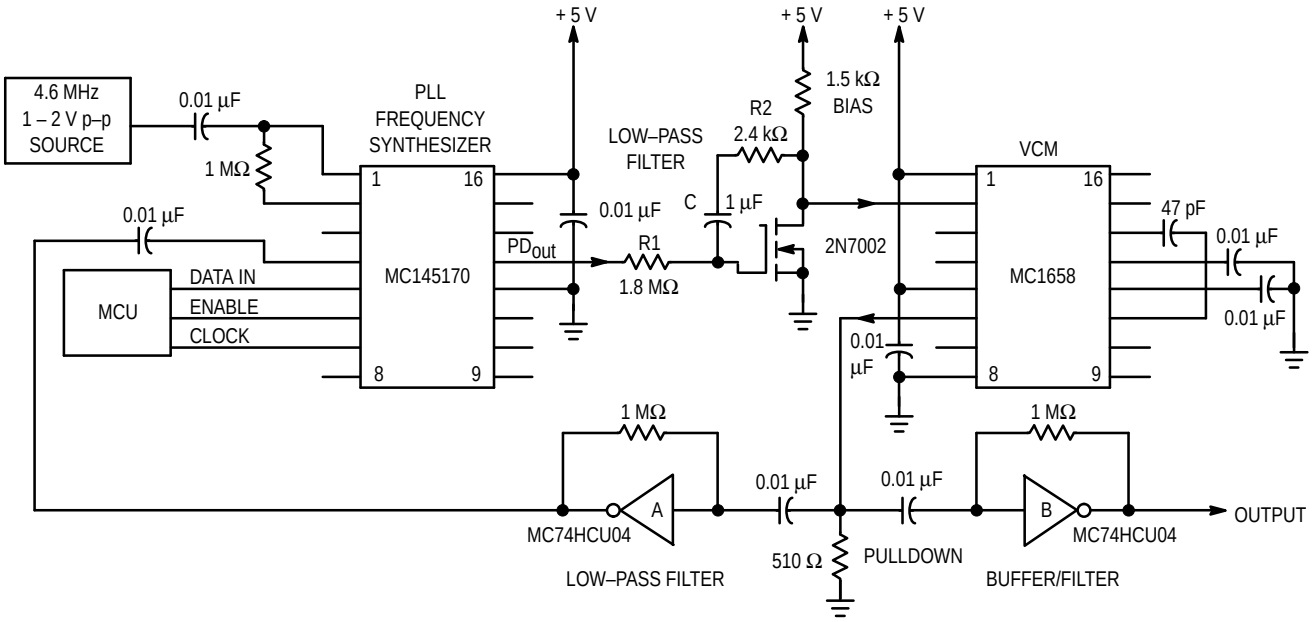

Figure 3. HF Synthesizer

In order to calculate the average divide value for the N Counter, follow this procedure. First, determine the average frequency; this is (12.19 + 9.2)/2 = 10.695 MHz or approximately 10.7 MHz. Next, divide this frequency by the resolution: 10.7 MHz/230 kHz = about 47.

Next, reference application note AN535 (see book DL136/D Rev 3 or 4). The active filter chosen takes the form shown in Figure 9 of the application note. This filter is used with the single–ended phase detector output of the MC145170, PD_{out}. The phase detector associated with PD_{out} has a gain $K_\phi = V_{DD}/4\pi$. For a supply of 5 V, this is $5/4\pi$ = 0.398 V/rad. The system's step response is shown in Figure 4. To achieve about 15% overshoot, a damping factor of 0.8 is used. This causes frequency to settle to within 1% at $\omega_n t$ = 5.5.

The information up to this point is as follows.

f_{ref} = 230 kHz

f_{VCM} = 9.2 to 12.19 MHz; the average is 10.7 MHz, average N = 47

power supply = 5 V for the phase detector

$K_{VCM} = 1 \times 10^8$ rad/s/V

overshoot = approximately 15%, yields a damping factor = 0.8

lock time t = 8 ms settling to within 1%, $\omega_n t$ = 5.5

$K\phi$ or K_p = 0.398 V/rad.

From the application note, equation 61, $\omega_n = 5.5/t = 5.5/0.008 = 687.5$ rad/s.

Equation 59 is $R1C = (K_p K_v)/\omega_n^2 N$

$= (0.398 \times 1 \times 10^8)/687.5^2 \times 47$

$= 1.79$

Equation 59 is used because of the high–gain FET.

Next, the capacitor C is picked to be 1 µF. Therefore, R1 = 1.79/C which is 1.79 MΩ. The standard value of 1.8 MΩ is used for R1.

Equation 63 is $R2 = (2\zeta)/C\ \omega_n$

$= (2 \times 0.8)/(1 \times 10^{-6} \times 687.5)$

$= 2.33$ kΩ.

A standard value for R2 of 2.4 kΩ is utilized.

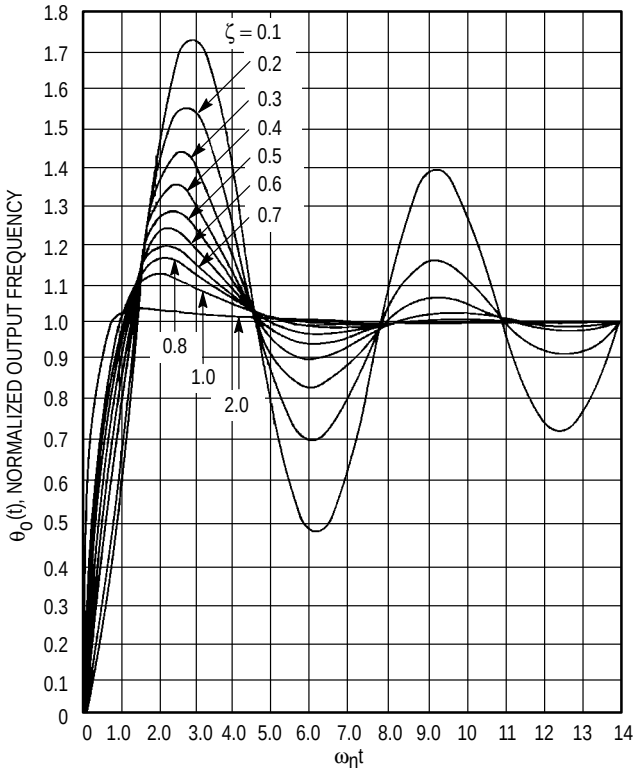

Figure 4. Type 2 Second Order Step Response

HF SYNTHESIZER PROGRAMMING

Programming the MC145170 is straightforward. The three registers may be programmed in a byte–oriented fashion. The registers retain their values as long as power is applied. Thus, usually both the C and R Registers are programmed just once, right after power up.

The C Register, which configures the device, is programmed with $C0 (1 byte). This sets the phase detector to the proper polarity and activates PD_{out}. This also turns off the unused outputs. The phase detector polarity is determined by the filter and the VCM. For this example, the MC1658 data sheet shows that a higher voltage level is needed if speed is to be increased. However, the low–pass filter inverts the signal from the phase detector (due to the active element configuration). Therefore, the programming of the polarity for the phase detector means that the POL bit must be a “1.”

The R Register is programmed for a divide value that results in the proper frequency at the phase detector reference input. In this case, 230 kHz is needed. Therefore, with the 4.6 MHz source shown in Figure 3, the R Register needs a value of $000014 (3 bytes, 20 in decimal).

The N Register determines the frequency tuned. Tuning 9.2 MHz requires the proper value for N to multiply up the reference of 230 kHz to 9.2 MHz. This is 40 decimal. For 12.19 MHz, the value is 53 decimal. To tune over the range, change the value in the N Register within the range of 40 to 53 with a 2–byte transfer. Table 1 shows the possible frequencies.

Table 1. The HF Oscillator Frequencies

N Value	Frequency, MHz
40	9.20
41	9.43
42	9.66
43	9.89
44	10.12
45	10.35
46	10.58
47	10.81
48	11.04
49	11.27
50	11.50
51	11.73
52	11.96
53	12.19

EXTRA FILTERING FOR THE HF LOOP

When the HF oscillator was built, the proper frequencies could not be tuned. The output of the MC1658 was examined with an oscilloscope and the switching edges were discovered to be “ragged.” That is, the output did not appear to be a square wave with clean transitions.

The f_{in} input of the MC145170 is sensitive to 500 mV p–p signals, and the ragged edges were being amplified and counted down by the N Counter. Therefore, the edges needed cleaning up. One method would have been to add a low–pass filter between the MC1658 and MC145170. However, because an additional buffer was needed elsewhere in the circuit, an MC74HCU04 inverter was used in place of the filter. This inverter’s frequency response is low enough to clean up the ragged edges. That is, filtering of the ragged edges occurred, and the output had smoother transitions. As mentioned previously, one of the elements in the inverter package was used to buffer the output of the VCM before feeding it to the outside world. See Figure 3.

VHF SYNTHESIZER

The MC145170 may be used in VHF designs, also. The range for this next example is 140 to 160 MHz in 100 kHz increments.

VHF SYNTHESIZER LOW–PASS FILTER

To illustrate design with the doubled–ended phase detector, the ϕ_R and ϕ_V outputs are used. This requires an operational amplifier, as shown in Figure 5. From the design guidelines shown in the MC145170 data sheet, the following equations are used:

$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{N\ C\ R_1}} \quad (1)$$

$$\text{damping factor} \quad \zeta = \frac{\omega_n R_2 C}{2} \quad (2)$$

where, from the data sheet, the equation for the ϕ_R and ϕ_V phase detector,

$$K_\phi = \frac{V_{DD}}{2\pi} = \frac{5}{2\pi} = 0.796 \text{ V/rad} \quad (3)$$

$$\zeta = 0.707,$$

$$\omega_n = \frac{2\pi f_R}{50} = \frac{2\pi \times 100 \text{ kHz}}{50} = 12{,}566 \text{ rad/s} \quad (4)$$

and

$$K_{VCO} = \frac{2\pi\ \Delta\ f_{VCO}}{\Delta\ V_{VCO}} = \frac{2\pi \times (160 - 140 \text{ MHz})}{10 - 2}$$

$$= 1.57 \times 10^7 \text{ rad/s/V} \quad (5)$$

The control voltage range on the input to the VCO is picked to be 2 to 10 V.

The average frequency = (140 + 160)/2 = 150 MHz. Therefore, the average N = 1500.

The above choices for ζ and ω_n are rules of thumb that are a good design starting point. A larger ω_n value results in faster loop lock times and higher reference frequency VCO sidebands for similar sideband filtering. (See Advanced Considerations.)

Choosing C_1 to be 4700 pF, R_1 is calculated from the rearranged expression for ω_n as:

$$R_1 = \frac{K_\phi K_{VCO}}{C_1 \omega_n^2 N} = \frac{(0.796 \text{ V/rad})(1.57 \times 10^7 \text{ rad/s/V})}{(4700 \text{ pF})(12{,}566 \text{ rad/s})^2\ (1500)}$$

$$= 11.23 \text{ k}\Omega \quad (6)$$

Therefore, chose an 11 kΩ standard value resistor.
R_2 is determined from:

$$R_2 = \frac{2\zeta}{\omega_n C_1} = \frac{(2)(0.707)}{(12{,}566)(4700 \text{ pF})}$$

$$= 23.94 \text{ k}\Omega \text{ or}$$
$$24 \text{ k}\Omega \text{ (standard value)} \quad (7)$$

VHF SYNTHESIZER EXTRA FILTERING

For more demanding applications, extra filtering is sometimes added. This reduces the VCO sidebands caused by a small amount of the reference frequency feeding through the filter. One form of this filtering consists of spitting R1 into two resistors; each resistor is one–half the value of R1, as indicated by R1/2 in Figure 5. Capacitors C_C are added from the

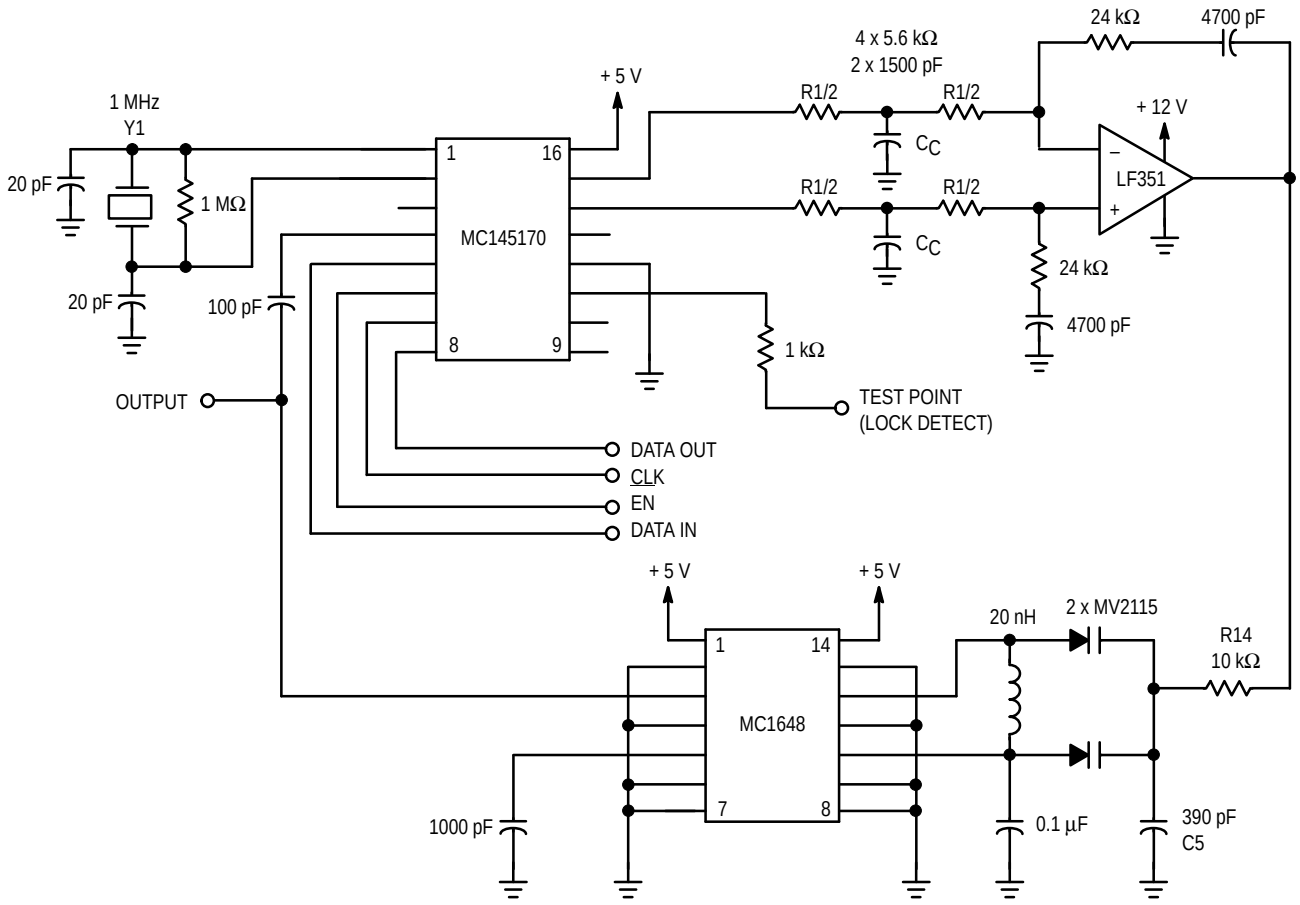

Figure 5. VHF Synthesizer

midpoints to ground to further filter the reference sidebands. The value of C_C is chosen so that the corner frequency of this added network does not significantly affect the original loop bandwidth ω_B.

The rule of thumb for an initial value is $C_C = 4 / (R1\ \omega_{RC})$, where ω_{RC} is the filter cutoff frequency. A good value is to choose ω_{RC} to be 10 x ω_B, so as to not significantly impact the original filter.

$$\omega_B = \omega_n \sqrt{1 + 2\zeta^2 + \sqrt{2 + 4\zeta^2 + 4\zeta^4}} \quad (8)$$

$$= 12{,}566\sqrt{1+(2)(0.707)^2+ \sqrt{2+(4)(0.707)^2+ (4)(0.707)^4}}$$

$$= 25{,}860 \text{ rad/s}$$

$$\omega_{RC} = 10\ \omega_B = (10)(25{,}860) = 258{,}600 \text{ rad/s} \quad (9)$$

$$C_C = \frac{4}{R1\omega_{RC}} = \frac{4}{(11.23\ \text{k}\Omega)(258{,}600 \text{ rad/s})} \quad (10)$$

$$= 1377 \text{ pF} \approx 1500 \text{ pF}$$

There is also a filter formed at the input to the VCO. Again, this should be selected to ensure that it does not significantly affect the loop bandwidth. For this example, the filter is dominated by R14 with C5. The capacitance of the varactors (in series with the rest of the circuit) is much smaller than C5 and can therefore be neglected for this calculation.

As above, let ω_{RC} = 258,600 rad/s be the cutoff of this filter. R14 is chosen to be 10 kΩ. Therefore,

$$C_5 = \frac{1}{\omega_{RC}R_{14}} = \frac{1}{(258{,}600)(10\ \text{k}\Omega)} \quad (11)$$

$$= 387 \text{ pF} \approx 390 \text{ pF}$$

THE VARACTOR

The MV2115 was selected for its tuning ratio of 2.6 to 1. The capacitance can be changed from 49.1 pF to 127.7 pF over a reverse bias swing of 2 to 30 volts. Contact your Motorola representative for information regarding the MV2115 varactor diode.

For example, three parameters are considered.

C_T = Nominal capacitance
CR = Capacitance ratio
fR = Frequency ratio

$$CR = \frac{C_V\text{min}}{C_V\text{max}} = \left(\frac{V_{max}}{V_{min}}\right)^{\rho} \quad (12)$$

where ρ = the capacitance exponent

Therefore,

$$CR = 2.6 = \left(\frac{30}{2}\right)^{\rho} \quad (13)$$

$$\log(2.6) = \rho\log(15) \quad (14)$$

$$\rho = \log(2.6)/\log(15) = 0.3528 \quad (15)$$

Using the nominal capacitance of 100 pF at 4 volts:

$$\frac{100\text{ pF}}{C_V\text{max}} = \left(\frac{10}{4\text{ V}}\right)^{0.3528} \quad (16)$$

$$\frac{100\text{ pF}}{C_V\text{max}} = 1.382$$

Solving for $C_V$max:

$$\frac{100\text{ pF}}{1.382} = 72.4\text{ pF}$$

Solving for $C_V$min:

$$2.6 = \frac{C_V\text{min}}{49.1\text{ pF}} \quad (17)$$

$$C_V\text{min} = (2.6)(49.1\text{ pF})$$

$$C_V\text{min} = 127.7\text{ pF}$$

THE VCO

For convenience, the MC1648 VCO is selected. The tuning range of the VCO may be calculated as

$$\frac{f_{max}}{f_{min}} = \frac{(C_d\text{max} + C_S)^{0.5}}{(C_d\text{min} + C_S)^{0.5}} \quad (18)$$

where

$$f_{min} = \frac{1}{2\pi[L(C_d\text{max} + C_S)]^{0.5}} \quad (19)$$

As shown in Figure 8 of the data sheet, the VCO tank circuit is comprised of two varactors and an inductor. Typically, a single varactor might be used in either a series or parallel configuration. However, the second varactor has a two–fold purpose. First, if the 10 kΩ isolating impedance is left in place, the varactors add in series for a smaller capacitance. Second, the added varactor acts to eliminate distortion due to the tank voltage changing.

Therefore, with the two varactors in series, $C_d$max′ = $C_d$max/2. The shunt capacitance (input plus external capacitance) is symbolized by C_S.
Therefore, solving for the inductance:

$$L = \frac{1}{(2\pi f_{min})^2(C_d\text{max}' + C_S)} = 19.9\text{ nH} \approx 20\text{ nH} \quad (20)$$

The Q of the inductor should be more than 100 for best performance.

$$f_{min} = \frac{1}{2\pi[(19.9\text{ nH})(69.85\text{ pF})]^{0.5}} = 135\text{ MHz} \quad (21)$$

$$f_{max} = \frac{1}{2\pi[(19.9\text{ nH})(42.2\text{ pF})]^{0.5}} = 173\text{ MHz} \quad (22)$$

The frequency ratio is 1.5 to 1 and is impacted by the tuning range of the MV2115 varactor diode used in the tank circuit. Therefore, the required range of 140 to 160 MHz is not limited by this VCO design.

A pc board should be used to obtain favorable results with this VHF circuit. The lead lengths in the tank circuit should be kept short to minimize parasitic inductance. The length of the trace from the VCO output to the PLL input should be kept as short as possible. In addition, use of surface–mount components is recommended to help minimize strays.

VHF SYNTHESIZER PROGRAMMING

Again, programming the three registers of the MC145170 is straightforward. Also, usually both the C and the R Registers are programmed only once, after power up.

The C Register configures the device and is programmed with $80 (1 byte). This sets the phase detector to the correct polarity and activates the ϕ_R and ϕ_V outputs while turning off the other outputs. Like the HF oscillator, the phase detector polarity is determined by how the filter is hooked up and the VCO.

The R Register is programmed for a divide value that delivers the proper frequency at the phase detector reference input. In this case, 100 kHz is needed. Therefore, with the 1 MHz crystal shown, the R Register needs a value of $00000A (3 bytes, 10 in decimal).

The N Register determines the frequency tuned. To tune 140 MHz, the value required for N to multiply up the reference of 100 kHz to 140 MHz is 1400 decimal. For 160 MHz, the value is 1600 decimal. To tune over the range, simply change the value in the N Register with a 2–byte transfer.

ADVANCED CONSIDERATIONS

The circuit of Figure 5 may not function at very–high temperature. The reason is that the MC145170 is guaranteed to a maximum frequency of 160 MHz at 85°C. Therefore, there is no margin for overshoot (reference Figure 4) at high temperature. There are two possible solutions: (1) use the MC145170–1 or MC145170–2 which are rated to 185 MHz, or (2) limit the tuning to less than 160 MHz.

Operational amplifiers are usually too noisy for critical applications. Therefore, if an active element is required in the integrator, one or more discrete transistors are utilized. These may be FETs or bipolar devices. However, active filter elements are not needed if the VCO loading is not severe, such as is encountered with most discrete VCO designs. Because active elements add noise, some performance parameters are improved if they are not used. On the other hand, an active filter can be used to scale up the VCO control voltage. For example, to tune a wide range, the control voltage may have to range up to 10 V. For a 5 V PLL output, this would be scaled by 2x via use of active elements.

Some applications have requirements that must be met in the areas of phase noise and reference suppression. These parameters are in conflict with fast lock times. That is, as lock times are reduced, reference suppression becomes more difficult. Both reference suppression and phase noise are advanced areas that are covered in several publications. As an example, consider that the VCO input voltage range for the above VHF loop was merely picked to be 8 V. Advanced

techniques demand a trade off between this voltage range and the spectral purity of the VCO output. This is because the lower the control voltage range, the more sensitive the VCO is to noise coming into its control input.

A VCO IC may not offer enough performance for some applications. Therefore, the VCO may have to be designed from discrete components.

Figure 6 shows the performance of the VHF Oscillator prototype on a spectrum analyzer. Note that the reference sidebands appear at 100 kHz as expected, and are 50 dB down.

REFERENCES

Motorola data sheet MC145170/D
Motorola data sheet MC145170–1/D
Motorola data sheet MC145170–2/D
Motorola application note AN535/D

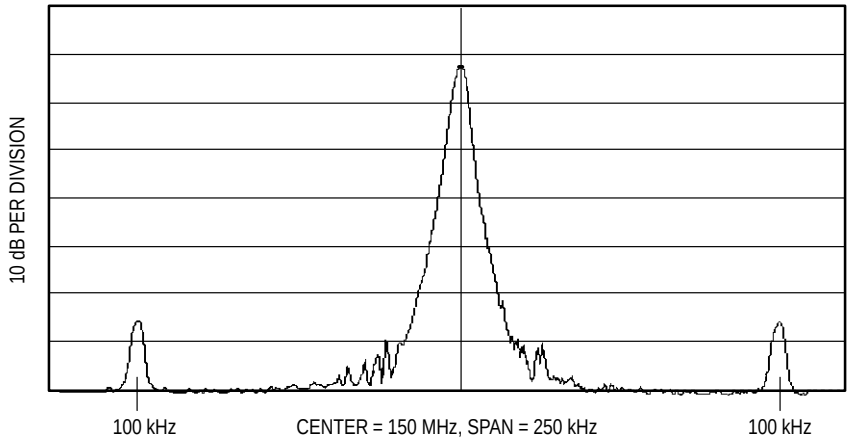

Figure 6. VHF Oscillator Performance

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SIEMENS

Mixers

S 042 P

Bipolar IC

Features

- Versatile application
- Wide range of supply voltage
- Few external components
- High conversion transconductance
- Low noise figure

Type	Ordering Code	Package
S 042 P	Q67000-A335	P-DIP-14

Symmetrical mixer for frequencies up to 200 MHz. It can be driven by an external source or by the built-in oscillator. The input signals are suppressed at the outputs. In addition to the usual mixer applications in receivers, converters, and demodulators for AM and FM, the S 042 P can also be used as electronic polarity switch, multiplier etc.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	15	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	– 40 to 125	°C
Thermal resistance (system-air) .	$R_{th\,SA}$	90	K/W

Operating Range

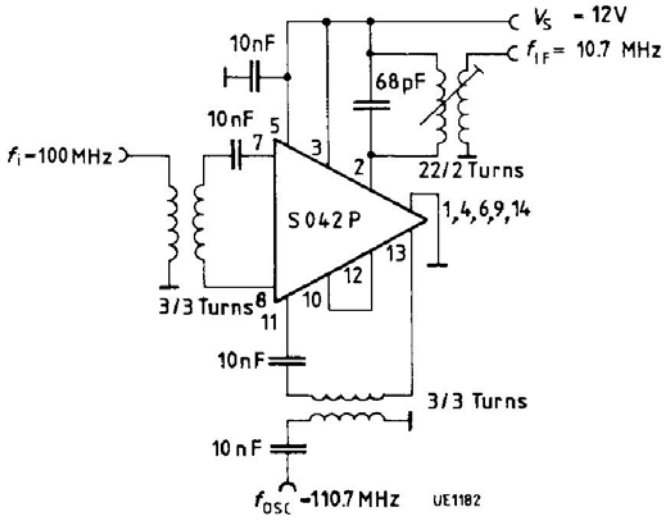
Supply voltage	V_S	4 to 15	V
Ambient temperature	T_A	–15 to 70	°C

Characteristics

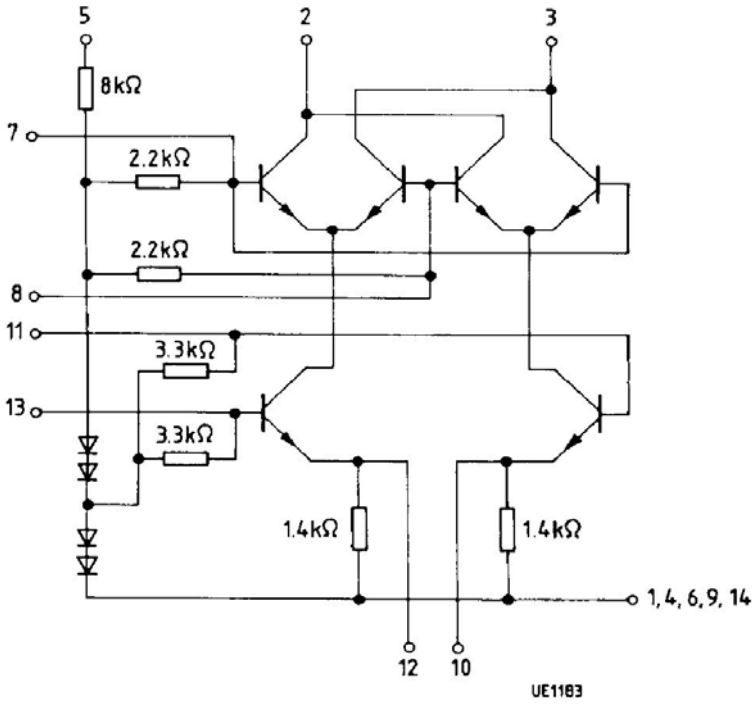
V_S = 12 V, T_A = 25 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Current consumption	$I_S = I_2 + I_3 + I_5$	1.4	2.15	2.9	mA
Output current	$I_2 = I_3$	0.36	0.52	0.68	mA
Output current difference	$I_3 - I_2$	–60		60	µA
Supply current	I_5	0.7	1.1	1.6	mA
Power gain f_i = 100 MHz, f_{OSC} = 110.7 MHz	G_P	14	16.5		dB
Breakdown voltage $I_{2,3}$ = 10 mA; $V_{7,8}$ = 0 V	V_2, V_3	25			V
Output capacitance	$C_{2\text{-}M}$, $C_{3\text{-}M}$		6		pF
Conversion transconductance f = 455 kHz	$S = \frac{I_2}{V_7 - V_8} = \frac{I_3}{V_7 - V_8}$		5		mS
Noise figure	NF		7		dB

Test Circuit



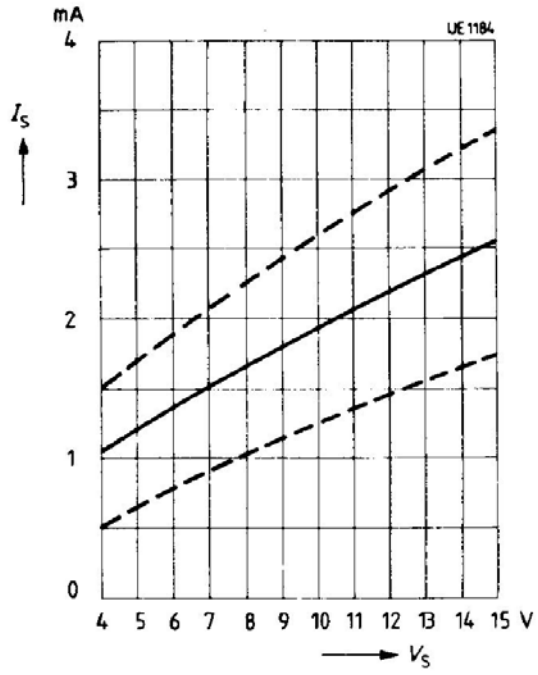
Circuit Diagram



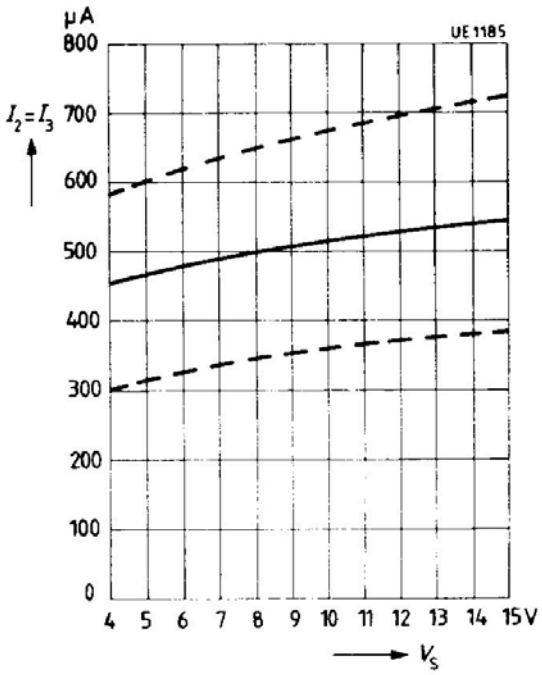
A galvanic connection between pins 7 and 8 and pins 11 and 13 through coupling windings is recommended.

A resistor of at least 220 Ω may be connected between pins 10 and 14 (ground) and between pins 12 and 14 to increase the currents and thus the conversion transconductance. Pins 10 and 12 may be connected through any impedance. In case of a direct connection between pins 10 and 12, the resistance from this pin to 14 may be at least 100 Ω. Depending on the layout, a capacitor (10 to 50 pF) may be required between pins 7 and 8 to prevent oscillations in the VHF band.

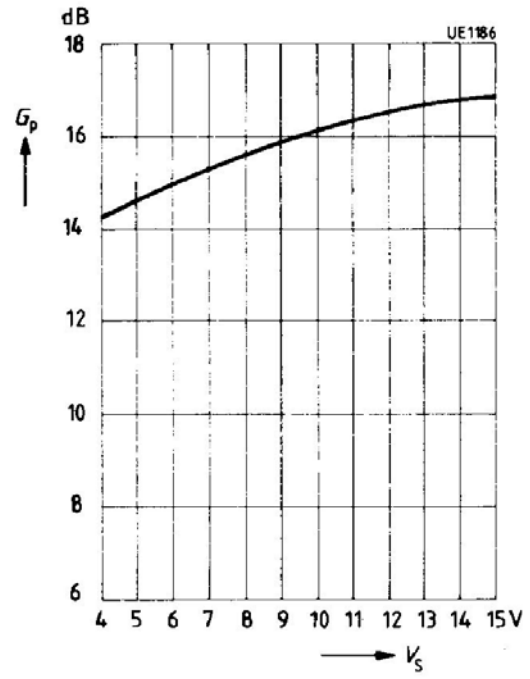
Total current consumption versus supply voltage



Output current versus supply voltage

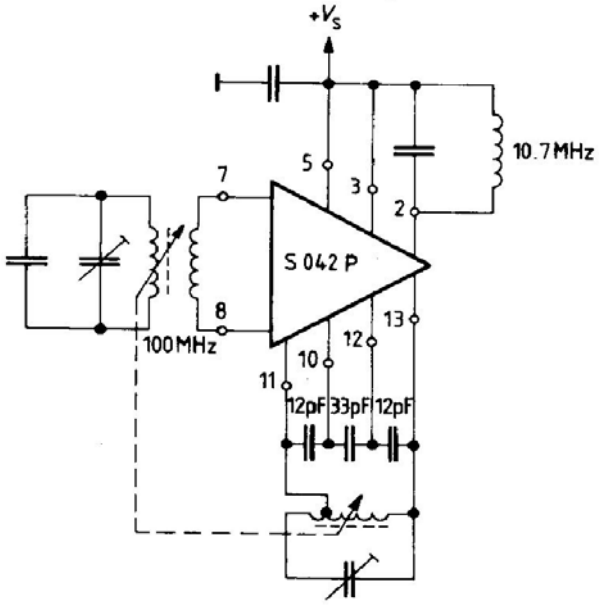


Power gain versus supply voltage

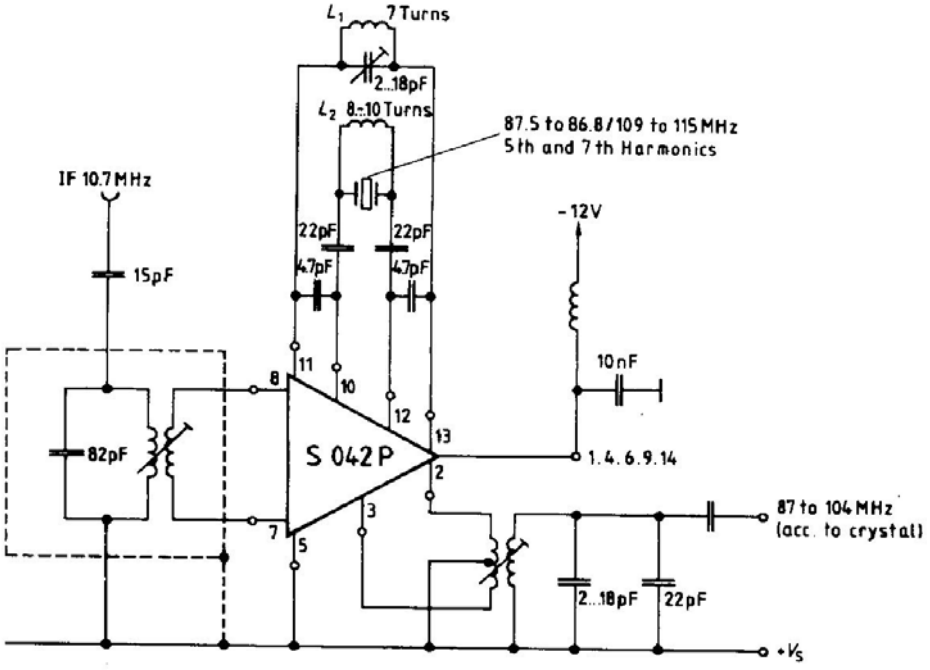


Application Circuits

FM Mixer with inductive tuning

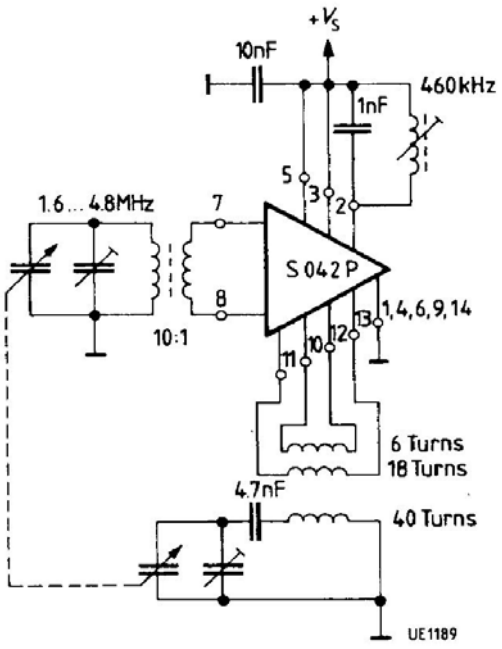


FM Mixer with crystal oscillator

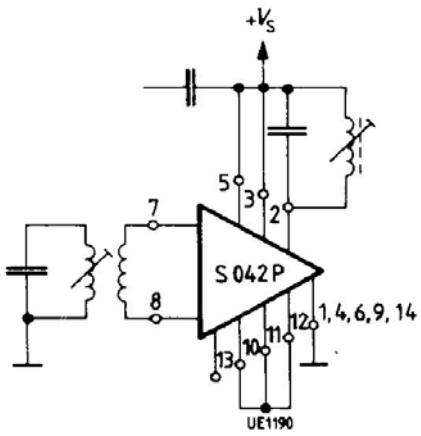


For harmonic crystals an adequate inductance is recommended between pins 10 and 12 to avoid oscillations to the fundamental.

Mixer for Short-Wave Application
in self-oscillating operation



Differential Amplifier with internal neutralization, also suited for use as limiter for frequencies up to 50 MHz or at higher currents up to 100 MHz



Symmetrische Mischer

S 042 E
S 042 P

Grenzwerte

Parameter	Kurzzeichen	Wert	Einheit
Speisespannung	U_S	15	V
Sperrschichttemperatur	T_j	150	°C
Lagertemperatur	T_s	125	°C

Alle Werte Maximalwerte

Kennwerte ($U_S = 12\,V$, $\vartheta_a = 25°C$)

Parameter	Kurzzeichen	Wert			Einheit
		min	typ.	max.	
Stromaufnahme	$I_S = I_2 + I_3 + I_5$	1,4	2,15	2,9	mA
Ausgangsstrom	$I_2 = I_3$	0,36	0,52	0,68	mA
Ausgangsstromdifferenz	$I_3 - I_2$	−60		60	mA
Versorgungsstrom	I_5	0,7	1,1	1,6	mA
Leistungsverstärkung ($f = 100\,MHz$, $f_{OSZ} = 110{,}7\,MHz$)	V_P	14	16,5		dB
Durchbruchspannung ($I_2 = I_3 = 10\,mA$; $U_7 = U_8 = 0\,V$)	U_2, U_3	25			V
Ausgangskapazität	C_2, C_3		6		pF
Mischsteilheit ($f = 455\,kHz$)	$S = \frac{I_2}{U_7 - U_8} = \frac{I_3}{U_7 - U_8}$		5		mS
Rauschzahl	F		7		dB
Wärmewiderstand Systemumgebung	R_{thSu}				K/W
S 042 E				190	
S 042 P				90	

Alle im Index erwähnten Anschlüsse beziehen sich auf S 042 P

Kurzcharakteristik

- S 042 E im Gehäuse 5 J 10 DIN 41 873 ähnlich TO-100 und S 042 P im Gehäuse DIP 14 ähnlich TO-116
- Symmetrische Mischer für Frequenzen bis 200 MHz
- Fremdsteuerung oder Betrieb mit internem Oszillator möglich
- Sehr vielseitige Einsatzmöglichkeiten: Neben den üblichen Mischeranwendungen in Empfängern, Umsetzern und Demodulatoren für AM und FM auch als elektronische Polaritätsumschalter, Multiplizierer u. ä. verwendbar
- Großer Speisespannungsbereich (4 . . . 15 V)
- Geringe Außenbeschaltung
- Hohe Mischsteilheit
- Geringes Rauschen
- Umgebungstemperatur −4 . . . 70 °C

Applikationshinweise

- Eine galvanische Verbindung zwischen Anschluß 7 und 8 bzw. 11 und 13 über Koppelwicklungen wird empfohlen.
- Zwischen Anschluß 10 und Masse und zwischen Anschluß 12 und Masse darf je ein Widerstand von mindestens 220 Ω geschaltet werden, der die Ströme und damit die Steilheit erhöht.
- Die Anschlüsse 10 und 12 dürfen durch eine beliebige Impedanz verbunden werden.
- Sind die Anschlüsse 10 und 12 direkt verbunden, darf der Widerstand von dieser Verbindung nach Masse mindestens 100 Ω betragen.
- Je nach Aufbau macht sich ein Kondensator von 10 pF bis 50 pF zwischen den Anschlüssen 7 und 8 erforderlich, um Schwingungen im VHF-Bereich zu unterbinden.
- Die Eingangssignale werden ausgangsseitig unterdrückt.

Maßbild

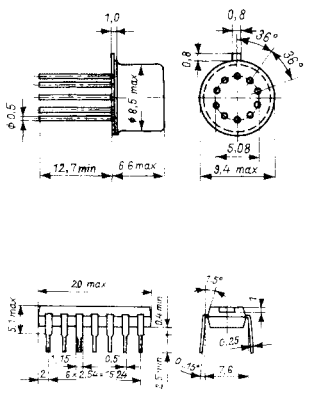


Bild 1: Maßbild für das Gehäuse TO-100 (oben) und TO-116 (unten)

Innenschaltung

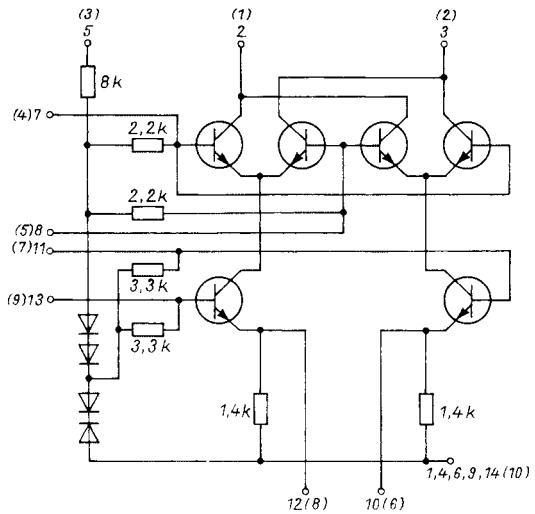


Bild 2: Innenschaltung (Anschlüsse in Klammern gelten für S 042 E)

Kennlinien

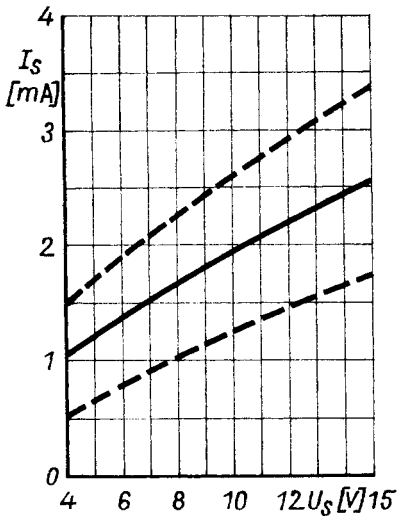


Bild 3: Gesamtstromaufnahme I_S als Funktion der Speisespannung U_S

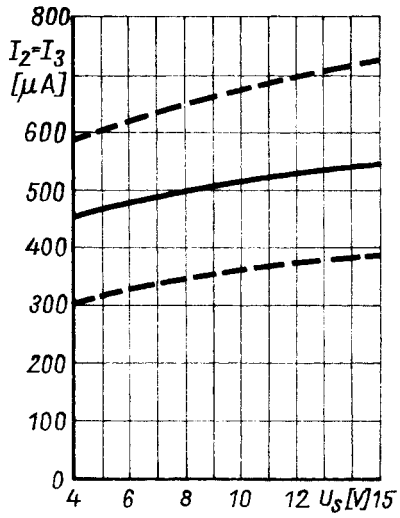


Bild 4: Ausgangsstrom $I_2 = I_3$ als Funktion der Speisespannung U_S

Applikationsschaltungen

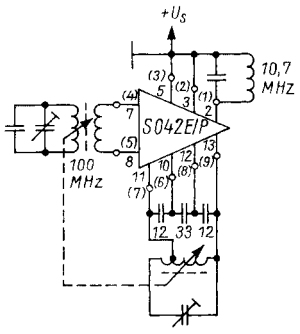


Bild 5: Anwendungsschaltung UKW-Mischer mit induktiver Abstimmung (Anschlüsse in Klammern für SO 42 E)

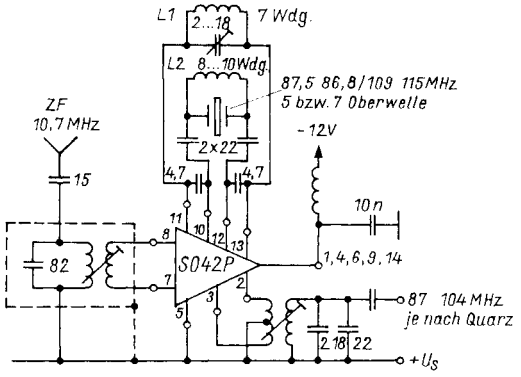


Bild 6: Anwendungsschaltung UKW-Mischer mit Quarzoszillator; bei Obertonquarzen empfiehlt sich eine entsprechende Induktivität zwischen Anschluß 10 und 12, um Schwingen auf der Grundfrequenz zu verhindern.

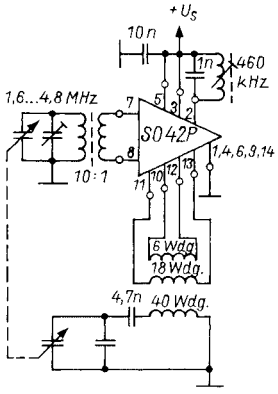
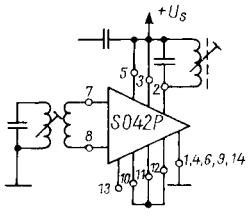


Bild 7: Anwendungsschaltung eines Mischers für den Kurzwellenbereich im selbstschwingenden Betrieb; diese Schaltung ist grundsätzlich auch für den Lang- und Mittelwellenbereich verwendbar.

Bild 8: Differenzverstärker mit interner Neutralisation, auch als Begrenzer geeignet. Der nominelle Frequenzbereich geht bis 50 MHz, bei erhöhtem Strom sind maximal 100 MHz möglich.



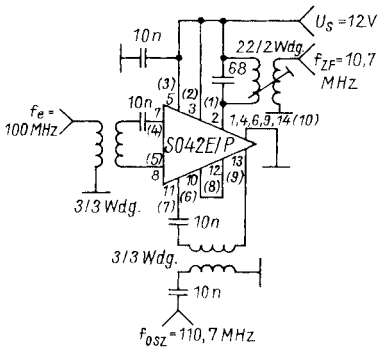


Bild 9: Meßschaltung (Anschlüsse in Klammern für S 042 E)