THEME BAC 2007
STATION DE NETTOYAGE ROBOTISEE

Sciences Techniques Industrielles

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BESANCON

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1. Mise en situation

1.1 Introduction

Pour ce Thème de BAC 2007, nous vous proposons d'étudier un robot aspirateur conçu par le constructeur IRobot.

I Robot s'est depuis longtemps engagé à fabriquer des produits robotiques qui rendent plus sûre et plus facile la vie de personnes de tous horizons. Au cours de ces 14 dernières années, IRobot a conçu et fabriqué des produits novateurs pour l'armée américaine, les forces de l'ordre, les secteurs du nettoyage industriel et des jouets, et aujourd'hui, pour le marché de consommation.

Le Roomba est un aspirateur automatique qui balaie et aspire tout seul les sols domestiques. Il suffit de l'allumer et de partir pour qu'il nettoie l'intégralité du sol, en parvenant même à atteindre les endroits difficiles d'accès, tels que le sol sous les lits, les divans et les armoires.

Le Roomba fait appel à un **processus de nettoyage en trois étapes** afin de ne manquer aucune saleté et de laisser derrière lui un sol parfaitement propre. Grâce à une technologie de navigation intelligente, le Roomba utilise un processus de trajectoire circulaire.

Toutes les particules sont collectées dans un **compartiment sans sac** facile à retirer, à vider et à remettre en place. Grâce à ses algorithmes d'intelligence artificielle, il couvre tout le sol pendant le processus de nettoyage automatique.

Équipé d'un **capteur de contours de la pièce**, le Roomba se déplace aisément le long des murs et autour des meubles afin de nettoyer l'intégralité du sol.
Sans accessoire supplémentaire, le Roomba est extrêmement léger (seulement 2,9 kg) et très facile à porter et à ranger.
Le Roomba se révèle efficace sur presque tous les sols domestiques, dont le parquet en bois dur, le linoléum, les carreaux et le stratifié, ainsi que sur les tapis à poil ras et moyens.

Le Roomba effectue même automatiquement la transition entre différents revêtements de sol.

Une **unité de cloisonnement virtuel** vient compléter l'équipement du Roomba : elle crée un mur invisible à l'aide d'un rayon infrarouge de 4 mètres de large maximum afin de bloquer les passages ouverts ou de diviser de grandes pièces.

Des **capteurs de marches** intégrés et un système de navigation intelligent permettent également au Roomba de nettoyer ainsi jusqu'au bord sans jamais tomber.

1.2 Eléments constitutifs du système technique

1. L'unité de cloisonnement virtuel :

L'unité de cloisonnement virtuel sert à délimiter la zone de travail de votre aspirateur Roomba dans la pièce ou l'endroit à nettoyer.
Cette unité est en mesure de bloquer des passages de porte d'une largeur maximale de 4m. L'unité de cloisonnement virtuel sert à bloquer des passages ouverts ou à délimiter un secteur dans une grande pièce.

2. Le socle de chargement :

L'aspirateur Roomba retourne automatiquement à son socle lorsque la batterie est presque vide ou quand il a fini le nettoyage. Il se recharge en 3 heures.

L'aspirateur Roomba est toujours chargé lorsque vous en avez besoin.

3. La télécommande :

La télécommande permet d'éteindre puis d'allumer l'aspirateur.
Elle permet de le piloter vers des zones précises.
Elle dispose de trois boutons permettant d'activer les modes « Clean », « Spot », et « Max ».
Le nettoyage est ainsi facilité et adaptée à la superficie grâce à un indicateur de détection de saleté.

4. La batterie APS rechargeable :

Inclue dans le robot, cette batterie de 14.4 volts NiMh est compatible avec tous les modèles de Roomba.

Grâce à la technologie APS (Advanced Power System), la batterie se recharge plus vite que les générations précédentes. Elle a une autonomie 25% supérieure et une durée de vie supérieure de moitié.

5. Le chargeur de batterie :

L'aspirateur peut être relié directement par l'utilisateur au chargeur pour recharger sa batterie à partir du secteur.

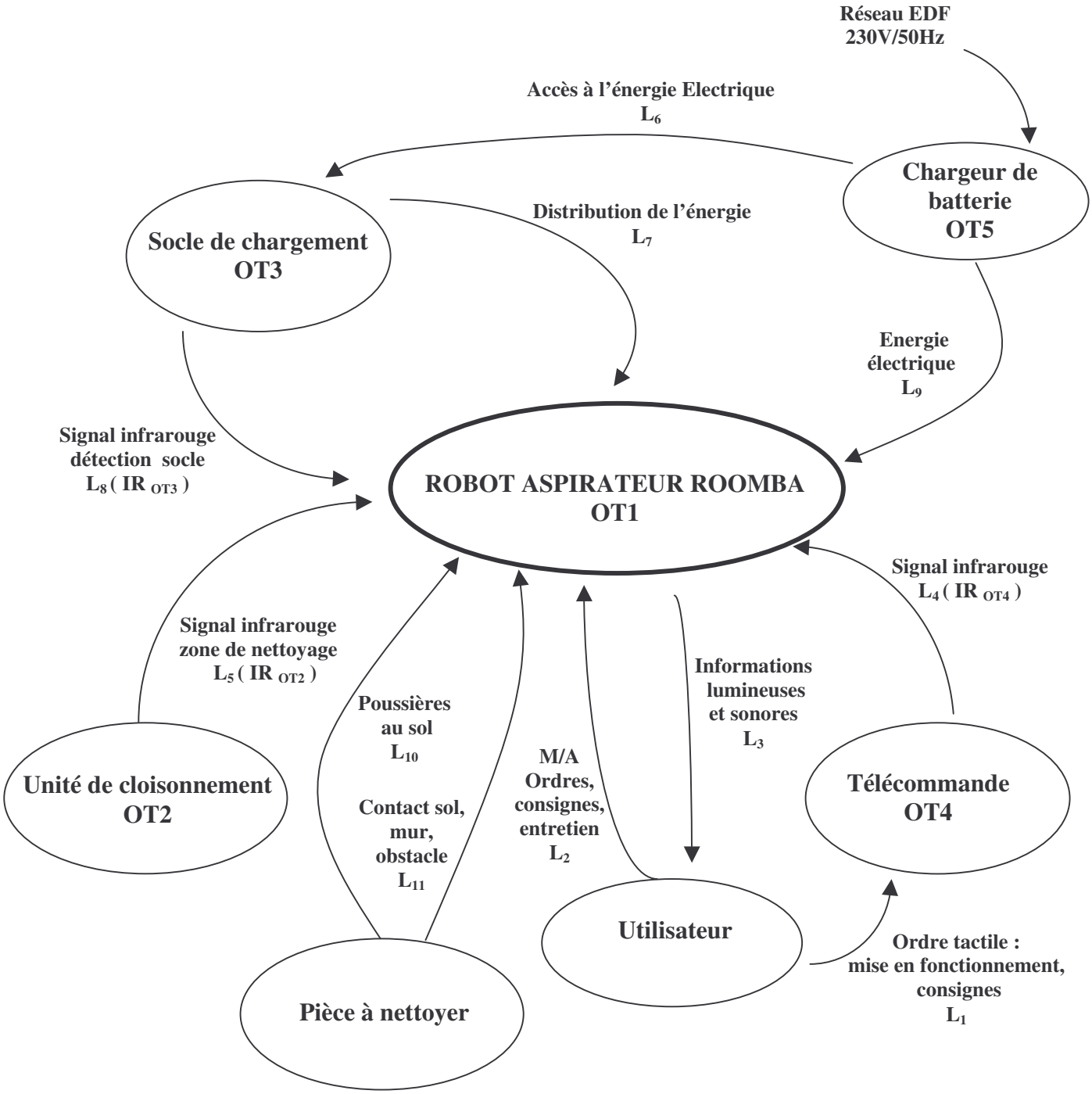
1.3 Limite du système technique

Le robot Roomba est prévu pour un usage domestique, Il nettoie tous types de surfaces lisses (carrelages, parquets, lino). Il sera difficile d'opérer sur des surfaces telles que la moquette ou les sols rugueux.
L'aspirateur dispose d'un ramasse poussière de capacité relativement réduite, ce qui peut devenir un inconvénient si la pièce est particulièrement sale.

L'objectif terminal de cette étude est de modifier une structure existante : à partir de la partie opérative du robot, le travail consistera à réaliser la partie commande.

2. Description fonctionnelle du système technique

2.1 Diagramme Sagittal



2.2 Eléments du système pris deux à deux

Utilisateur - Télécommande

- L_1 : L'utilisateur par appui tactile, envoie des informations de mise en fonctionnement ou d'arrêt, des consignes de nettoyage (mode : Clean, Max, ou Spot), de retour au socle de chargement ou d'orientation du robot.

Utilisateur - Robot

- L_2 : L'utilisateur met en place le robot, donne des informations de mise en fonctionnement ou d'arrêt, des consignes de nettoyage (mode : Clean, Max, ou Spot), de retour au socle de chargement , et entretient le robot (vidage du bac à poussières, changement des filtres,...).
- L_3 : Il reçoit des informations lumineuses (état de charge de la batterie, voyant M/A, voyant pièce sale) et sonores (bip M/A, bip batterie déchargée, et bip état de surface).

Télécommande - Robot aspirateur

- L_4 : La télécommande envoie un signal, onde infrarouge représentatif du fonctionnement désiré.

Unité de cloisonnement-Robot aspirateur:

- L_5 : L'unité de cloisonnement envoie un signal infrarouge au robot permettant à celui - ci de délimiter sa zone de nettoyage.

Socle de chargement-Robot aspirateur

- L_6 : Le socle de chargement reçoit l'énergie électrique régulée par le chargeur de batterie.
- L_7 : OT_3 distribue l'énergie électrique nécessaire au chargement de la batterie APS.
- L_8 : Le socle de chargement émet un signal infrarouge permettant au robot de se positionner pour une éventuelle charge.

Chargeur de batterie-Robot aspirateur :

- L_9 : Le chargeur fournit l'énergie nécessaire à la charge de la batterie du robot APS. Cette énergie peut être transmise directement au robot ou par l'intermédiaire de OT_3.

Pièce à nettoyer-Robot aspirateur :

- L_{10} : Le robot aspire et ramasse la poussière dans un tiroir : une partie (la plus fine) est aspirée, l'autre est balayée et récoltée dans une autre partie du collecteur.
- L_{11} : Le robot s'adapte à la pièce à nettoyer en détectant les contours, les obstacles, les différences de niveau (escalier par exemple). De plus si le contact entre le sol et le robot est interrompu, ce dernier fige ses mouvements automatiquement.

2.3 Approche des milieux associés

Milieu humain :

L'appareil doit être simple d'utilisation. L'utilisateur doit pouvoir contrôler visuellement l'évolution du cycle de nettoyage.
Le système doit rester relativement léger, d'un encombrement réduit et facilement transportable. L'utilisateur doit pouvoir vider facilement le ramasse poussière et également procéder à une maintenance des accessoires de nettoyage du robot (filtre, dépoussiérage des capteurs).

Milieu physique :

L'objet doit pouvoir être déplacé facilement et doit pouvoir évoluer sur tous types de surfaces lisses. Le robot aspirateur doit disposer d'une coque en matière plastique suffisamment solide pour résister aux petits chocs frontaux lors de ces multiples déplacements.
De par la mobilité du robot, l'alimentation du système doit être prélevée sur batterie rechargeable.

Milieu technique :

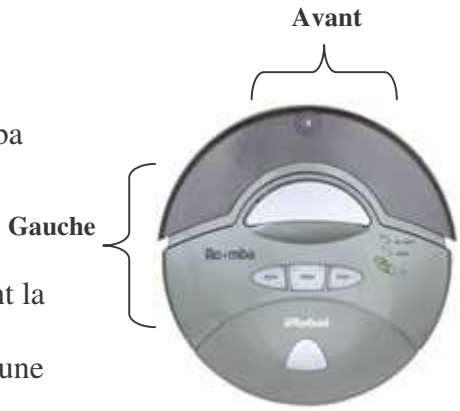
Rechargement de l'ensemble sur secteur EDF (230V / 50hz).
L'autonomie de la batterie doit être d'environ 2 heures.

Milieu économique :

Le coût du système technique ne dépasse pas 350€, et reste compétitif dans la gamme des prix grand public des aspirateurs autonomes.

3. Analyse fonctionnelle de l'OT_1 « Robot aspirateur Roomba »

3.1 Fonction d'usage :



Après avoir chargé sa batterie APS, le robot aspirateur Roomba procède à l'enlèvement de la poussière dans une pièce.

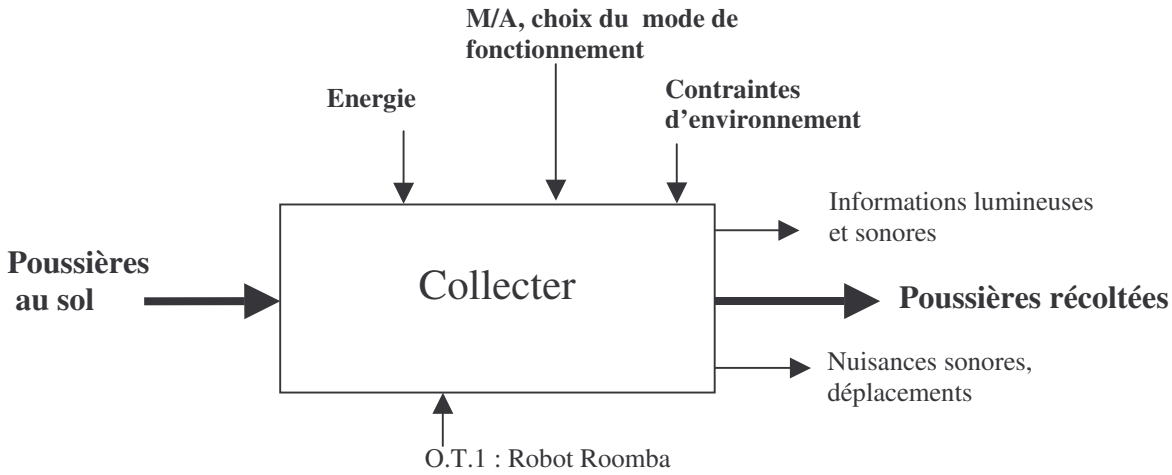
Le robot possède 3 modes de fonctionnement :

- En mode « **Clean** »l'aspirateur détermine automatiquement la trajectoire optimale pour nettoyer l'ensemble de la pièce.
- En mode « **Spot** » il concentre le pouvoir d'aspiration sur une zone de 1 m de diamètre.
- En mode « **Max** », il allonge la durée de nettoyage jusqu'à 95 minutes lorsque la zone à nettoyer est particulièrement sale.

3.2 Etude fonctionnelle de niveau 1 et 2 :

3.2.1 Fonction globale : Collecter des poussières à partir de consignes.

3.2.2 Schéma fonctionnel de niveau 1 :

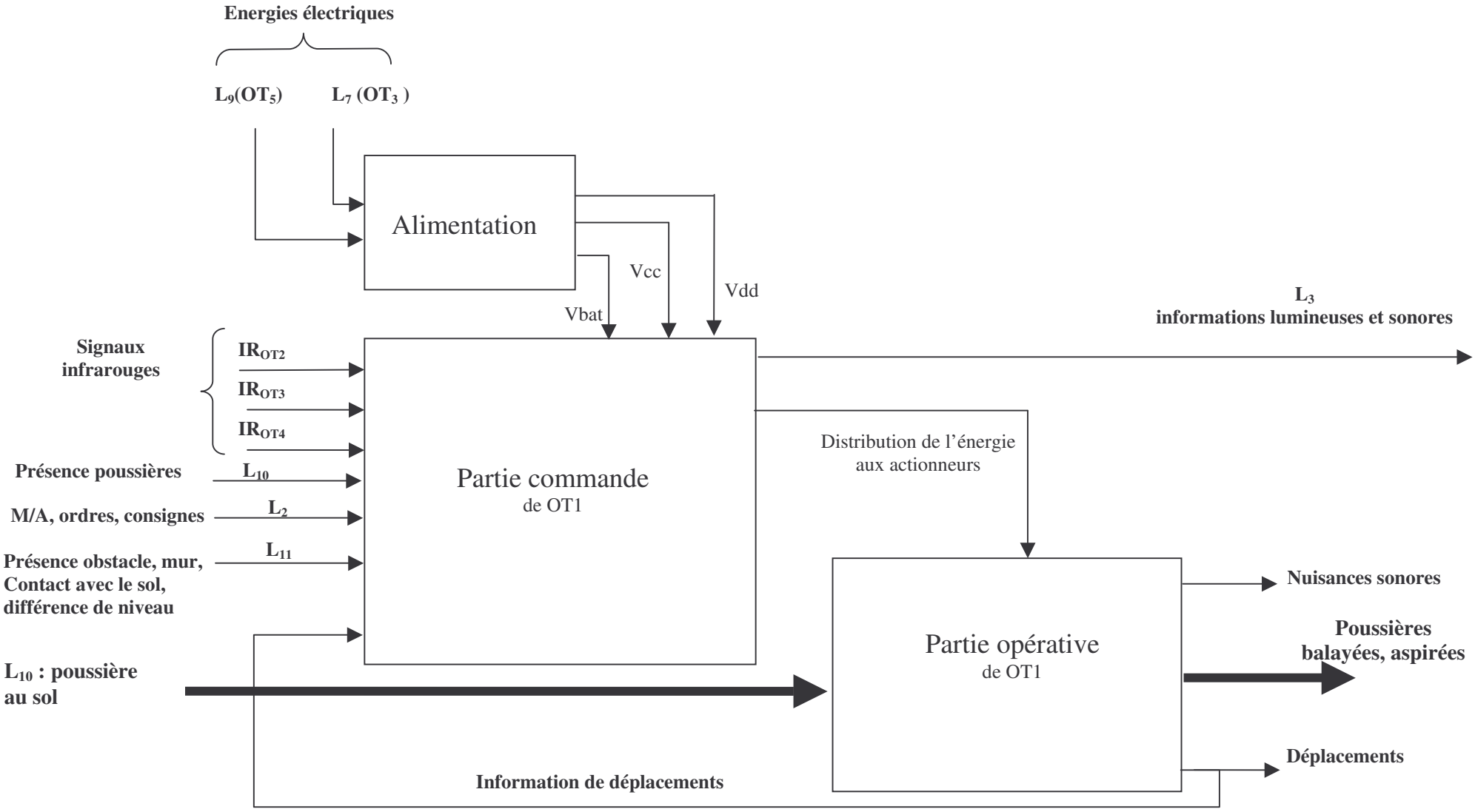


Matière d'œuvre :

Elle est de type matériel : poussière présente en faible ou grande quantité au sol.

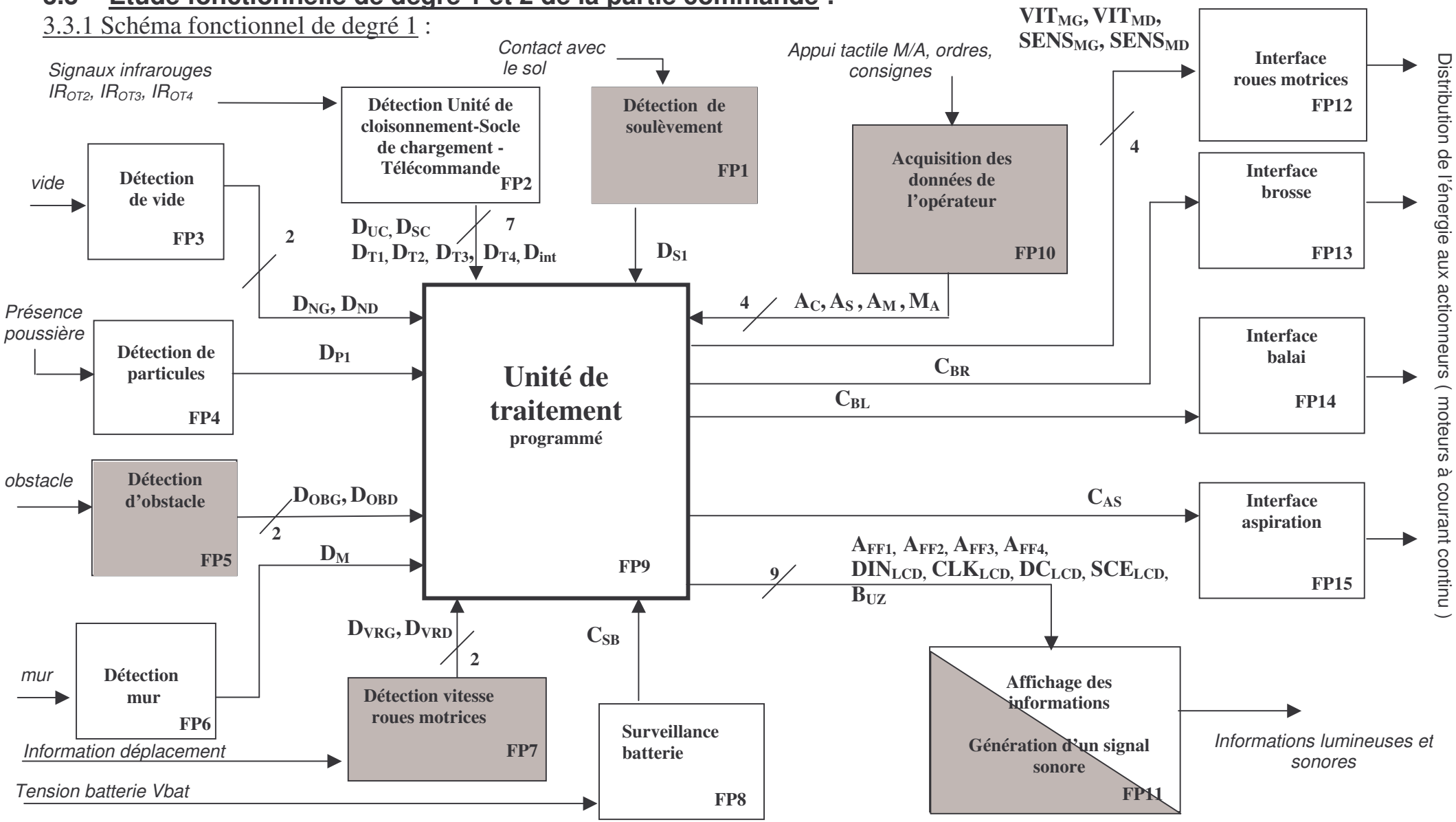
Matière d'œuvre entrante : poussières au sol
Matière d'œuvre sortante : poussières dans le collecteur de particules

3.2.3 Schéma fonctionnel de niveau 2 de l'objet technique OT1 « Robot aspirateur » :



3.3 Etude fonctionnelle de degré 1 et 2 de la partie commande :

3.3.1 Schéma fonctionnel de degré 1 :



3.3.2 Définition des fonction principales :

Remarques : Les fonctions principales grisées sont intégrées à la carte fond de panier et/ou au robot.

FP1 : Détection de soulèvement :

3 capteurs permettent au robot de détecter sa position (posé sur le sol ou soulevé). La fonction fait appel à des interrupteurs mécaniques : les trois interrupteurs doivent être fermés pour que le robot soit détecté « au sol ».

- Entrée : Contact avec le sol.
- Sortie : D_{S1}: Signal logique compatible TTL

FP2 : Détection Unité de cloisonnement -Socle de chargement-Télécommande :

Un capteur « de distance » infrarouge reçoit les informations provenant des 3 autres objets techniques du système, et transmet à FP9 des ordres propres au fonctionnement désiré.

- Entrée : $IR_{OT2,}$ $IR_{OT3,}$ $IR_{OT4,}$: signaux infrarouges modulés en amplitude représentatifs du fonctionnement de chaque OT.
- Sortie : D_{UC} : signal logique compatible TTL
- Sortie : D_{SC} : signal analogique ; tension proportionnelle à la distance d'éloignement
- Sortie : $D_{T1,}$ $D_{T2,}$ $D_{T3,}$ D_{T4} : Information numérique : Code binaire sur 4 bits.
- Sortie : D_{INT} : signal logique compatible TTL

FP3 : Détection de vide :

Pour assurer la protection du robot vis à vis des différences éventuelles de niveau, Roomba doit pouvoir détecter un escalier, un vide grâce à 4 capteurs de niveau situés sous la coque.

- Entrée : Différence de niveau.
- Sortie : D_{NG}, D_{ND} : signaux logiques compatible TTL.

FP4 : Détection de particules :

Des capteurs piézo-électriques permettent de reconnaître la densité de la poussière, une procédure de nettoyage particulière est alors lancée : Le robot tourne dans le sens horaire sur le secteur particulièrement sale.

- Entrée : Quantité de poussière.
- Sortie : D_{P1} : signal logique compatible TTL.

FP5 : Détection d'obstacle :

Le robot est muni d'un pare-chocs qui amortit les chocs frontaux. Lorsqu'un obstacle se présente, Roomba le heurte et change de direction (il recule puis tourne pour se réorienter). La procédure de nettoyage n'est pas interrompue. La fonction fait appel à deux diodes émettrices IR et deux phototransistors récepteurs.

- Entrée : Présence d'obstacle.
- Sortie : D_{OBG}, D_{OBD} : signaux logiques compatible TTL.

FP6 : Détection mur :

Les cloisons et murs des pièces à nettoyer permettent au robot de se diriger et de calculer ses propres trajectoires. Un capteur (émetteur et récepteur IR) situé dans le pare-chocs détecte la paroi de droite.

- Entrée : Distance au mur
- Sortie : D_M : signal logique compatible TTL

FP7 : Détection vitesse roues motrices :

Le système doit pouvoir contrôler sa vitesse de progression. Deux capteurs de vitesse (une roue dentée de 40 dents associée à un émetteur-récepteur infrarouge sur chaque roue motrice) permettent d'obtenir deux signaux dont la fréquence est proportionnelle à la fréquence de rotation des moteurs.

- Entrée : Fréquence de rotation
- Sortie : D_{VRG}, D_{VRD} : signaux logiques de fréquence variable compatible TTL.

FP8 : Surveillance batterie :

La batterie APS permet au robot de fonctionner pendant une durée de 120min maximum. Un dispositif permet à FP9 de connaître le seuil minimum de charge de la batterie. Si le seuil critique est atteint, un voyant clignote et le robot cherche son socle de chargement pour revenir effectuer une recharge.

- Entrée : V_{BAT} : signal analogique; tension de la batterie
- Sortie : C_{SB} : signal logique compatible TTL qui ordonne au robot une nouvelle charge de batterie.

FP9 : Unité de traitement :

On utilise une carte de gestion à base de microcontrôleur 68HC711 E9 située au centre de la carte fond de panier. En fonction de l'état des capteurs infrarouges et des informations provenant de OT_2 (Unité de cloisonnement), OT_3 (Socle de chargement), et OT_4 (Télécommande), FP9 envoie des ordres de commandes aux différents actionneurs du robot, et des informations visuelles et sonores pour l'utilisateur.

- Entrée : D_{S1},voir FP1;
  D_{UC}, D_{SC}, D_{INT}, D_{T1}, D_{T2}, D_{T3}, D_{T4} voir FP2 ; D_{NG}, D_{ND}, voir FP3 ;
  D_{P1}, voir FP4 ; D_{OBG}, D_{OBD} voir FP5 ; D_M voir FP6,
  D_{VRG},D_{VRD} voir FP7 ; C_{SB} voir FP8, et A_C, A_S , A_M, M_A voir FP10.
- Sortie : A_{FF1}, A_{FF2} , A_{FF3}, A_{FF4}, CKL_{LCD} ,DIN_{LCD}, DC_{LCD} SCE_{LCD}, B_{UZ} voir FP11 ;
  $SENS_{MG}$, $SENS_{MD}$, VIT_{MG},VIT_{MD} voir FP12; C_{BR}, voir FP13; C_{BL}, voir FP14; C_{AS}, voir FP15.

FP10 : Acquisition des données de l'opérateur :

A défaut d'utiliser la télécommande, l'opérateur peut directement commander le robot grâce à 4 touches situées sur la coque (touche M/A, touches Clean, Spot et Max).

- Entrée : Appui tactile de l'opérateur.
- Sortie : A_C, A_S, A_M, M_A : Informations binaires; signal logique compatible TTL.

FP11 : Affichage des informations- Génération d'un signal sonore :

Le robot possède des voyants et un indicateur sonore qui renseignent sur l'état et le mode de fonctionnement du mobile. Un afficheur à cristaux liquides indique à l'utilisateur le temps d'aspiration et l'état de charge de la batterie (chargée, déchargée).

- Entrée : $A_{FF1}, A_{FF2}, A_{FF3}, A_{FF4}$: mot binaire de 4 bits pour la commande des voyants du robot (voyant max, voyant clean, voyant power, voyant spot).
  CLK_{LCD}, DIN_{LCD}, DC_{LCD}, SCE_{LCD} : Informations numériques ; mot binaire de 4 bits nécessaire au fonctionnement de l'afficheur LCD.
  B_{UZ} : signal logique compatible TTL (de fréquence 400Hz pour la génération d'un signal sonore).
- Sortie : Informations visuelles et sonores.

FP12 : Interface roues motrices :

La progression du robot est assurée par deux moteurs à courant continu situés de chaque côté et à proximité des roues motrices du mobile. La commande s'effectue grâce à 4 signaux issus de FP9 qui dictent le sens et la vitesse de progression de chaque roue.

- Entrée : $SENS_{MG}, SENS_{MD}$: signaux logiques représentatifs du sens
  VIT_{MG}, VIT_{MD} : signaux d'horloge à rapport cyclique variable
- Sortie : Alimentation limitée en énergie des moteurs.

FP13 : Interface brosse :

Le robot est muni d'une brosse centrale qui tourne dans le sens horaire et qui propulse la poussière dans le compartiment ramasse poussière. La brosse est actionnée par un moteur à courant continu protégé contre les éventuelles surcharges.

- Entrée : C_{BR} : signal logique compatible TTL de mise en fonctionnement du moteur brosse.
- Sortie : Alimentation en énergie du moteur brosse.

FP14 : Interface balai :

Roomba est équipé d'un petit balai situé à gauche de la coque qui ramène la poussière au centre du robot. La partie opérative est constituée d'un axe non rigide munis de 2 balais, ce qui facilite sa rotation lorsque le mobile heurte un obstacle. L'ensemble est actionné par un moteur à courant continu.

- Entrée : C_{BL} : signal logique compatible TTL de mise en fonctionnement du moteur balai.
- Sortie : Alimentation en énergie du moteur balai

Note : Le moteur consomme 60mA à vide est 80mA en charge, la résistance du moteur $R_M = 12.5\Omega$.

FP15 : Interface aspiration :

La poussière fine non balayée par la brosse est aspirée dans le compartiment ramasse poussière. Le moteur à courant continu qui commande l'aspiration de la poussière n'est pas visible et se situe dans le compartiment ramasse poussière.

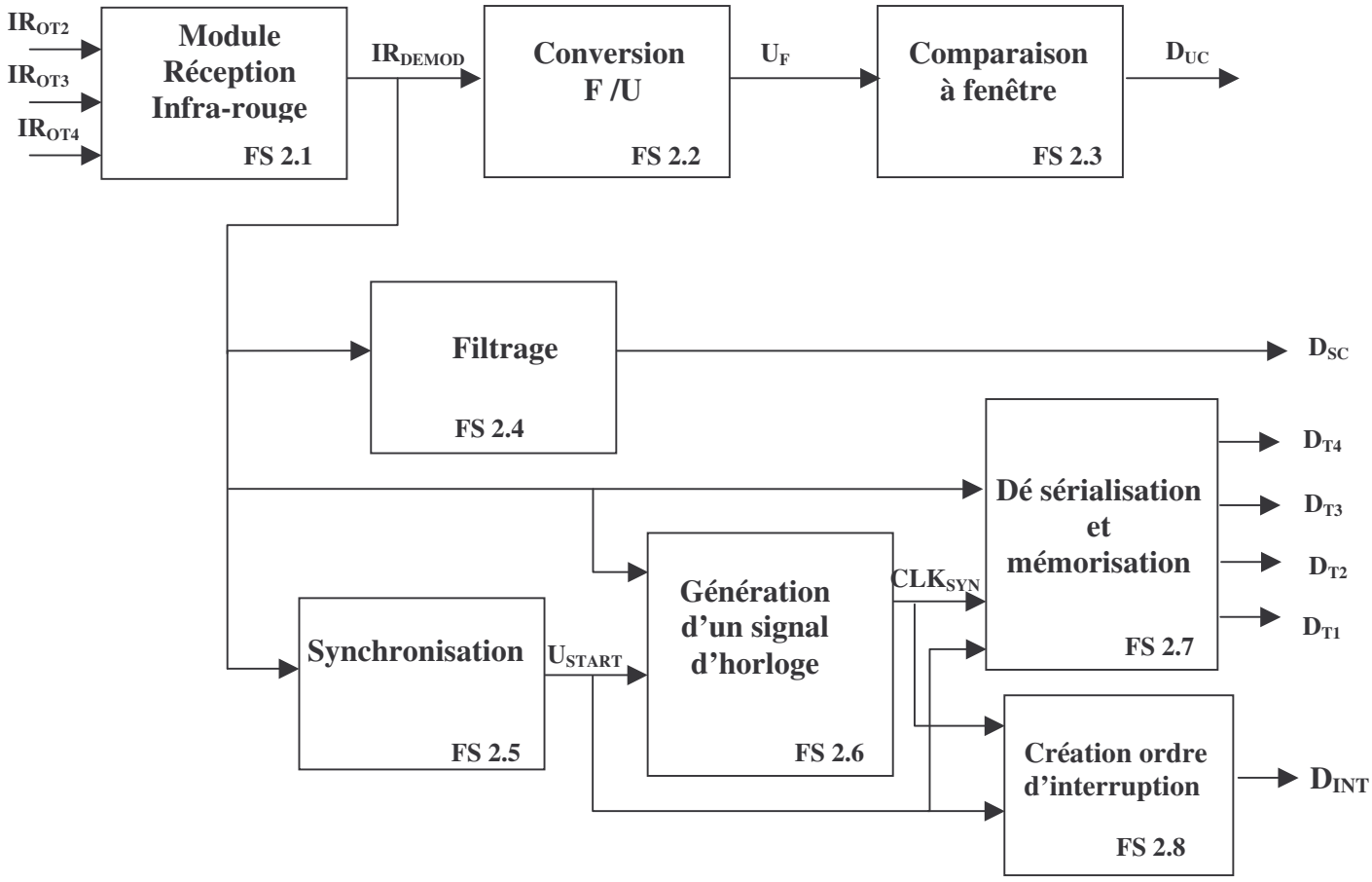
- Entrée : C_{AS} : signal logique compatible TTL de mise en fonctionnement du moteur aspirateur de déchets.
- Sortie : Alimentation en énergie du moteur aspiration.

Note : Le moteur consomme 150mA , la résistance du moteur $R_M = 22.5\Omega$.

3.3.3 Etude fonctionnelle de degré 2 :

a) Schéma fonctionnel de degré 2 de FP 2 « Détection OT_2, OT_3, OT_4 »

Le capteur qui détecte les objets techniques du système est équipé d'une optique permettant de capter le signal dans toutes les directions. Chaque OT émet son signal propre.



Définition des fonctions secondaires de FP 2 :

FS 2.1 : Module Réception Infra-rouge :

Entrée :
- IR_{OT2} : signal IR de porteuse F = 38khz modulé en amplitude à 500 Hz
- IR_{OT3} : signal IR de porteuse F = 38khz modulé en amplitude par un code binaire.
- IR_{OT4} : signal IR de porteuse F = 38khz modulé en amplitude par un code binaire fonction de la touche appuyée (8 touches différentes).

Sortie :
- IR_{DEMOD} : signal numérique représentant l'ordre envoyé par OT_2, ou OT_3, ou OT_4.

La fonction est réalisée par un composant intégré au pare chocs du robot. Il capte, filtre et démodule le signal.

FS 2.2 : Conversion F/U :

Entrée :
- signal numérique issu de FS 2.1.

Sortie :
- U_F : tension proportionnelle à la fréquence du signal reçu.

FS 2.3 : Comparaison à fenêtre :

Entrée :
- signal analogique issu de FS 2.2.

Sortie :
- D_{UC} : signal binaire compatible TTL au niveau haut si le signal est reçu de OT2. (signal de fréquence 500hz)

FS 2.4 : Filtrage :

Entrée :
- signal numérique issu de FS 2.1.

Sortie :
- D_{SC} : Information analogique; tension proportionnelle à l'éloignement de OT3.

FS 2.5 : Synchronisation :

Entrée :
- signal numérique issu de FS 2.1.

Sortie :
- U_{START} : signal binaire qui déclenche la génération d'un signal d'horloge lorsque le début de trame est détecté et qui déclenche la mémorisation du code en fin de trame.

FS 2.6 : Génération d'un signal d'horloge :

Entrée :
- signal binaire issu de FS 2.5.

Sortie :
- CLK_{SYN} : Signal d'horloge qui rythme la désérialisation de la trame.

FS 27 : Dé sérialisation et mémorisation :

Entrée :
- signal d'horloge issu de FS 2.6.

Sortie :
- D_{T1}, D_{T2}, D_{T3}, D_{T4} : Information numérique; Code binaire représentatif des touches appuyées sur la télécommande.

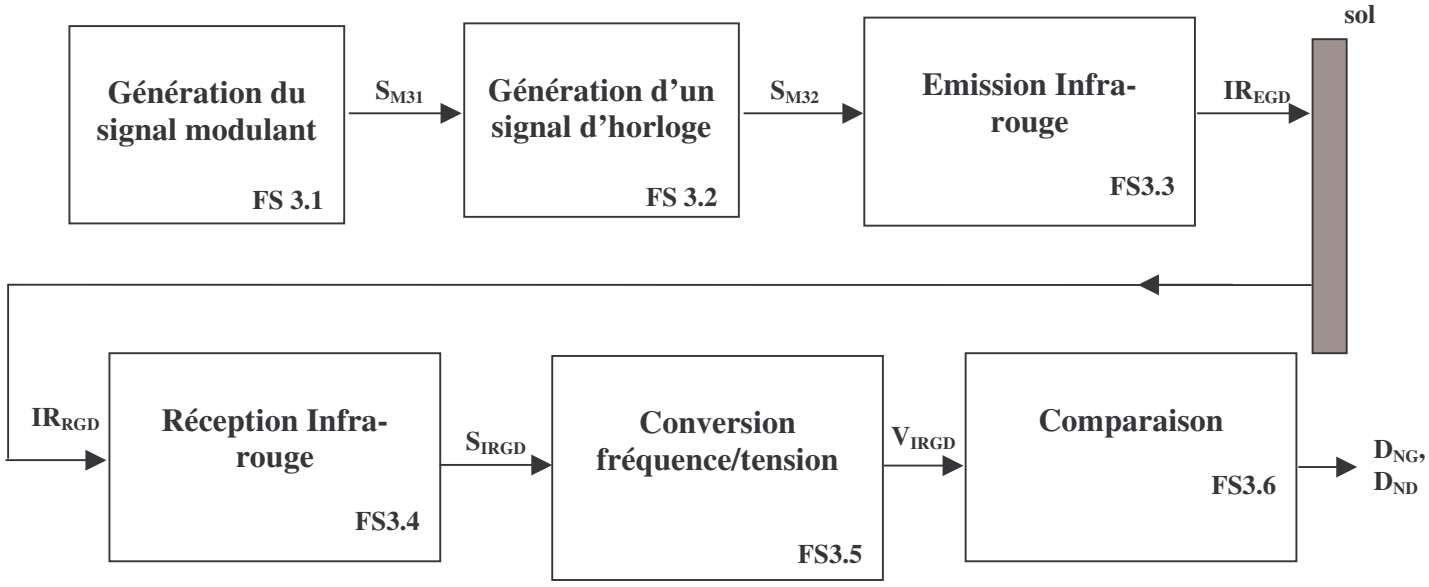
FS 2.8 : Création ordre d'interruption:

Entrée :
- signal d'horloge issu de FS 2.6.
- signal binaire issu de FS 2.5.

Sortie :
- D_{INT} **:** signal binaire qui déclenche une demande d'interruption pour FP9 et indique à FP9 de venir lire le code de la touche appuyée.

b) Schéma fonctionnel de degré 2 de FP 3 « Détection de vide »

Un signal modulé en amplitude (pour éviter les perturbations dues à la lumière) est émis en permanence par les diodes infrarouges situées sous le robot à l'avant gauche et droit. La présence du sol réfléchit l'onde sur les récepteurs. Les émetteurs et récepteurs infrarouge sont logés dans le pare choc du robot.



Définition des fonctions secondaires de FP 3 :

FS 3.1 : Génération du signal modulant :

Entrée :
- aucune

Sortie :
- S_{M31} : signal d'horloge de fréquence 1khz de rapport cyclique 0,3.

FS 3.2 : Génération d'un signal d'horloge :

Entrée :
- signal modulant issu de FS 3.1.

Sortie :
- S_{M32} : signal d'horloge de fréquence 12khz, de rapport cyclique 0,5 modulé en amplitude.

FS 3.3 : Emission Infra-rouge :

Entrée :
- signal modulé en amplitude issu de FS 3.2.

Sortie :
- IR_{EGD} : signaux IR émis à gauche et droite sous le robot.

FS 3.4 : Réception Infra-rouge :

Entrée :
- signaux IR réfléchis par le sol à gauche et à droite sous le robot.

Sortie :

- S_{IRGD} : signaux image des signaux IR reçus à gauche et à droite.

FS 3.5 : Conversion fréquence/tension :

Entrée :
- signaux issus de FS 3.4.

Sortie :

- V_{IRGD} : signaux analogiques proportionnels à la fréquence des signaux IR reçus à gauche et à droite.

FS 3.6 : Comparaison :

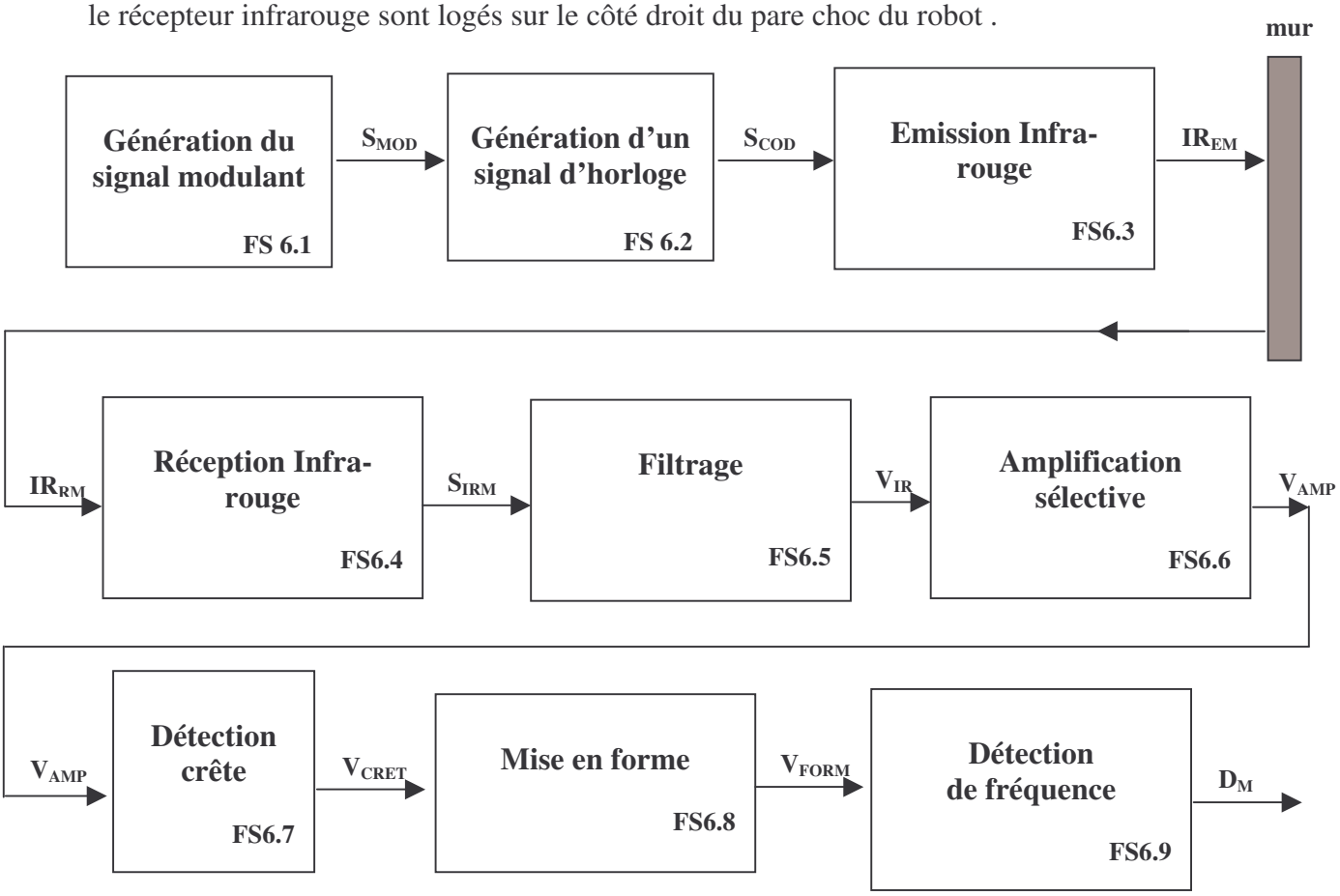
Entrée :
- signaux issus de FS 3.5.

Sortie :

- D_{NG}, D_{ND} : signaux logiques indiquant une différence de niveau (vide) à gauche ou à droite.

c) Schéma fonctionnel de degré 2 de FP 6 « Détection mur »

Un signal infra-rouge modulé en amplitude (pour éviter les perturbations dues à la lumière et à d'autres systèmes utilisant des IR) est émis en permanence. La présence d'un mur réfléchit l'onde (robot positionné parallèlement au mur) sur le récepteur. L'émetteur et le récepteur infrarouge sont logés sur le côté droit du pare choc du robot .



Définition des fonctions secondaires de FP 6 :

FS 6.1 : Génération du signal modulant :

Entrée
- Aucune

Sortie :
- S_{MOD} : signal d'horloge de fréquence F =210Hz

La fonction est réalisée grâce à un astable à portes logiques.

FS 6.2 : Génération d'un signal d'horloge :

Entrée :
- signal d'horloge modulant issu de FS 6.1

Sortie :
- S_{COD} : signal d'horloge de fréquence 21khz modulé en amplitude.

La fonction est réalisée grâce à un astable commandé à portes logiques.

FS 6.3 : Emission infra-rouge:

Entrée :
- signal d'horloge modulé issu de FS 6.2.

Sortie :
- IR_{EM} : signal infrarouge émis par l'émetteur .

La diode émettrice est logée dans le pare chocs du robot de même que le récepteur.

FS 6.4 : Réception infra-rouge:

Entrée :
- IR_{RM} : signal infra-rouge réfléchi par le mur et reçu par le photo-transistor.

Sortie :
- S_{IRM} : signal analogique représentatif du signal infra-rouge reçu par le photo transistor

FS 6.5 : Filtrage:

Entrée :
- signal issu de FS 6.4.

Sortie :
- V_{IRM} : tension filtrée débarrassée des perturbations liées au milieu extérieur (lumière), image du signal reçu.

Un filtre accordé à 21Khz permet de conserver la composante utile du signal.

FS 6.6 : Amplification sélective:

Entrée :
- signal issu de FS 6.5.

Sortie :
- V_{AMP} : tension amplifiée ($A_V = 500$) et filtrée.

Une double amplification est utilisée séparée par un étage de filtrage.

FS 6.7 : Détection crête :

Entrée :
- signal issu de FS 6.6.

Sortie :
- V_{CRET} : tension enveloppe du signal (signal démodulé).

FS 6.8 : Mise en forme :

Entrée :
- signal issu de FS 6.7.

Sortie :
- V_{FORM} : signal d'horloge représentatif de l'onde réfléchie et démodulée.

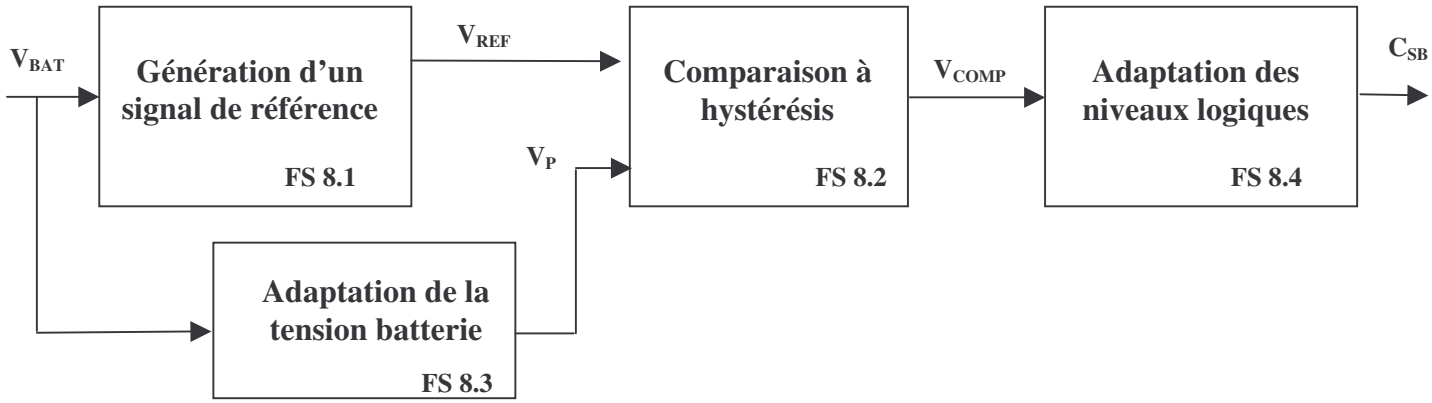
FS 6.9 : Détection de fréquence :

Entrée :
- signal issu de FS 6.8.

Sortie :
- D_M : signal binaire qui informe FP9 de la détection d'un mur.

Un circuit spécialisé de type NE 567 réalise la détection de la fréquence de 210Hz.

d) Schéma fonctionnel de degré 2 de FP 8 « Surveillance batterie »



Définition des fonctions secondaires de FP 8 :

La batterie du robot a une autonomie d'environ 1h35' en mode Max et de 45' en mode Clean. (essai réalisé sur sol type carrelage).
Lorsque Roomba retourne à son socle de chargement, la tension de la batterie est voisine de 14.4 V alors qu'elle est de 17.1 V lorsqu'elle est complètement chargée.
(Tension batterie avec robot sur socle de chargement V_{BAT} = 19.8V).

FS 8.1 : Génération d'un signal de référence :

Entrée :
- V_{BAT} : tension continue de la batterie 14.4V < V_{BAT} < 19.8 V.

Sortie :
- V_{REF} : tension continue de référence pour le comparateur à hystérésis.

La surveillance nécessite l'élaboration d'un signal de référence qui fixera les seuils haut et bas du comparateur à hystérésis de la fonction FS 8.2.

FS 8.2 : Comparaison à hystérésis :

Entrée :

- V_{REF} : tension de référence issue de FS 8.1.
- V_P : tension continue réglable proportionnelle à l'état de charge de la batterie APS.

Sortie :
- V_{COMP} : Signal logique représentatif de l'état de la batterie (déchargée ou chargée).

FS 8.3 : Adaptation de la tension batterie :

Entrée :

- V_{BAT} : tension continue de la batterie

Sortie :

- V_P : tension continue réglable proportionnelle à l'état de charge de la batterie APS.

FS 8.4 : Adaptation des niveaux logiques :

Entrée :

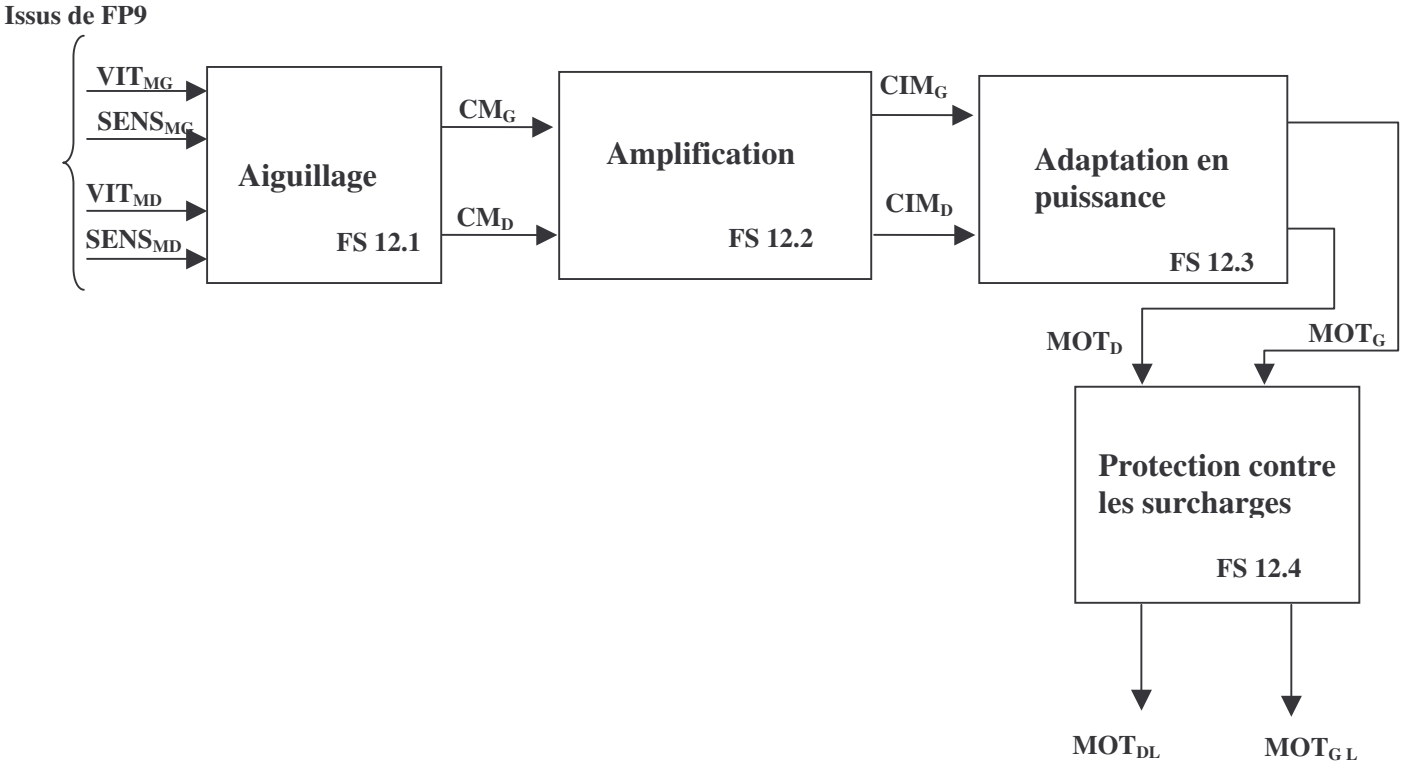
- V_{COMP} : Signal logique issu de FS 8.2.

Sortie :

- C_{SB} : Signal logique ; information binaire compatible TTL, qui prévient le microcontrôleur de l'état de charge de la batterie (batterie déchargée ou batterie opérationnelle).

e) Schéma fonctionnel de degré 2 de FP 12 « Interface roues motrices »

La commande d'entraînement des roues droite et gauche, est contrôlée par le 68HC711. On utilisera la technique de la modulation de largeur d'impulsion pour diriger le mobile. En effet, il faudra veiller à commander les 2 roues de manière indépendante, car le robot se déplace souvent avec une trajectoire en arc de cercle. Il peut même reculer.



Définition des fonctions secondaires de FP 12 :

FS 12.1 : Aiguillage :

Entrée :

- VIT_{MG}, VIT_{MD}, $SENS_{MG}$, $SENS_{MG}$: 4 signaux logiques issus du microcontrôleur permettant au robot de parcourir une trajectoire, parmi lesquels 2 signaux logiques dictant le sens d'entraînement des roues motrices et 2 signaux modulés en largeur d'impulsion (MLI) contrôlant la vitesse de rotation de chacune des roues.

Sortie :

- CM_G, CM_D : 2 informations logiques ; signaux binaires représentatifs de la trajectoire à effectuer.

Les signaux qui contrôlent la vitesse du moteur sont modulés en largeur d'impulsion. Pour chaque moteur le signal VIT est dirigé par un aiguillage lui même activé par l'entrée logique correspondant au sens de rotation.

FS 12.2 : Amplification :

Entrée :

- signaux logiques issus de FS 12.1.

Sortie :

- CIM_G, CIM_D : 2 informations logiques; signaux binaires mais cette fois-ci amplifiés en courant image de la trajectoire à effectuer.

FS 12.3 : Adaptation en puissance :

Entrée :

- signaux logiques issus de FS 12.2.

Sortie :

- MOT_G, MOT_D : puissances délivrées au moteur droit et gauche ;

On utilise ici un pont en H traditionnel en technologie bipolaire. La puissance dissipée par les transistors devra rester faible.

FS 12.4 Protection contre les surcharges :

Entrée :

- MOT_G, MOT_D : puissances délivrées au moteur droit et gauche.

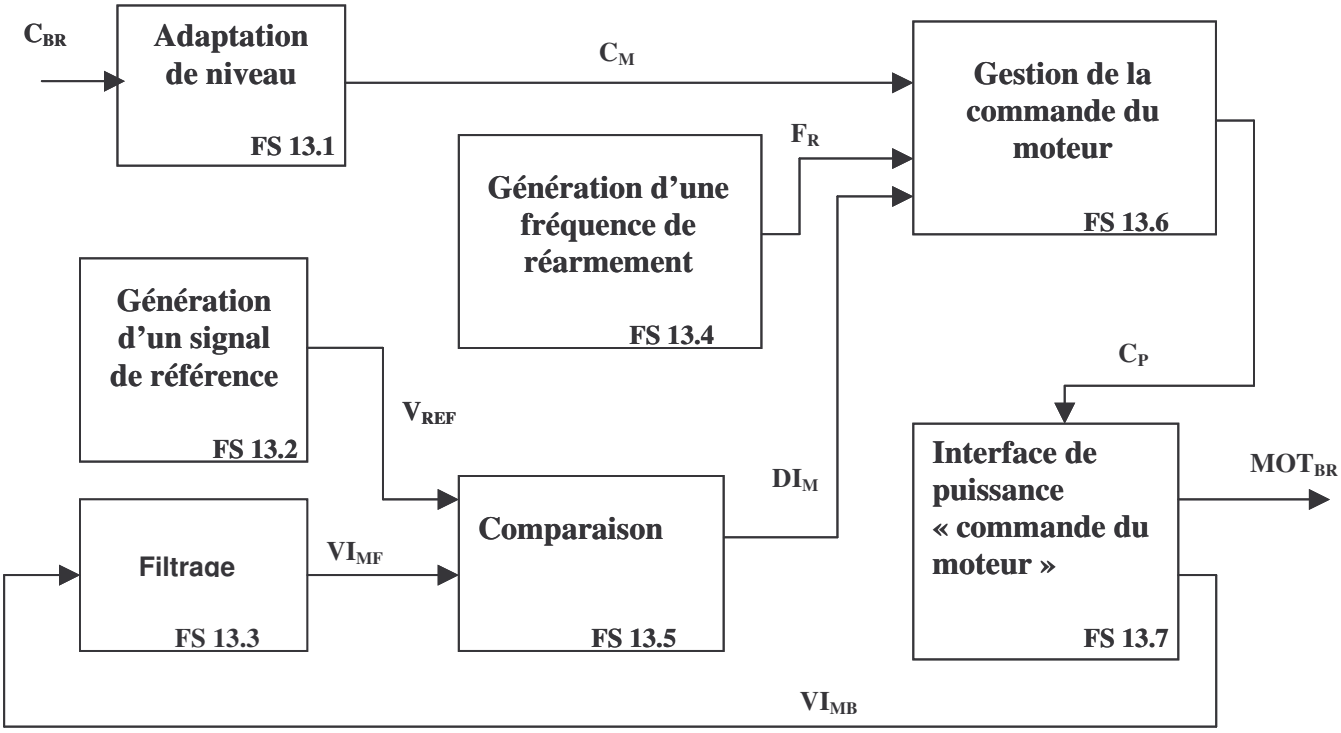
Sortie :

- MOT_{GL}, MOT_{DL} : puissances limitées délivrées au moteur droit et gauche.
  (limitation en courant dans chaque branche du pont contre d'éventuels court-circuits)

f) Schéma fonctionnel de degré 2 de FP 13 « Interface brosse »

La commande de la brosse est également contrôlée par le 68HC711. La structure mise en œuvre utilise un moteur à courant continu et un système de réduction afin de diminuer la vitesse de rotation tout en gardant un couple de rotation important.
Le moteur de la brosse est situé au centre du robot devant le compartiment ramasse poussière.

La commande brosse est équipée d'un système de protection en cas de blocage de la brosse par des éléments tels que fils électriques, ficelles, plastiques, etc… , on limitera le courant au environ d'un ampère.



Définition des fonctions secondaires de FP 13 :

FS 13.1 : Adaptation de niveau :

Entrée :
- C_{BR} : signal binaire compatible TTL issue de FP9 .

Sortie :
- C_M : signal binaire 0 –12V : commande du moteur.

FS 13.2 : Génération d'un signal de référence :

Entrée :
- aucune

Sortie :
- V_{REF} : information analogique ; tension continue réglable. Règle la valeur du courant maximal à ne pas dépasser dans le moteur.

FS 13.3 : Filtrage :

Entrée :
- VI_{MB} : tension analogique image du courant moteur .

Sortie :
- VI_{MF} : tension analogique image du courant moteur sans perturbation.

FS 13.4 : Génération d'une fréquence de réarmement :

Lors d'un dépassement de courant dans le moteur, on coupe le transistor de puissance de FS13.7 . Celui-ci sera réarmé à une fréquence de 20kHz.

Entrée :
- aucune

Sortie :
- F_R : signal périodique 0-12V de fréquence 20kHz et de rapport cyclique 8% environ .

FS 13.5 : Comparaison :

Entrée :
- signaux analogiques issus de FS 13.2 et de FS 13.3

Sortie :
- DI_M: signal binaire, détection d'une surintensité dans le moteur.

FS 13.6 : Gestion de la commande du moteur :

Entrée :
- $C_{M,}$ F_R et DI_M signaux binaires issus de FS13.1, FS 13.4 et de FS 13.5

Sortie :
- C_P : signal binaire, commande le transistor de puissance.

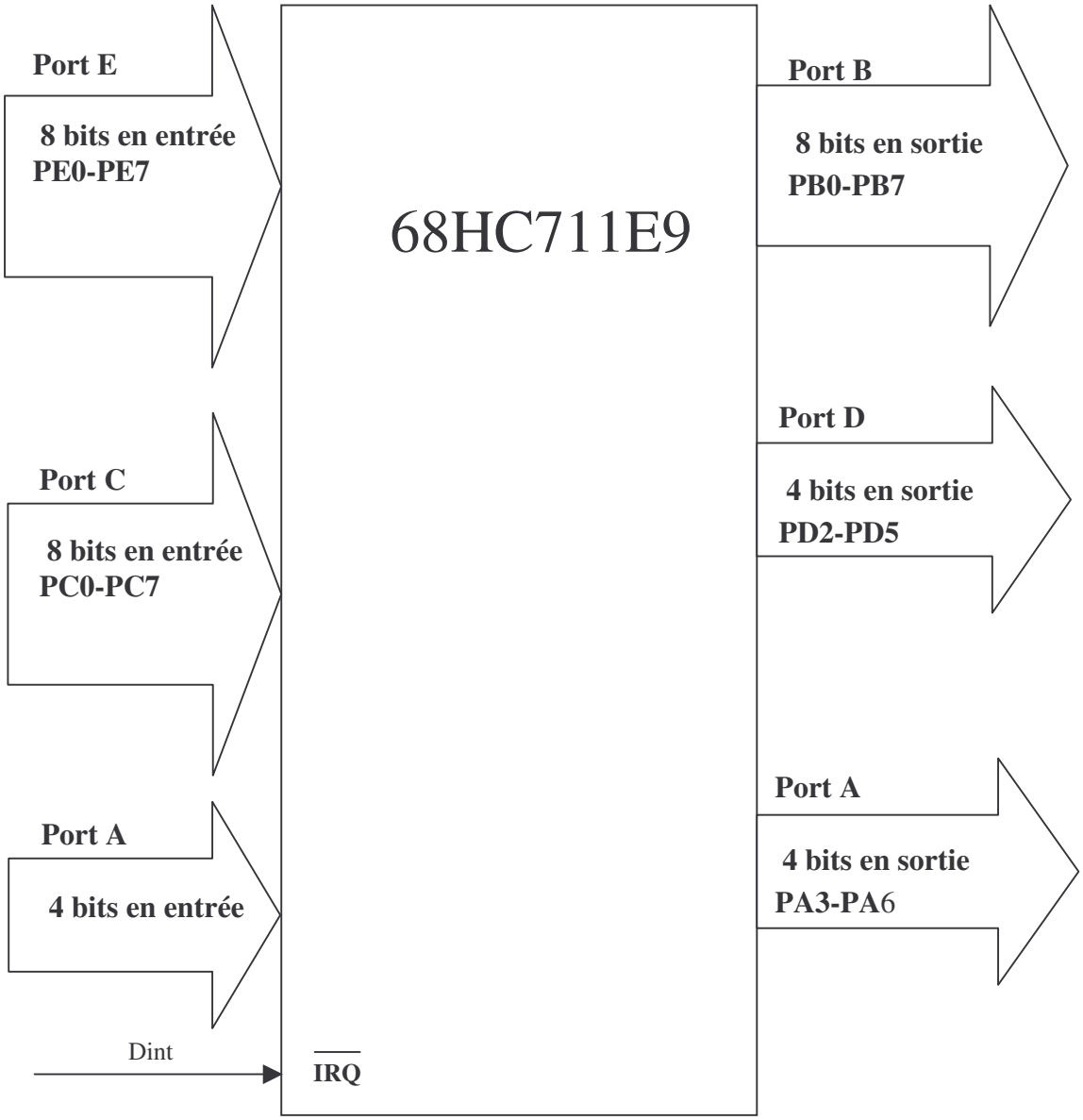
FS 13.7 : Interface de puissance :

Entrée :
- C_P : signal binaire issu de FS13.6 active le transistor de puissance.

Sortie :
- $MOT_{BR,}$: alimentation du moteur brosse
- VI_{MB} : tension analogique image du courant moteur.

Note : Résistance de l'enroulement moteur $R_M = 10\Omega$.

4. Affectation des ports du 68HC711E9



ENTREES

Port C : 8 bits en entrée

- FP2 : Détection : (Télécommande) : D_{T1} à D_{T4} — 4 bits P_{C0} à P_{C3}
- FP2 : Détection : (Unité de cloisonnement): D_{UC} — 1 bit P_{C4}
- FP3 : Détection de niveau : D_{NG} et D_{ND} — 2 bits P_{C5}- P_{C6}
- FP4 : Détection de particules : D_{P1} — 1 bit P_{C7}

Port E : 8 bits en entrée

- FP2 : Détection : (Socle de rechargement) : D_{SC} 1 bit P_{E0}
- FP5 : Détection d'obstacle : D_{OBG} et D_{OBD} 2 bits P_{E1}- P_{E2}
- FP6 : Détection mur : D_M 1 bit P_{E3}
- FP10: Acquisition des données de l'opérateur :
  A_C, A_S, A_M, M_A 4 bits P_{E4}- P_{E7}

Port A : 4 bits en entrée

- FP7 : Détection vitesse roue motrices : D_{VRD}, D_{VRG} 2 bits P_{A0}- P_{A1}
- FP1 : Détection de soulèvement : D_{S1} 1 bit P_{A2}
- FP8 : Surveillance batterie : C_{SB} 1 bit P_{A7}

IRQ : 1 bit en entrée

- FP2 : Détection : (Télécommande) : D_{INT}

SORTIES

Port B : 8 bits en sortie

- FP12 : Commande d'entraînement roues motrices :
  $SENS_{MD}$, $SENS_{MG}$ 2 bits P_{B1}- P_{B3}
- FP13 : Commande brosse : C_{BR} 1 bit P_{B4}
- FP14 : Commande balai : C_{BL} 1 bit P_{B5}
- FP15 : Commande aspiration : C_{AS} 1 bit P_{B6}
- FP11 : Affichage voyants : A_{FF1} (voyant max) 1 bit P_{B7}
  Affichage LCD des informations :
  DIN_{LCD}, CLK_{LCD} 2 bits P_{B0}- P_{B2}

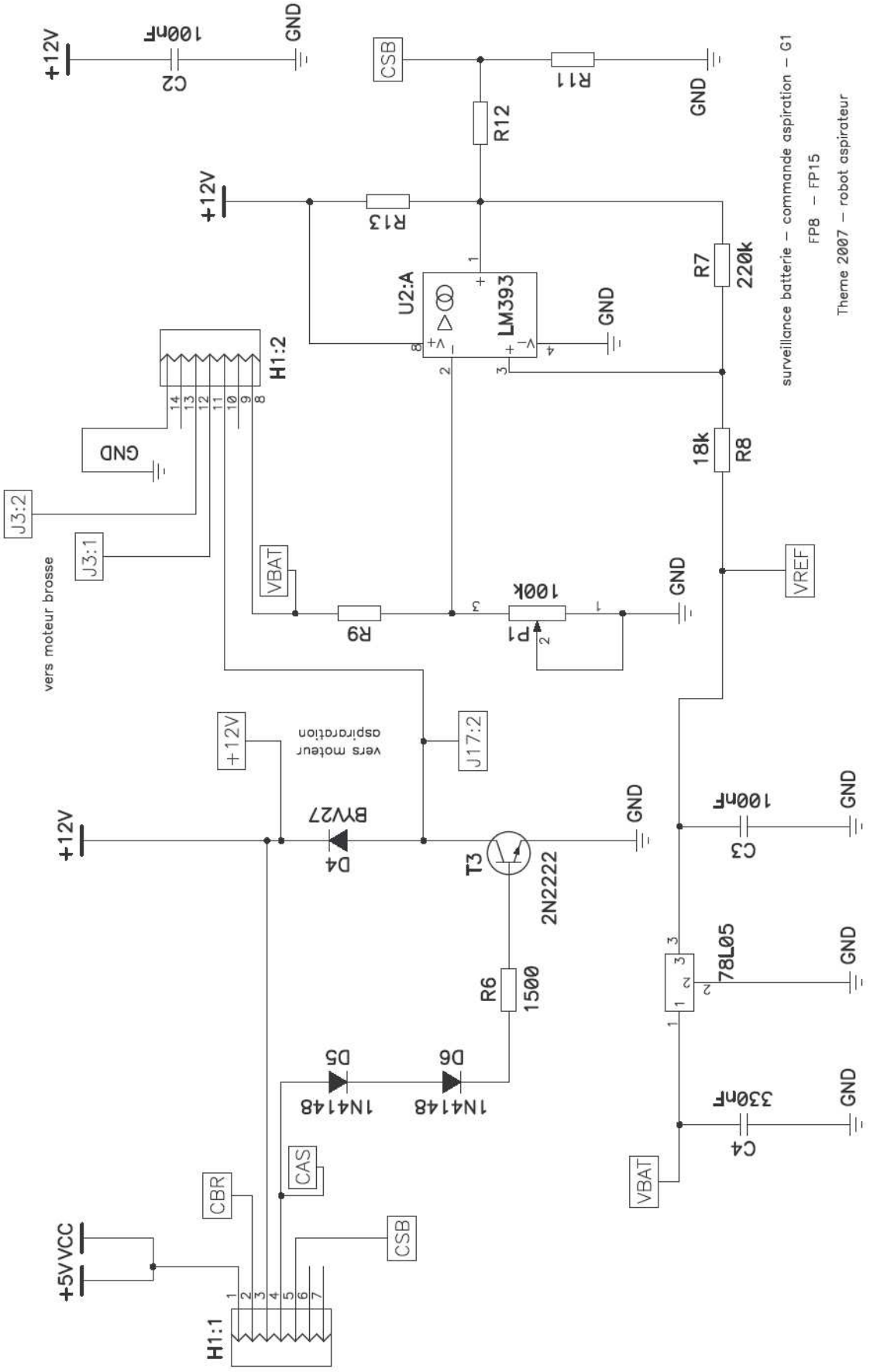
Port A : 4 bits en sortie

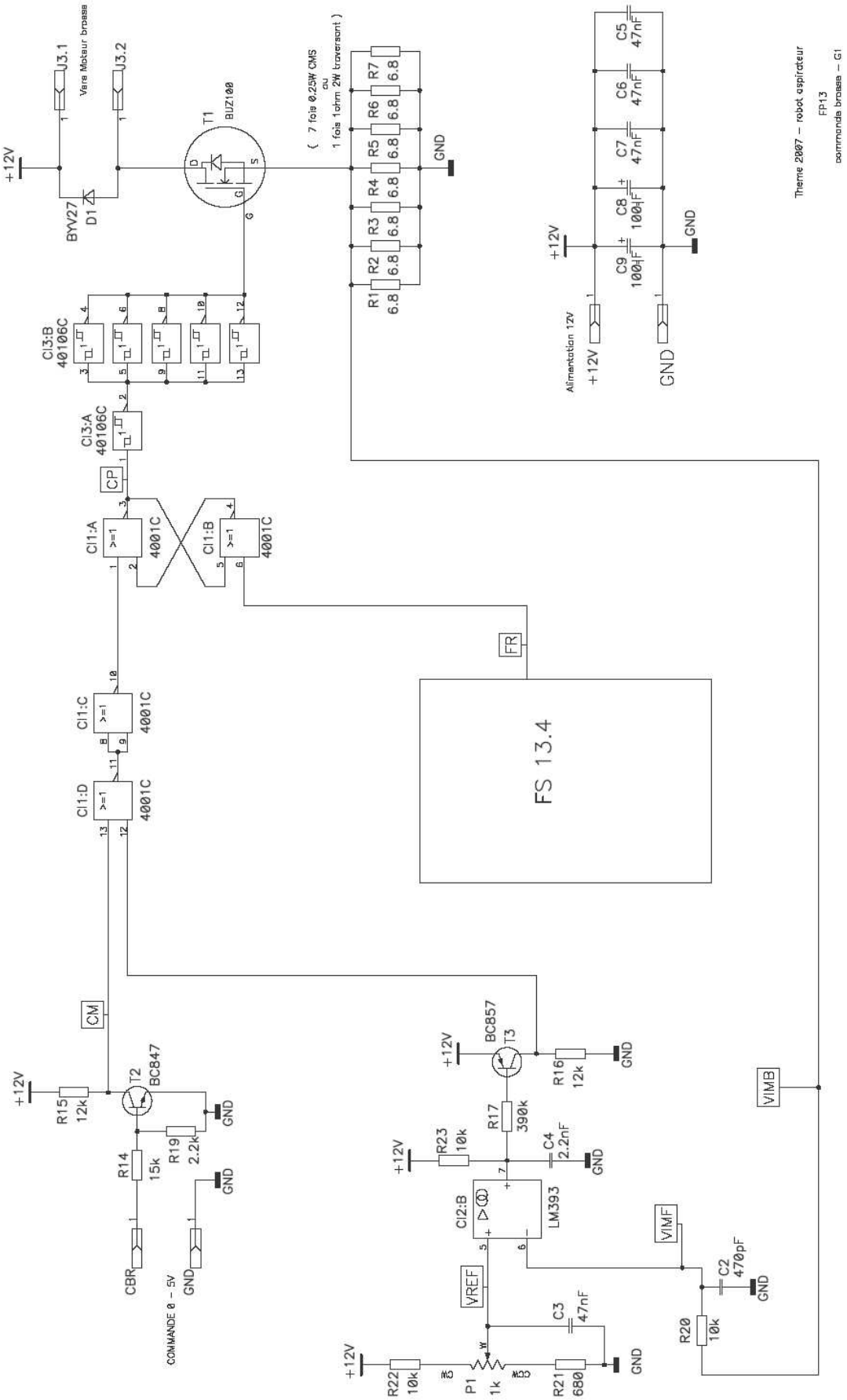
- FP11 : Affichage LCD des informations :
  SCE_{LCD} , DC_{LCD} 2 bits P_{A3}- P_{A4}
- FP12 : Commande d'entraînement roues motrices :
  VIT_{MG}, VIT_{MD} 2 bits P_{A5}- P_{A3}

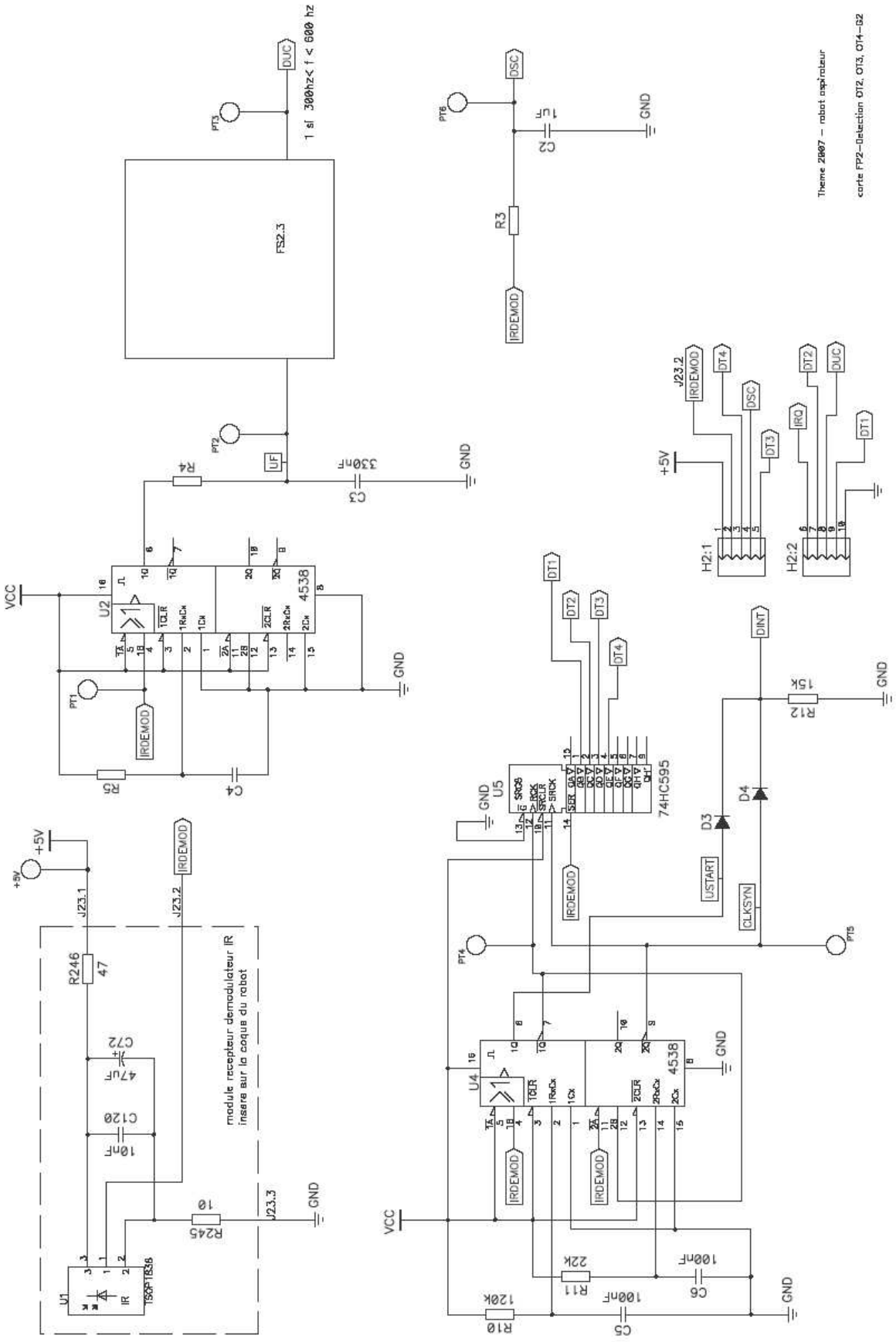
Port D : 4 bits en sortie

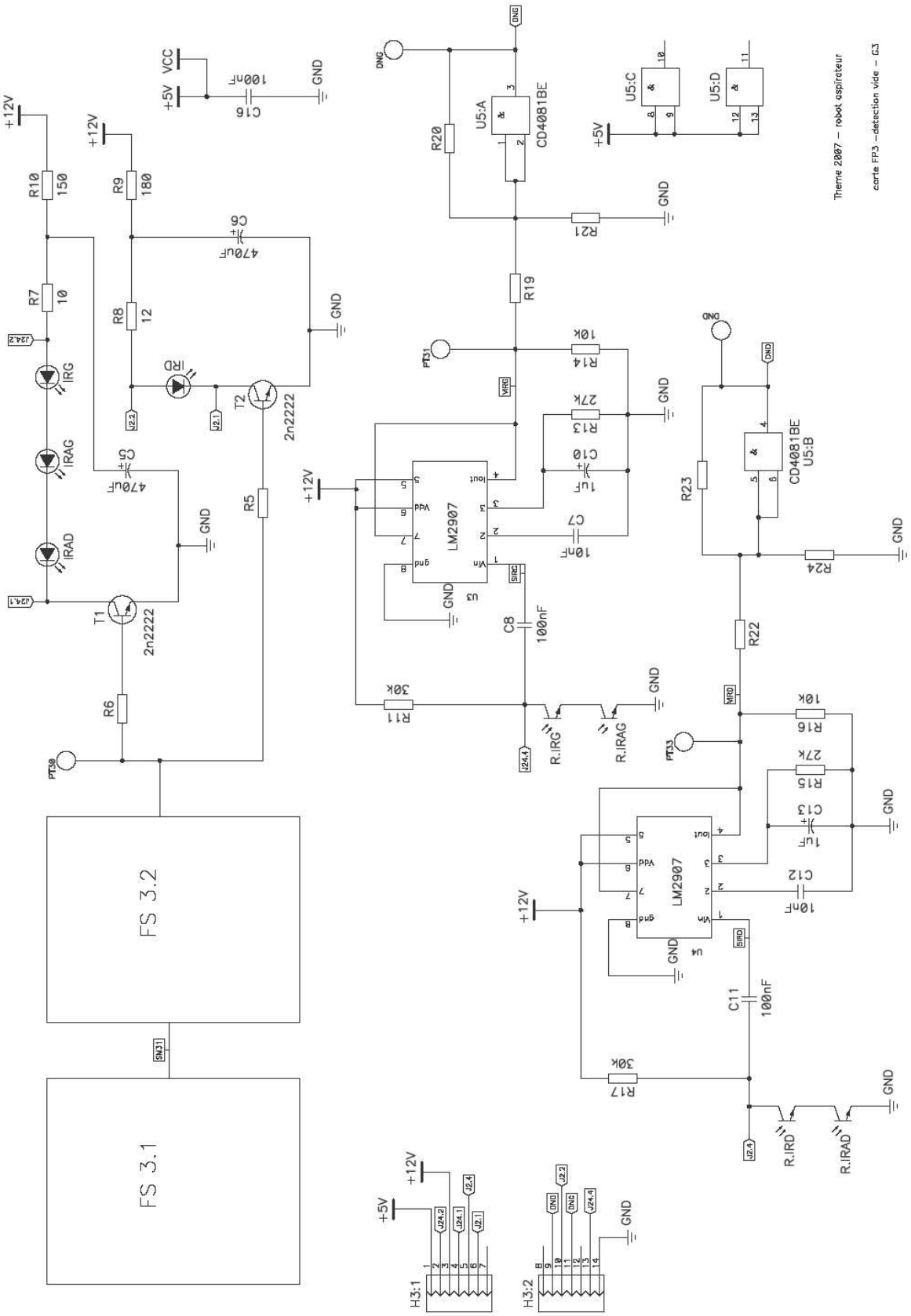
- FP11 : Génération d'un signal sonore : B_{UZ} 1 bit P_{D2}
- FP11 : Affichage voyants : A_{FF2} , A_{FF3}, A_{FF4} 3 bits P_{D3}- P_{D5}
  (voyant clean, voyant power, voyant spot)

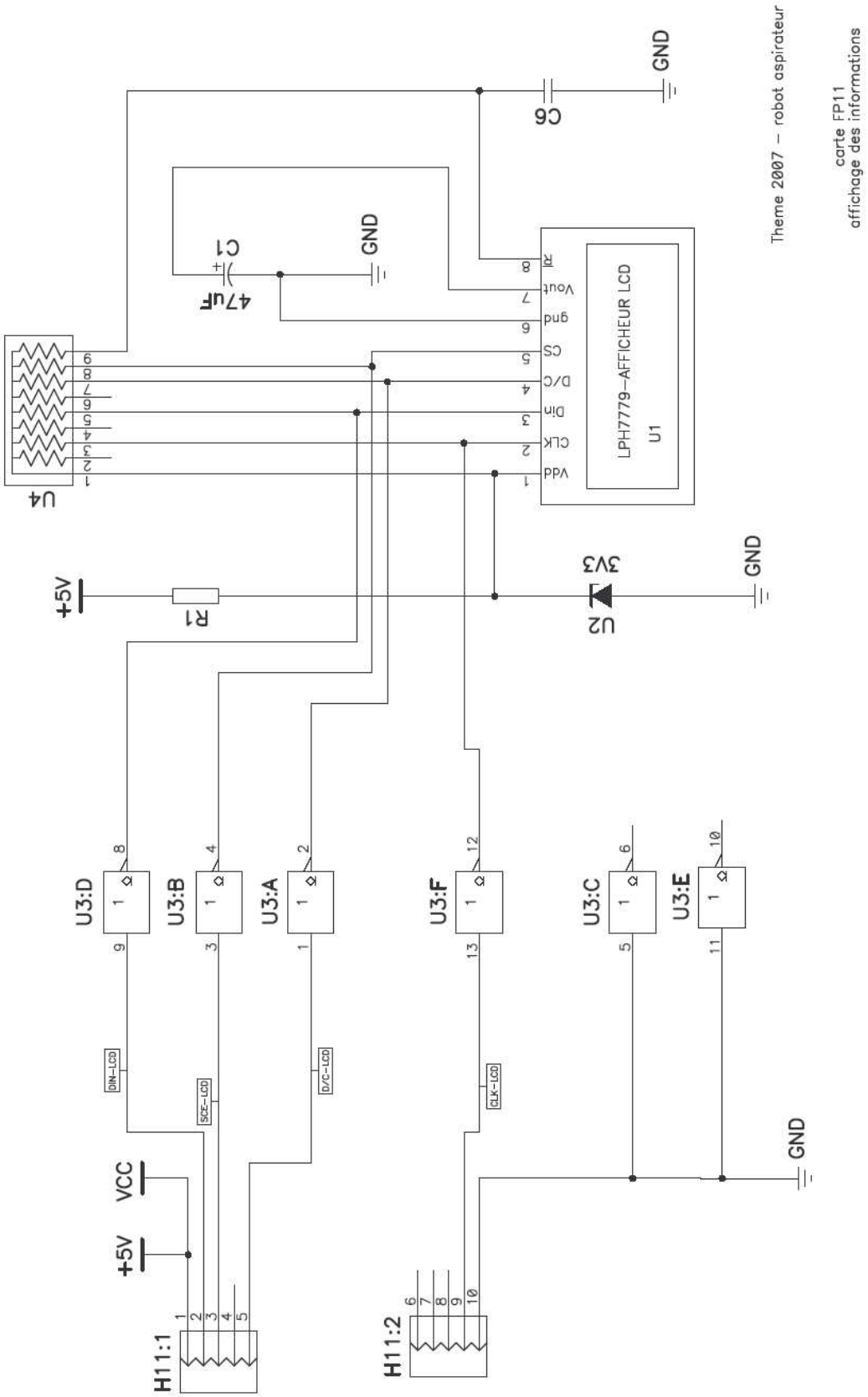
4. Schémas structurels

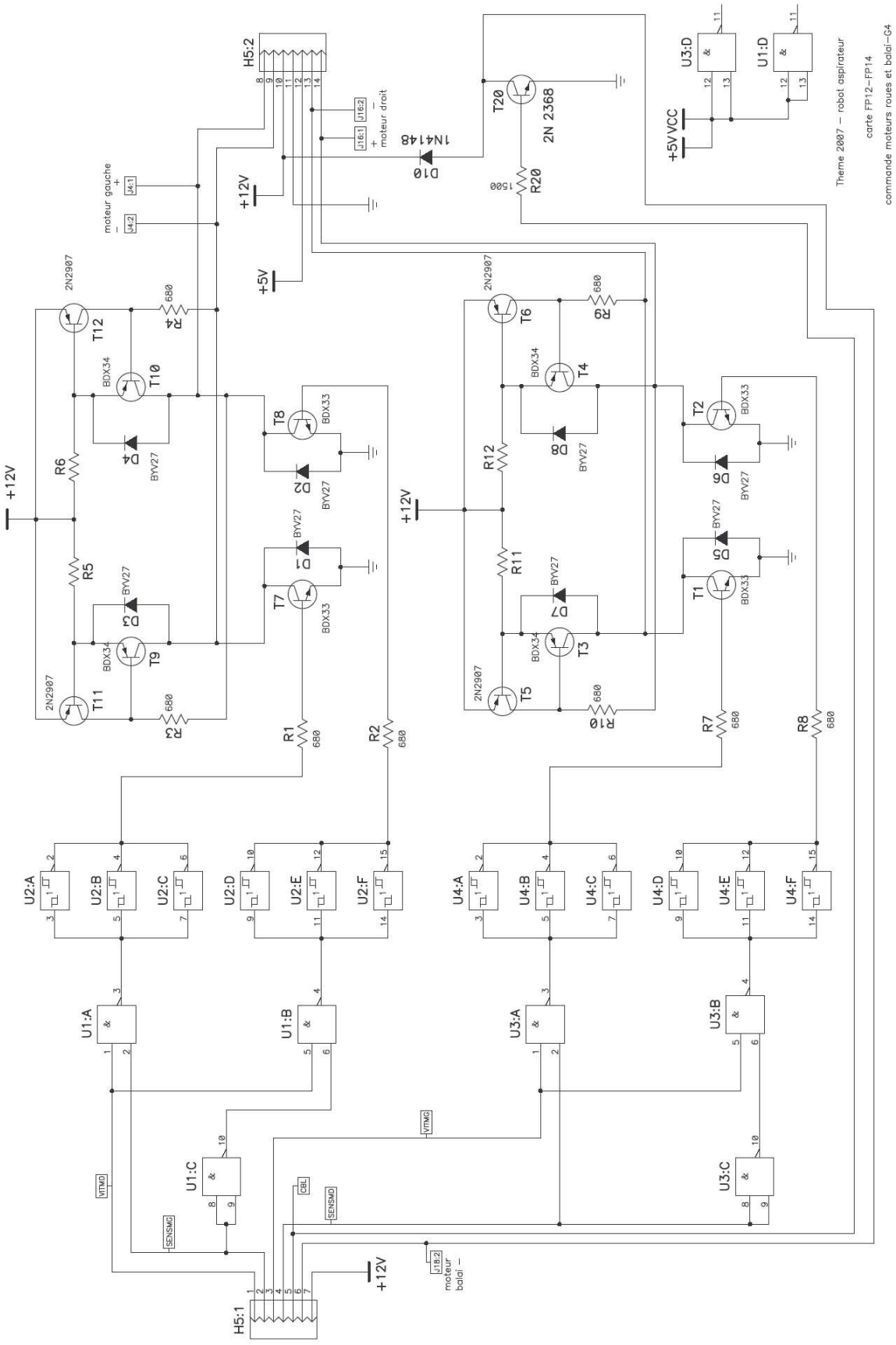


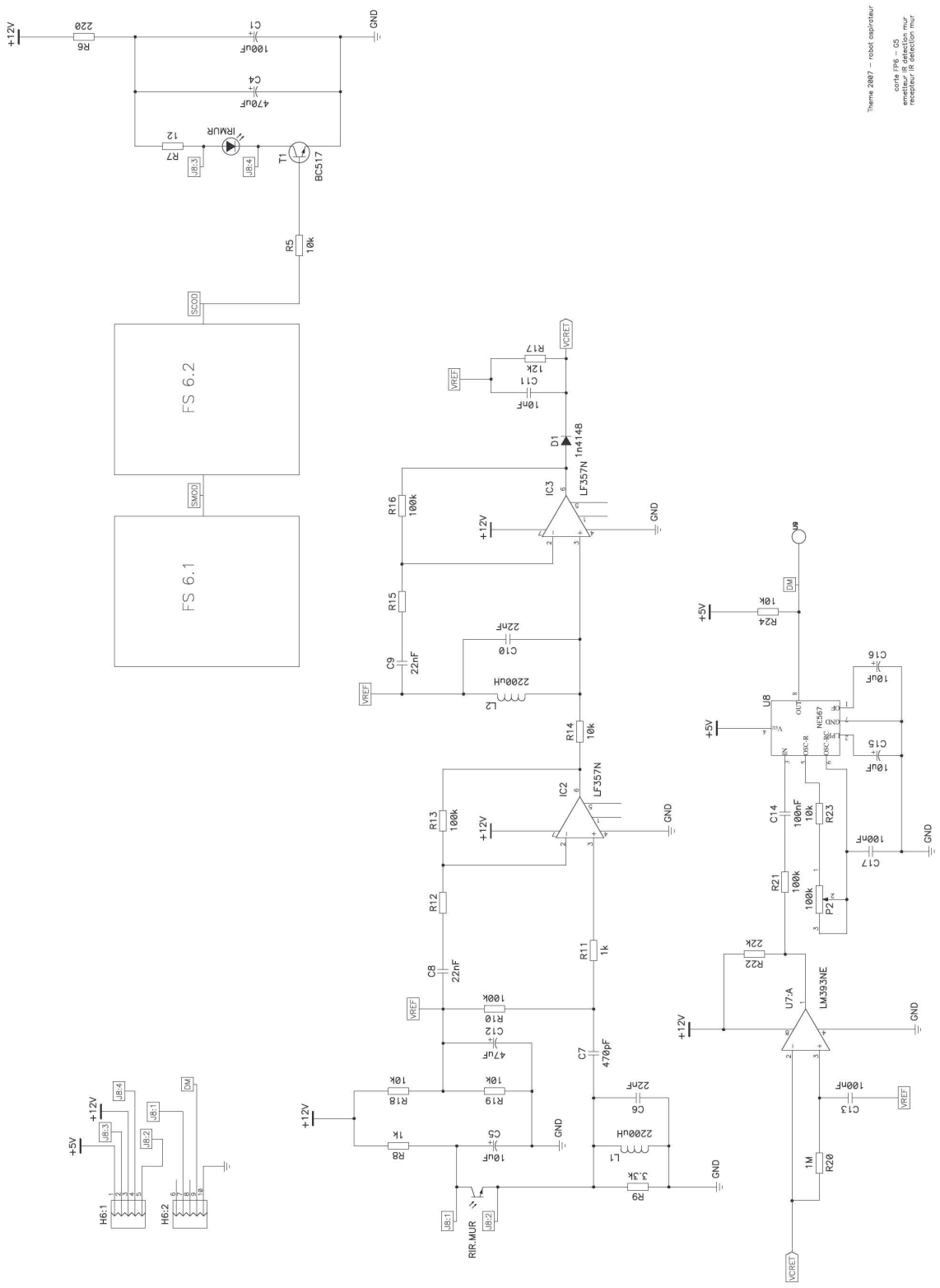

Vers Moteur brosse
U3.1
U3.2
T1
BUZ100
BYV27
D1
+12V
GND
(7 fois 0,25W CMS
ou
1 fois 1ohm 2W traversant)
R1 6.8
R2 6.8
R3 6.8
R4 6.8
R5 6.8
R6 6.8
R7 6.8
C5 47nF
C6 47nF
C7 47nF
C8 100µF
C9 100µF
Alimentation 12V
Thème 2007 – robot aspirateur
FP13
commande brosse – G1
Cl3:B 40106C
Cl3:A 40106C
CP
Cl1:A 4001C
Cl1:B 4001C
Cl1:C 4001C
Cl1:D 4001C
FR
FS 13.4
CM
T2 BC847
R15 12k
R14 15k
R19 2.2k
CBR
COMMANDE 0 - 5V
T3 BC857
R16 12k
R17 390k
R23 10k
C4 2.2nF
Cl2:B LM393
VREF
C3 47nF
R22 10k
P1 1k
R21 680
VIMF
C2 470pF
R20 10k
VIMB


Theme 2007 – robot aspirateur
carte FP2–detection DT2, DT3, DT4–B2
1 si 300hz< f < 600 hz
FS2.3
DUC
PT3
PT6
DSC
C2
1uF
GND
R3
IRDEMOD
J23.2
DT4
DSC
DT3
DT2
DUC
IRQ
DT1
+5V
H2:1
H2:2
PT2
UF
330nF
C3
R4
VCC
U2
4538
PT1
R5
C4
DT1
DT2
DT3
DT4
DINT
R12
15K
U5
74HC595
D3
D4
USTART
CLKSYN
PT4
PT5
J23.1
J23.2
R246
47
C72
47uF
C120
10nF
module recepteur demodulateur IR
insere sur la coque du robot
R245
10
J23.3
U1
TSOP1838
U4
22K
R11
100nF
C6
C5
120K
R10


Thème 2007 – robot aspirateur
carte FP3 –détection vide – G3
FS 3.2
FS 3.1
LM2907
CD4081BE
2n2222
IRG
IRAG
IRAD
IRD
R.IRG
R.IRAG
R.IRD
R.IRAD
+12V
+5V
GND
VCC


Theme 2007 – robot aspirateur
carte FP11
affichage des informations
GND
C6
C1
47uF
LPH7779–AFFICHEUR LCD
U1
Vout
gnd
CS
D/C
Din
CLK
Vdd
U4
+5V
R1
3V3
U2
U3:D
U3:B
U3:A
U3:F
U3:C
U3:E
DIN-LCD
SCE-LCD
D/C-LCD
CLK-LCD
VCC
H11:1
H11:2


Theme 2007 – robot aspirateur
carte FP12–FP14
commande moteurs roues et balai–G4
+12V
+5V
+5V VCC
moteur gauche
moteur droit
moteur balai
1N4148
2N 2368
BDX34
BDX33
BYV27
2N2907
VITMD
VITMG
SENSMD
SENSMG
CBL


Theme 2007 -- robot aspirateur
carte FP6 -- G5
emetteur IR detection mur
recepteur IR detection mur
+12V
R6 220
C1 100uF
C4 470uF
R7 12
IRMUR
J8:3
J8:4
T1 BC517
R5 10k
SCOD
FS 6.2
SMOD
FS 6.1
VCRET
R17 12k
VREF
C11 10nF
D1 1n4148
IC3 LF357N
R16 100k
R15
C9 22nF
C10 22nF
L2 2200uH
R14 10k
IC2 LF357N
R13 100k
R12
C8 22nF
R11 1k
R10 100k
C12 47uF
C7 470pF
R18 10k
R19 10k
C6 22nF
R8 1k
C5 10uF
L1 2200uH
R9 3.3k
GND
J8:1
J8:2
RIR.MUR
+5V
DM
R24 10k
U8
NE567
C16 10uF
C15 10uF
C14 100nF
R23 10k
C17 100nF
R21 100k
P2 100k
R22 22k
U7:A LM393NE
C13 100nF
R20 1M
H6:1
H6:2

6 -Travail demandé

L'étude du système est répartie entre 5 groupes de travail (binôme). Ces 5 groupes auront à réaliser au total 6 cartes électroniques. Toutes les cartes auront un connecteur HE10 (dont le brochage est imposé) relié à la carte fond de panier, sur laquelle sera insérée la carte microcontrôleur.

Tous les capteurs et les moteurs utilisés sont ceux déjà implantés dans le robot. Pour tester les cartes réalisées, vous pourrez soit les connecter directement au robot, soit utiliser un (ou des) capteur(s) extérieur(s) supplémentaire(s). L'ensemble sera implanté sur le dessus du robot.

Constitution des groupes de travail :

Groupe 1 :

FP13 « Commande brosse »
FP15 « Commande aspiration »
FP 8 « Surveillance batterie »

Les 3 fonctions seront regroupées sur une seule carte électronique reliée par le connecteur H1.

Groupe 2 :

FP2 « Détection unité de cloisonnement-Socle de chargement-Télécommande »

La fonction sera réalisée seule sur une seule carte électronique reliée par le connecteur H2.

Groupe 3 :

FP3 « Détection de niveau »
FP11 « Affichage des informations, génération d'un signal sonore »

Chaque fonction sera réalisée seule. Il y aura donc deux cartes électroniques à fabriquer. FP3 reliée par le connecteur H3 et FP11 reliée par le connecteur H11.

Groupe 4 :

FP12 « Commande des roues motrices »
FP14 « Commande balai »

Les 2 fonctions seront regroupées sur une seule carte électronique reliée par le connecteur H5.

Groupe 5 :

FP6 « Détection mur »

La fonction sera réalisée seule sur une seule carte électronique reliée par le connecteur H6.

Remarque importante relative à tous les groupes

Les questions posées ne sont pas exhaustives. Elles sont un guide pour vous aider dans la compréhension de votre système et la rédaction de votre dossier.
Ce dernier ne devra donc pas se présenter comme une suite chronologique de réponses à ces questions.

Travail commun à tous les groupes

- Connaissance fonctionnelle jusqu'au 1er degré du système
- Etude qualitative de vos fonctions
- Etude quantitative de vos fonctions
- Réalisation des maquettes
- Validation expérimentale : Test et relevés "commentés" de mesures
- (oscillogrammes etc. …..)
- Montage de l'ensemble sur le robot permettant un contrôle aisé par le jury.
- Rédaction d'un rapport comprenant les parties précédentes (voir annexe).
- Préparer un exposé oral en tenant compte de la grille d'évaluation qui vous sera présentée.
  Conseil : La présentation fonctionnelle jusqu'au 1er degré ne doit pas excéder 5mn pour l'épreuve orale.

Etude fonctionnelle:
Entourer les fonctions secondaires sur le structurel et identifier les signaux reliant ces fonctions.
Transcrire l'analyse fonctionnelle de second degré en chronogrammes décrivant le fonctionnement des fonctions principales étudiées.

Réalisation et essais :

Réaliser le(s) typon(s), fabriquer la carte et procéder aux réglages.
Faire un ou plusieurs relevés expérimentaux (**oscillogrammes**) permettant de valider le fonctionnement.

Travail groupe 1 :

Etude structurelle:

Pour FP8

Expliciter le fonctionnement de U2 :A lorsque :
- la batterie se décharge de 17V à 13V,
- la batterie se recharge de 13V à 19V,

Tracer les chronogrammes de fonctionnement correspondant de Vbat, et V en sortie de U2 :A
Tracer la caractéristique V_{CSB} en fonction de Vbat.

Dimensionner R9.
Calculer les seuils de basculement de U2 :A
Dimensionner R11 et R12.

Pour FP15

Expliciter le fonctionnement du transistor.
Quel est le rôle des différentes diodes ?

Mesurer le courant consommé par le moteur et justifier le choix du transistor. Vérifier que le transistor est bien saturé (calculer le coefficient de sursaturation éventuellement).

Pour FP13

Pour la position médiane de P1, calculer le seuil de basculement du comparateur. En déduire la valeur du courant I_M .

Donner l'état de DI_M lors d'une surintensité.

Tracer les chronogrammes théoriques de fonctionnement de FS 13.6 en faisant apparaître 3 zones (pas de commande, fonctionnement normal, surintensité).

En alimentant le moteur sous 12V, mesurer le courant consommé par celui-ci en fonctionnement normal, puis lorsqu'il est à limite du blocage. (Attention de réaliser la mesure rapidement). Proposer une valeur de réglage de Imaxi.

Proposer une structure réalisant FS13.4 à base d'un LM393.

Programmation

Réaliser un programme gérant FP13, FP15, FP8 et commandant l'allumage du voyant Power à la mise en marche du robot.

Travail groupe 2 :

Etude préliminaire :

Relever les chronogrammes du signal IR_{DEMOD} reçu de chacun des objets OT2, OT3, OT4 (pour chaque touche).

Donner le code correspondant à chacune des touches de la télécommande.

Etude structurelle:

Expliciter le fonctionnement du montage réalisé autour de U2.

Quel nom pourrait-on donner à l'ensemble D1, D2, R9 ?

Expliquer le fonctionnement du montage réalisé autour de U4 et U5.
Tracer les chronogrammes de fonctionnement correspondant.

Quel nom pourrait-on donner à l'ensemble D3, D4, R12 ?

On désire obtenir une tension de 2,5V en Uf (PT2), lorsque le signal IR reçu est émis par OT2, dimensionner R4, R5 et C4.

Proposer une structure réalisant FS2.3.

Justifier la valeur de R10, C5 et R11, C6.

Dimensionner R3.

Programmation

Réaliser un programme de test (avec ou sans interruption) permettant la validation de la carte.

Travail groupe 3 :

Etude structurelle:

Proposer une structure réalisant FS 3.1 et FS 3.2 à base de circuit NE556.
Tracer les chronogrammes de fonctionnement correspondant.

Expliquer le fonctionnement de la structure réalisée autour de U5:A.

Tracer l'allure de la caractéristique D_{NG} en fonction de la tension en sortie de U3 (PT31).
Expliquer le fonctionnement de U3 et U4.

Expliquer le fonctionnement du module afficheur LPH7779.

Dimensionner les composants réalisant FS 3.1 et FS 3.2.

Dimensionner R6, R5.

Calculer et tracer la caractéristique de transfert de U3 et U4.

Mesurer le seuil de basculement de U5:A (seul)
Exprimer les seuils de basculement de la structure réalisée autour de U5:A.

Dimensionner R20, R19, et R21

Programmation

Réaliser un programme permettant l'acquisition des signaux issus de FP3.

Réaliser le programme permettant d'afficher : 

Travail groupe 4 :

Etude structurelle:

Etablir la table de vérité des sorties de U1:A, U1:B, U3:A, U3:B en fonction de VIT_{MD} , $SENS_{MD}$, VIT_{MG}, $SENS_{MG}$ en précisant l'état des transistors T1, T2, T3, T4, T7, T8, T9, T10 et le déplacement du robot obtenu dans chaque cas.

Quel est le rôle des différentes diodes ?

Expliquer le fonctionnement de la protection contre les surcharges.

Donner l'expression du courant maxi pouvant circuler dans un moteur.

Expliquer pourquoi on a placé trois portes logiques en parallèle.

Expliquer le fonctionnement du transistor T20.

Expliquer le principe qu'il faudra utiliser pour faire varier la vitesse.

Mesurer le courant consommé par les moteurs des roues et justifier le choix des transistors.

Vérifier que le transistor T20 est bien saturé (calculer le coefficient de sursaturation éventuellement).

Dimensionner les résistances R5, R6, R11, R12 pour limiter le courant à 3 A.

Programmation

Réaliser un programme permettant de générer les signaux VIT_{MD} et VIT_{MG} (6 vitesses différentes).

Réaliser un programme permettant de mesurer la vitesse de rotation de chaque roue (signaux issus de FP7).

Travail groupe 5 :

Etude structurelle:

Proposer une structure réalisant FS 6.1 et FS 6.2 à base de portes logiques.
(Prévoir un réglage de la fréquence).

Tracer les chronogrammes de fonctionnement correspondant.

Expliquer le fonctionnement de FS 6.7.

Faire l'étude de l'impédance R9, C6, L1 :

- déterminer la fréquence de résonnance pour la valeur extrème de l'impédance.
- Tracer son impédance en fonction de la fréquence. (par calcul ou simulation).
- Justifier l'intérêt de cette structure.

Déterminer le coefficient d'amplification du premier amplificateur. Dimensionner R12 pour avoir une amplification d'environ 50.

Déterminer le coefficient d'amplification du second amplificateur. Dimensionner R15 pour avoir une amplification d'environ 10.

Etudier la réponse en fréquence de FS 6.9. Déterminer l'expression littérale de sa fréquence centrale et la calculer. Déterminer l'expression littérale de sa largueur de bande et la calculer.
Tracer la caractéristique de FS 6.9.

Programmation

Réaliser un programme permettant l'acquisition des signaux issus de FP1, FP5, FP6 et commandant l'émission d'un bip sonore lors du soulèvement du robot ou lors d'un appui sur une des touches du robot.

Proposition de plan pour votre rapport :

Le rapport devra comporter environ 30 pages hors annexe(s). En annexe, ne pourront figurer que les documents constructeurs indispensables à la compréhension du rapport. Il devra comporter un sommaire et les pages devront être numérotées. Le dossier peut être manuscrit.

Le rapport pourra suivre le plan suivant:

La partie présentation n'apparaît pas dans le dossier mais doit être parfaitement connue pour l'examen.

1. Etude fonctionnelle de 1er degré de l' objet technique.
- Schéma fonctionnel de 1er degré.
- Explications des fonctions principales.
- Définitions des liaisons.

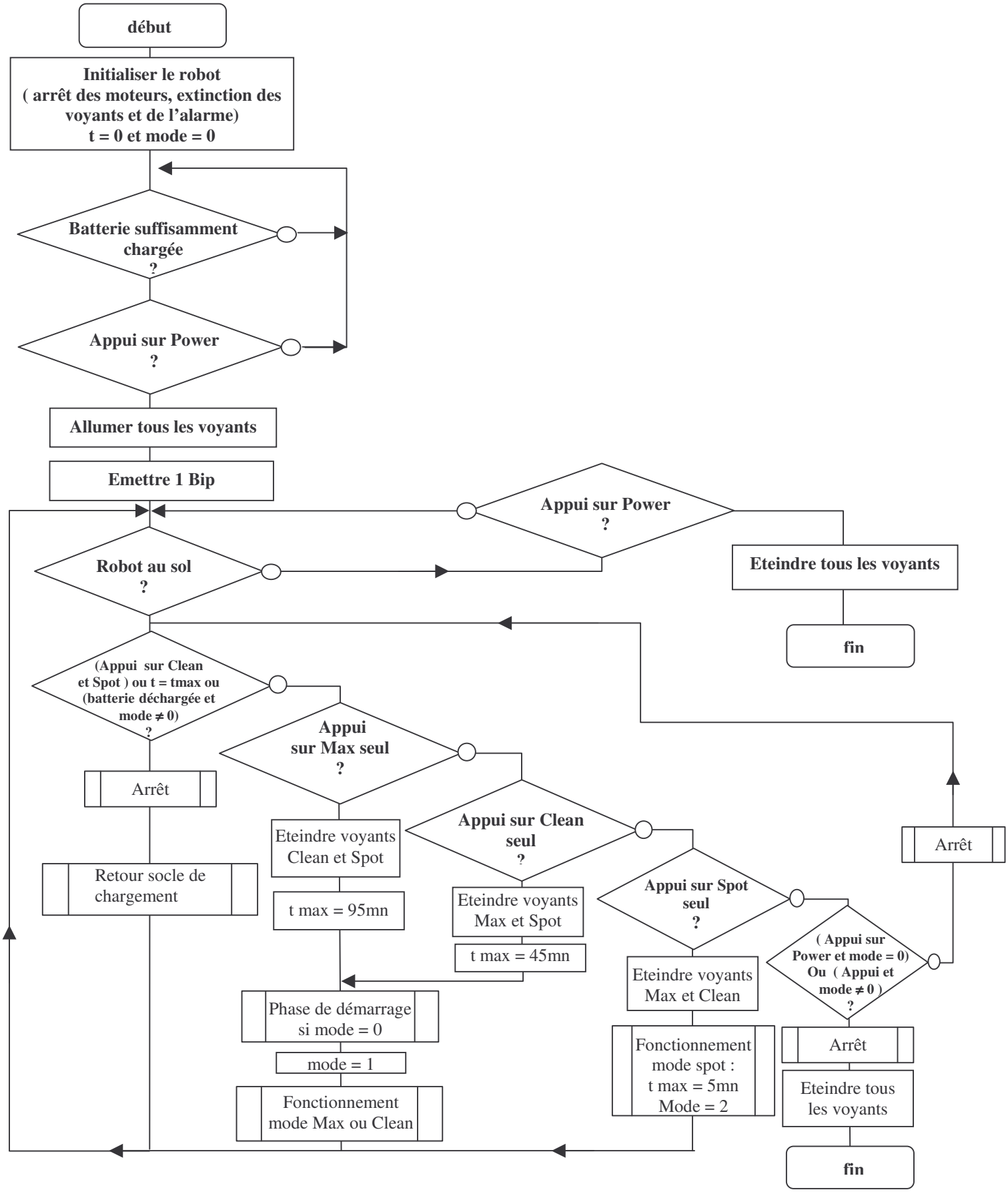
2. Explications à propos des fonctions étudiées.
- Position et justification de la présence des fonctions au sein du système ;
- Schéma fonctionnel de 2nd degré des fonctions principales ;
- Schémas structurels avec repérage des fonctions secondaires ;
- Définitions des liaisons ;
- Etude détaillée de chaque fonction secondaire qui peut comporter par exemple :
    - Schéma structurel de la fonction secondaire ;
    - Explications du fonctionnement de la fonction secondaire ;
    - Calcul ou justification des composants ;
    - Définitions des points tests ;
    - Chronogrammes théoriques et/ou oscillogrammes ;
    - Algorithme de fonctionnement ;
    - Programme de test ;
    - Etc…
- Méthode de mise en œuvre des cartes ;
- Relevés des mesures.

3. Algorithme et programmation éventuels des cartes étudiées.

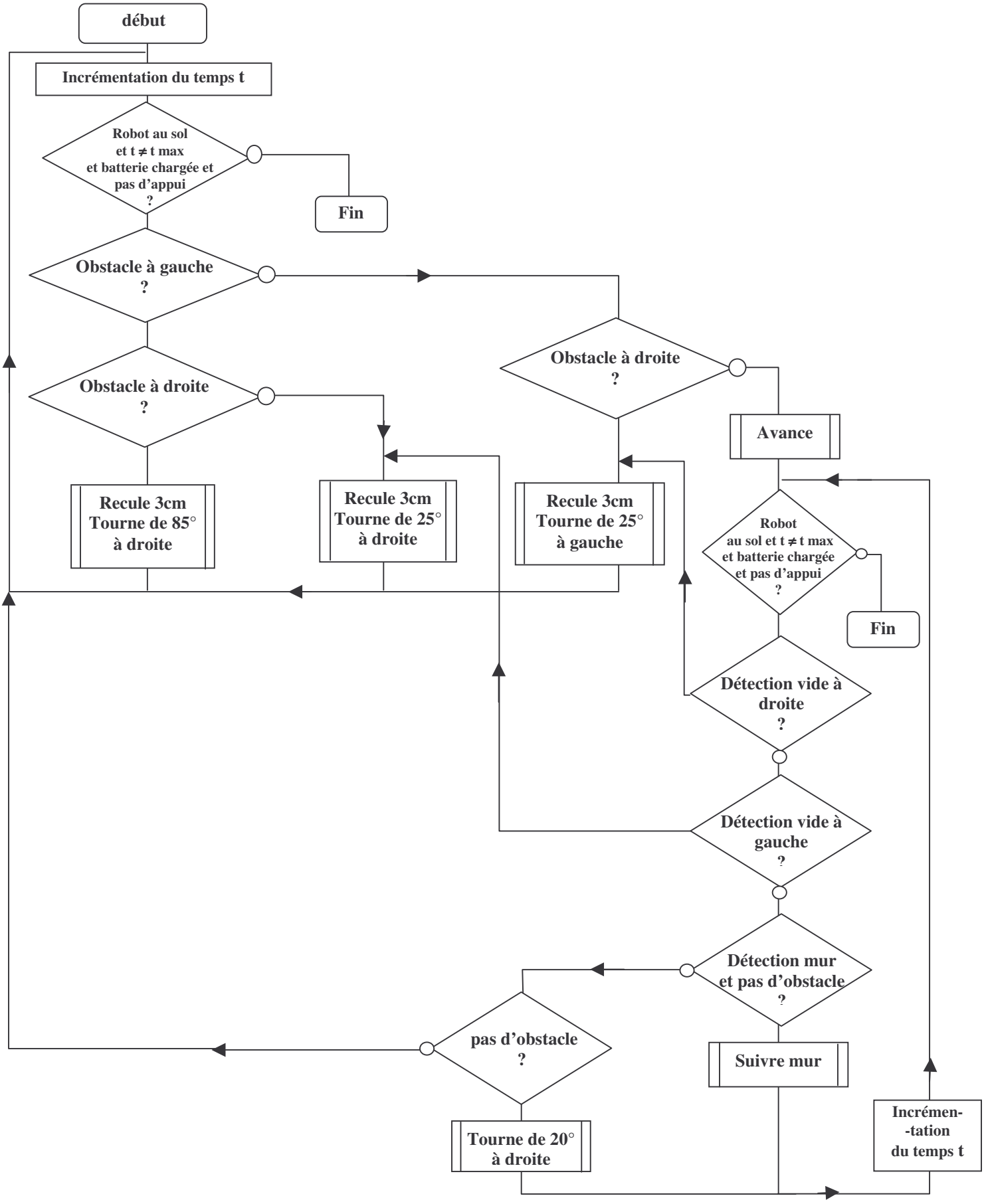
4. Documents de fabrication.
- Schémas structurels (réalisés par le binôme) et nomenclatures.
- Typons avec identification des faces et schémas d'implantation.
- Plan de câblage (définition de la connectique).

5. Annexe : Documentations des fabricants de composants.

7. Algorigrammes



Fonctionnement mode Max ou Clean : (simplifié : on ne tient pas compte de OT2, OT3, OT4)



- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

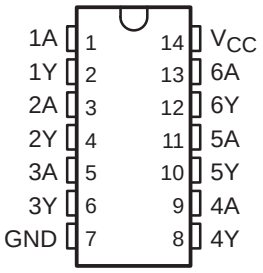
These devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$ in positive logic. The open-drain outputs require pullup resistors to perform correctly. They may be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

The SN54HC05 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC05 is characterized for operation from –40°C to 85°C.

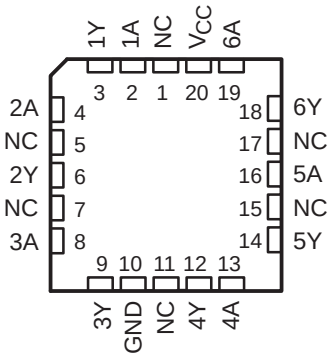
FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

SN54HC05 . . . J OR W PACKAGE
SN74HC05 . . . D OR N PACKAGE
(TOP VIEW)

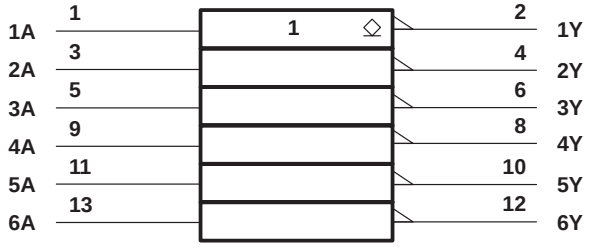


SN54HC05 . . . FK PACKAGE
(TOP VIEW)



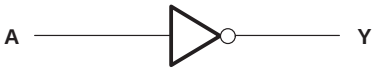
NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 127°C/W
N package . . . . . 78°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

			SN54HC05			SN74HC05			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC05		SN74HC05		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
I_{OH}	$V_I = V_{IH}$ or V_{IL}, $V_O = V_{CC}$		6 V		0.01	0.5		10		5	µA
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, $I_O = 0$		6 V			2		40		20	µA
C_i			2 V to 6 V		3	10		10		10	pF

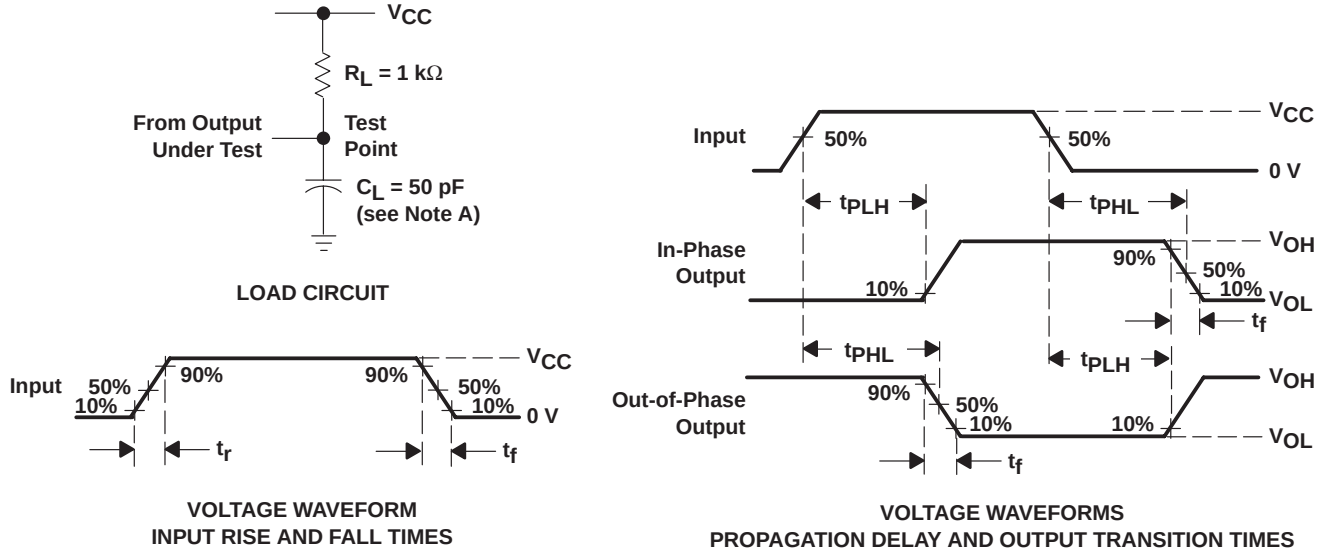
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC05		SN74HC05		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2 V		60	115		175		145	ns
			4.5 V		13	23		35		29	
			6 V		10	20		30		25	
t_{PHL}	A	Y	2 V		45	85		130		105	ns
			4.5 V		9	17		26		21	
			6 V		8	14		22		18	
t_f		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per inverter	No load	20	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

MC54/74HC595A

8-Bit Serial-Input/Serial or Parallel-Output Shift Register with Latched 3-State Outputs

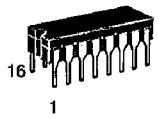
High–Performance Silicon–Gate CMOS

The MC54/74HC595A is identical in pinout to the LS595. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC595A consists of an 8–bit shift register and an 8–bit D–type latch with three–state parallel outputs. The shift register accepts serial data and provides a serial output. The shift register also provides parallel data to the 8–bit latch. The shift register and latch have independent clock inputs. This device also has an asynchronous reset for the shift register.

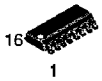
The HC595A directly interfaces with the Motorola SPI serial data port on CMOS MPUs and MCUs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 328 FETs or 82 Equivalent Gates
- Improvements over HC595
  - — Improved Propagation Delays
  - — 50% Lower Quiescent Power
  - — Improved Input Noise and Latchup Immunity



J SUFFIX
CERAMIC PACKAGE
CASE 620–10

N SUFFIX
PLASTIC PACKAGE
CASE 648–08



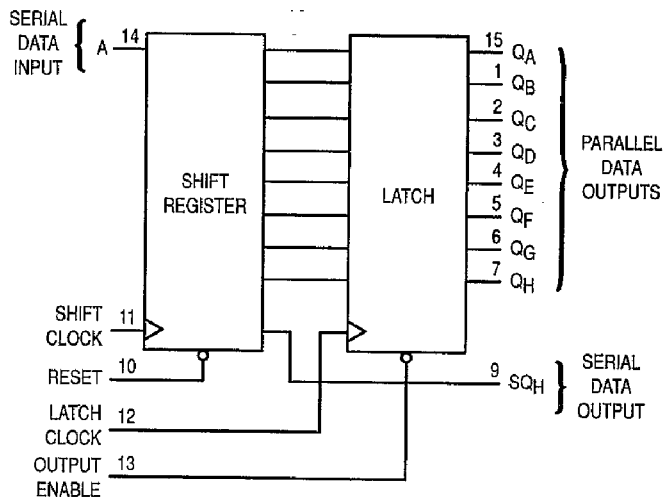
D SUFFIX
SOIC PACKAGE
CASE 751B–05

DT SUFFIX
TSSOP PACKAGE
CASE 948F–01

ORDERING INFORMATION

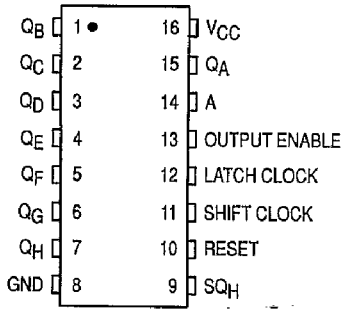
MC54HCXXXAJ	Ceramic
MC74HCXXXAN	Plastic
MC74HCXXXAD	SOIC
MC74HCXXXADT	TSSOP

LOGIC DIAGRAM



V_{CC} = PIN 16
GND = PIN 8

PIN ASSIGNMENT



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 1.5 to V_{CC} + 1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package) (Ceramic DIP)	 260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
Ceramic DIP: – 10 mW/°C from 100° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

3

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage, Q_A – Q_H	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 6.0 mA $\|I_{out}\|$ ≤ 7.8 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.7 5.2	
V_{OL}	Maximum Low–Level Output Voltage, Q_A – Q_H	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 6.0 mA $\|I_{out}\|$ ≤ 7.8 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.4 0.4	

NOTE: Information on typical parametric values can be found in Chapter 2.

DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{OH}	Minimum High–Level Output Voltage, SQ_H	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 4.0$ mA $\|I_{out}\| \leq 5.2$ mA	4.5 6.0	3.98 5.48	3.84 5.34	3.7 5.2	
V_{OL}	Maximum Low–Level Output Voltage, SQ_H	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 4.0$ mA $\|I_{out}\| \leq 5.2$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.4 0.4	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three–State Leakage Current, $Q_A - Q_H$	Output in High–Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ μA	6.0	4.0	40	160	μA

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6.0$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 7)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Shift Clock to SQ_H (Figures 1 and 7)	2.0 4.5 6.0	140 28 24	175 35 30	210 42 36	ns
t_{PHL}	Maximum Propagation Delay, Reset to SQ_H (Figures 2 and 7)	2.0 4.5 6.0	145 29 25	180 36 31	220 44 38	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Latch Clock to $Q_A - Q_H$ (Figures 3 and 7)	2.0 4.5 6.0	140 28 24	175 35 30	210 42 36	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to $Q_A - Q_H$ (Figures 4 and 8)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to $Q_A - Q_H$ (Figures 4 and 8)	2.0 4.5 6.0	135 27 23	170 34 29	205 41 35	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, $Q_A - Q_H$ (Figures 3 and 7)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, SQ_H (Figures 1 and 7)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State), $Q_A - Q_H$	—	15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2.

		Typical @ 25°C, $V_{CC} = 5.0$ V	
C_{PD}	Power Dissipation Capacitance (Per Package)*	300	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2.

TIMING REQUIREMENTS (Input $t_r = t_f = 6.0$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to −55°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Serial Data Input A to Shift Clock (Figure 5)	2.0 4.5 6.0	50 10 9.0	65 13 11	75 15 13	ns
t_{su}	Minimum Setup Time, Shift Clock to Latch Clock (Figure 6)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
t_h	Minimum Hold Time, Shift Clock to Serial Data Input A (Figure 5)	2.0 4.5 6.0	5.0 5.0 5.0	5.0 5.0 5.0	5.0 5.0 5.0	ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Shift Clock (Figure 2)	2.0 4.5 6.0	50 10 9.0	65 13 11	75 15 13	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
t_w	Minimum Pulse Width, Shift Clock (Figure 1)	2.0 4.5 6.0	50 10 9.0	65 13 11	75 15 13	ns
t_w	Minimum Pulse Width, Latch Clock (Figure 6)	2.0 4.5 6.0	50 10 9.0	65 13 11	75 15 13	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

3

FUNCTION TABLE

Operation	Inputs					Resulting Function			
	Reset	Serial Input A	Shift Clock	Latch Clock	Output Enable	Shift Register Contents	Latch Register Contents	Serial Output SQ_H	Parallel Outputs $Q_A - Q_H$
Reset shift register	L	X	X	L, H, ↘	L	L	U	L	U
Shift data into shift register	H	D	↗	L, H, ↘	L	$D \rightarrow SR_A$; $SR_N \rightarrow SR_{N+1}$	U	$SR_G \rightarrow SR_H$	U
Shift register remains unchanged	H	X	L, H, ↘	L, H, ↘	L	U	U	U	U
Transfer shift register contents to latch register	H	X	L, H, ↘	↗	L	U	$SR_N \rightarrow LR_N$	U	SR_N
Latch register remains unchanged	X	X	X	L, H, ↘	L	*	U	*	U
Enable parallel outputs	X	X	X	X	L	*	**	*	Enabled
Force outputs into high impedance state	X	X	X	X	H	*	**	*	Z

SR = shift register contents
LR = latch register contents
D = data (L, H) logic level
U = remains unchanged
X = don't care
Z = high impedance
* = depends on Reset and Shift Clock inputs
** = depends on Latch Clock input

PIN DESCRIPTIONS

INPUTS

A (Pin 14)

Serial Data Input. The data on this pin is shifted into the 8–bit serial shift register.

CONTROL INPUTS

Shift Clock (Pin 11)

Shift Register Clock Input. A low– to–high transition on this input causes the data at the Serial Input pin to be shifted into the 8–bit shift register.

Reset (Pin 10)

Active–low, Asynchronous, Shift Register Reset Input. A low on this pin resets the shift register portion of this device only. The 8–bit latch is not affected.

Latch Clock (Pin 12)

Storage Latch Clock Input. A low–to–high transition on this input latches the shift register data.

Output Enable (Pin 13)

Active–low Output Enable. A low on this input allows the data from the latches to be presented at the outputs. A high on this input forces the outputs (Q_A–Q_H) into the high–impedance state. The serial output is not affected by this control unit.

OUTPUTS

Q_A – Q_H (Pins 15, 1, 2, 3, 4, 5, 6, 7)

Noninverted, 3–state, latch outputs.

SQ_H (Pin 9)

Noninverted, Serial Data Output. This is the output of the eighth stage of the 8–bit shift register. This output does not have three–state capability.

3

SWITCHING WAVEFORMS

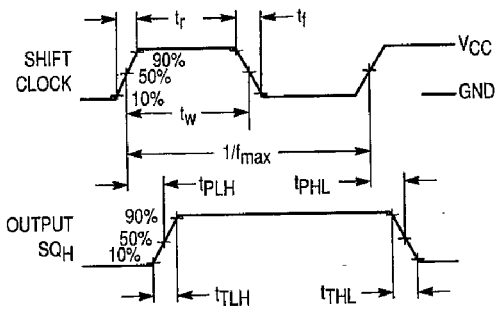


Figure 1.

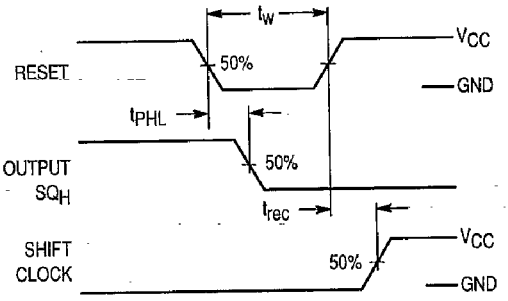


Figure 2.

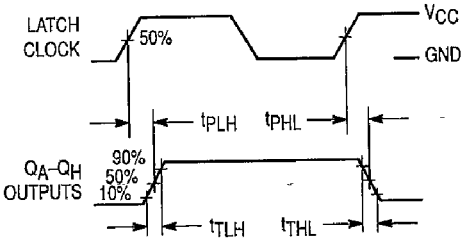


Figure 3.

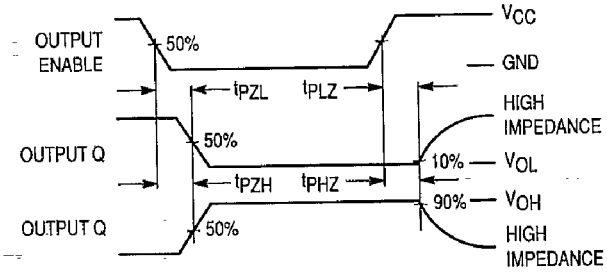


Figure 4.

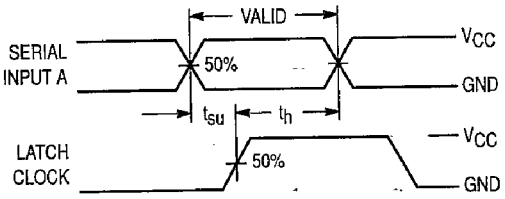


Figure 5.

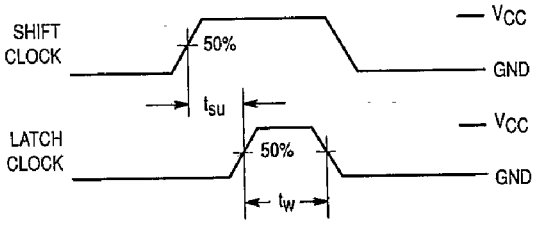
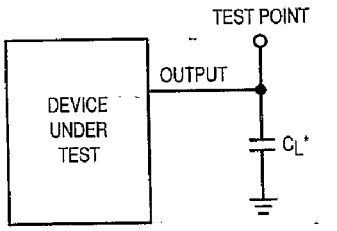


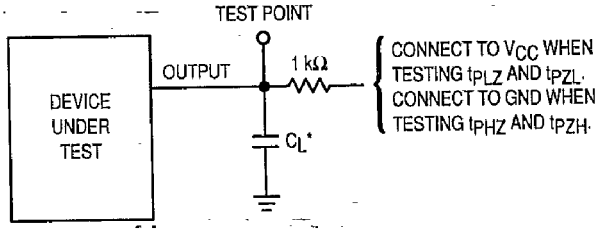
Figure 6.

TEST CIRCUITS



* Includes all probe and jig capacitance

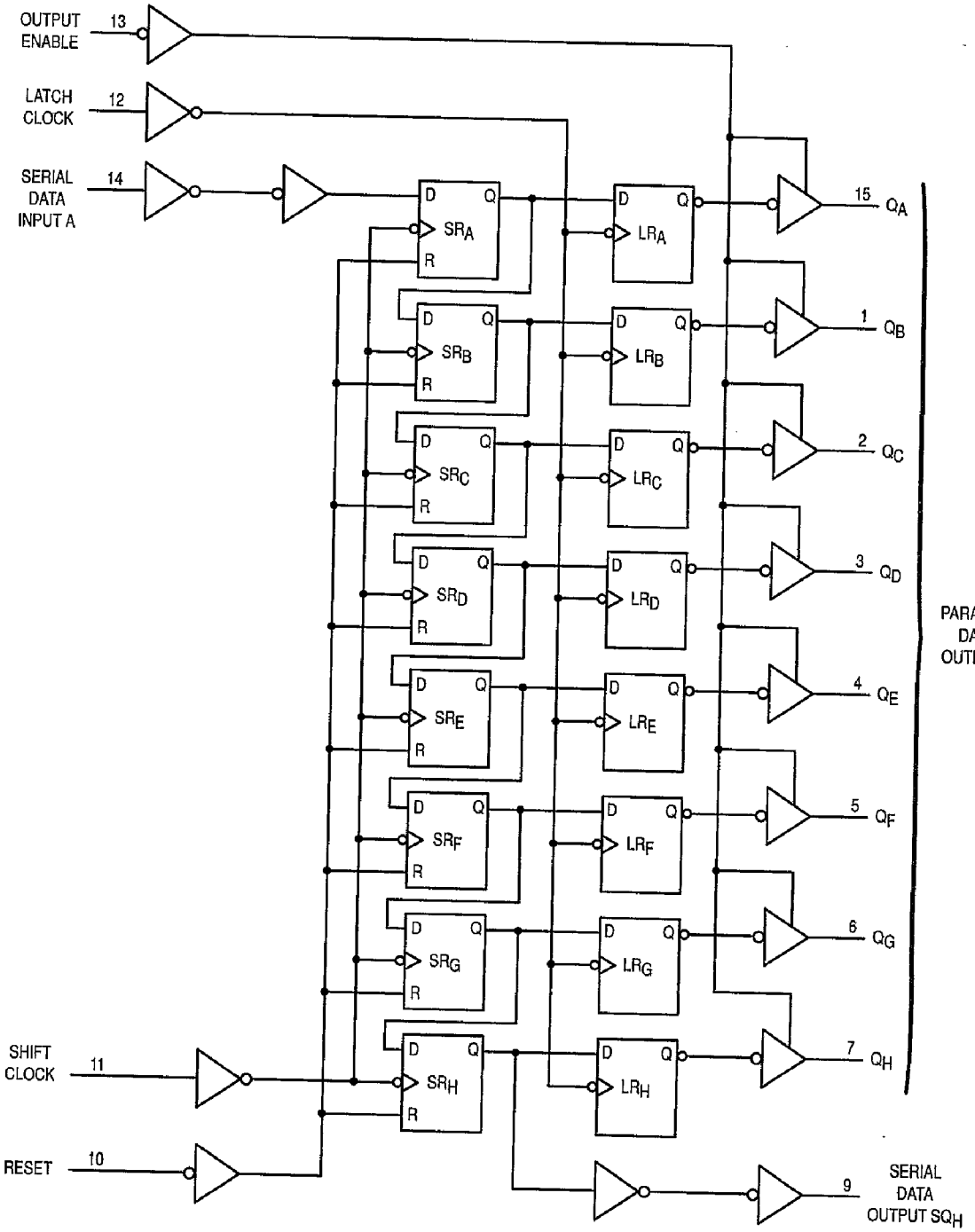
Figure 7.



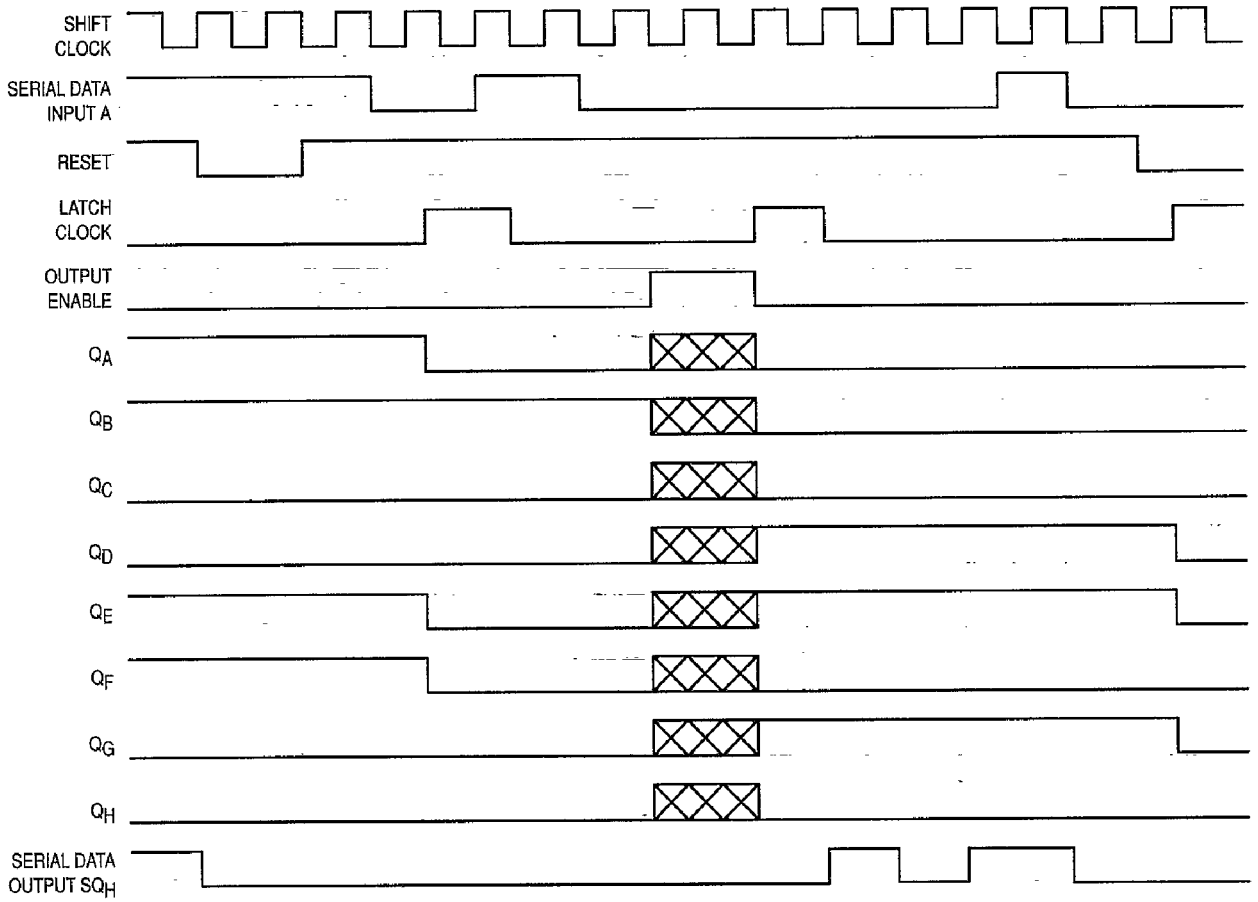
* Includes all probe and jig capacitance

Figure 8.

EXPANDED LOGIC DIAGRAM



TIMING DIAGRAM



NOTE: ⊠ implies that the output is in a high–impedance state.

3

National Semiconductor

June 1989

LM78L00 Series
3-Terminal Positive Voltage Regulators

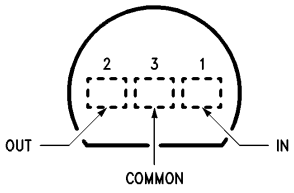
General Description

The LM78L00 series of 3-terminal positive voltage regulators employ internal current-limiting and thermal shutdown, making them essentially indestructible. If adequate heat sinking is provided, they can deliver up to 100 mA output current. They are intended as fixed voltage regulators in a wide range of applications including local (on-card) regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used with power pass elements to make high current voltage regulators. The LM78L00, used as a Zener diode/resistor combination replacement, offers an effective output impedance improvement of typically two orders of magnitude, along with lower quiescent current and lower noise.

Features

- Output current up to 100 mA
- No external components
- Internal thermal overload protection
- Internal short circuit current-limiting
- Available in JEDEC TO-92
- Output Voltages of 5.0V, 6.2V, 8.2V, 9.0V, 12V, 15V
- Output voltage tolerances of ±5% over the temperature range

Connection Diagram



TL/H/10051–1

Top View

Order Number LM78L05ACZ, LM78L09ACZ,
LM78L12ACZ, LM78L15ACZ, LM78L62ACZ or LM78L82ACZ
See NS Package Number Z03A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	−65°C to +150°C
Operation Junction Temperature Range	
Commercial (LM78L00AC)	0°C to +125°C
Lead Temperature	
TO-92 Package/SO-8	
(Soldering, 10 sec.)	265°C
Power Dissipation	Internally Limited
Input Voltage	
5.0V to 15V	35V
ESD Susceptibility	to be determined

LM78L05AC
Electrical Characteristics

0°C ≤ T_A ≤ +125°C, V_I = 10V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, unless otherwise specified (Note 1)

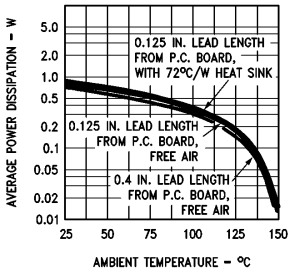
Symbol	Parameter		Conditions		Min	Typ	Max	Units
V_O	Output Voltage		T_J = 25°C		4.8	5.0	5.2	V
$V_{R\ LINE}$	Line Regulation		T_J = 25°C	7.0V ≤ V_I ≤ 20V		55	150	mV
				8.0V ≤ V_I ≤ 20V		45	100	
$V_{R\ LOAD}$	Load Regulation		T_J = 25°C	1.0 mA ≤ I_O ≤ 100V		11	60	mV
				1.0 mA ≤ I_O ≤ 40 mA		5.0	30	
V_O	Output Voltage (Note 2)		7.0V ≤ V_I ≤ 20V	1.0 mA ≤ I_O ≤ 40 mA	4.75		5.25	V
			7.0V ≤ V_I ≤ V_{Max}	1.0 mA ≤ I_O ≤ 70 mA	4.75		5.25	
I_Q	Quiescent Current					2.0	5.5	mA
ΔI_Q	Quiescent Current Change	With Line	8.0V ≤ V_I ≤ 20V				1.5	mA
		With Load	1.0 mA ≤ I_O ≤ 40 mA				0.1	
N_O	Noise		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			40		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		f = 120 Hz, 8.0V ≤ V_I ≤ 18V, T_J = 25°C		41	49		dB
V_{DO}	Dropout Voltage		T_J = 25°C			1.7		V
I_{pk}/I_{OS}	Peak Output/Output Short Circuit Current		T_J = 25°C			140		mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		I_O = 5.0 mA			−0.65		mV/°C

Note 1: The maximum steady state usable output current and input voltage are very dependent on the heat sinking and/or lead length of the package. The data above represent pulse test conditions with junction temperatures as indicated at the initiation of tests.

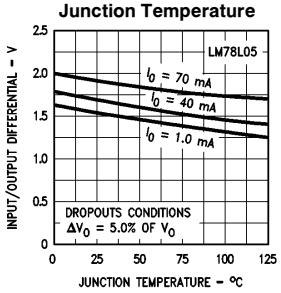
Note 2: Power Dissipation ≤ 0.75W.

Typical Performance Characteristics

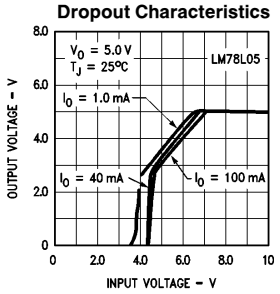
Worst Case Power Dissipation vs Ambient Temperature (TO-92)



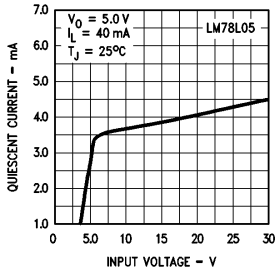
Dropout Voltage vs Junction Temperature



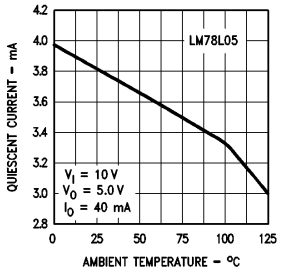
Dropout Characteristics



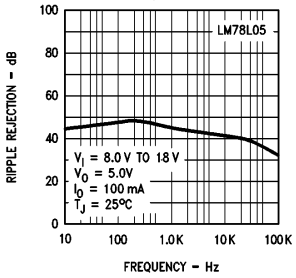
Quiescent Current vs Input Voltage



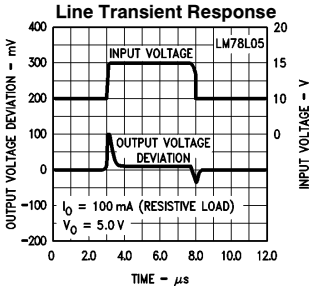
Quiescent Current vs Temperature



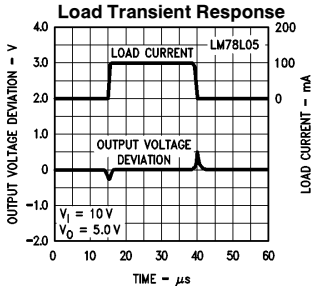
Ripple Rejection vs Frequency



Line Transient Response



Load Transient Response

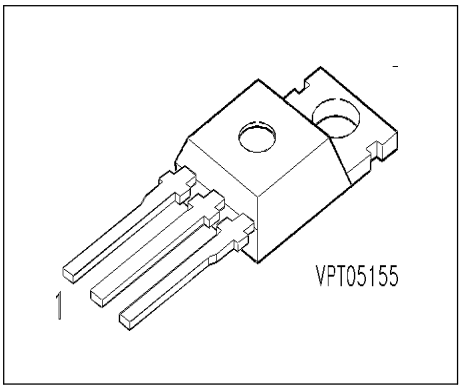


TL/H/10051–3

Note: Other LM78L00 Series devices have similar curves.

SIPMOS ® Power Transistor

- N channel
- Enhancement mode
- Avalanche-rated
- d*v*/d*t* rated
- Ultra low on-resistance
- 175°C operating temperature
- also in TO-220 SMD available



Pin 1	Pin 2	Pin 3
G	D	S

Type	V_{DS}	I_D	$R_{DS(on)}$	Package	Ordering Code
BUZ 100	50 V	60 A	0.018 Ω	TO-220 AB	C67078-S1348-A2

Maximum Ratings

Parameter	Symbol	Values	Unit
Continuous drain current T_C = 101 °C	I_D	60	A
Pulsed drain current T_C = 25 °C	I_{Dpuls}	240	
Avalanche energy, single pulse I_D = 60 A, V_{DD} = 25 V, R_{GS} = 25 Ω L = 70 µH, T_j = 25 °C	E_{AS}	250	mJ
Reverse diode d*v*/d*t* I_S = 60 A, V_{DS} = 40 V, di_F/dt = 200 A/µs T_{jmax} = 175 °C	d*v*/d*t*	6	kV/µs
Gate source voltage	V_{GS}	± 20	V
Power dissipation T_C = 25 °C	P_{tot}	250	W
Operating temperature	T_j	-55 ... + 175	°C
Storage temperature	T_{stg}	-55 ... + 175	
Thermal resistance, chip case	R_{thJC}	≤ 0.6	K/W
Thermal resistance, chip to ambient	R_{thJA}	≤ 75	
DIN humidity category, DIN 40 040		E	
IEC climatic category, DIN IEC 68-1		55 / 175 / 56	

Electrical Characteristics, at T_j = 25°C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static Characteristics					
Drain- source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA, T_j = -40 °C	$V_{(BR)DSS}$	50	-	-	V
Gate threshold voltage V_{GS}=V_{DS}, I_D = 1 mA	$V_{GS(th)}$	2.1	3	4	
Zero gate voltage drain current	I_{DSS}				
V_{DS} = 50 V, V_{GS} = 0 V, T_j = 25 °C		-	0.1	1	µA
V_{DS} = 50 V, V_{GS} = 0 V, T_j = -40 °C		-	1	100	nA
V_{DS} = 50 V, V_{GS} = 0 V, T_j = 150 °C		-	10	100	µA
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	-	10	100	nA
Drain-Source on-resistance V_{GS} = 10 V, I_D = 60 A	$R_{DS(on)}$	-	0.013	0.018	Ω

Electrical Characteristics, at T_j = 25°C, unless otherwise specified

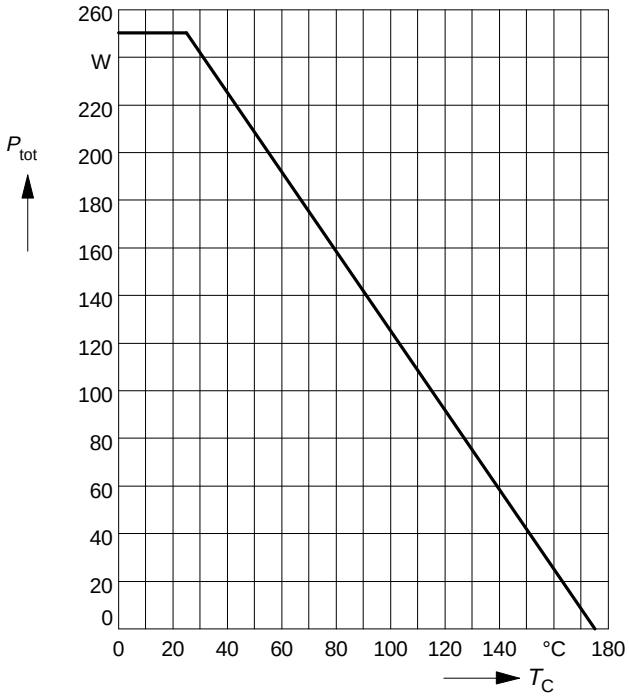
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Dynamic Characteristics					
Transconductance $V_{DS} \geq 2 * I_D * R_{DS(on)max}$, I_D = 60 A	g_{fs}	25	39	-	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	2400	3200	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	-	800	1200	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	-	300	450	
Turn-on delay time V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A R_{GS} = 50 Ω	$t_{d(on)}$	-	40	60	ns
Rise time V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A R_{GS} = 50 Ω	t_r	-	100	150	
Turn-off delay time V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A R_{GS} = 50 Ω	$t_{d(off)}$	-	250	335	
Fall time V_{DD} = 30 V, V_{GS} = 10 V, I_D = 3 A R_{GS} = 50 Ω	t_f	-	140	190	

Electrical Characteristics, at T_j = 25°C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse Diode					
Inverse diode continuous forward current T_C = 25 °C	I_S	-	-	60	A
Inverse diode direct current,pulsed T_C = 25 °C	I_{SM}	-	-	240	
Inverse diode forward voltage V_{GS} = 0 V, I_F = 120 A	V_{SD}	-	1.4	1.8	V
Reverse recovery time V_R = 30 V, I_F=I_S, di_F/dt = 100 A/µs	t_{rr}	-	70	-	ns
Reverse recovery charge V_R = 30 V, I_F=I_S, di_F/dt = 100 A/µs	Q_{rr}	-	0.16	-	µC

Power dissipation

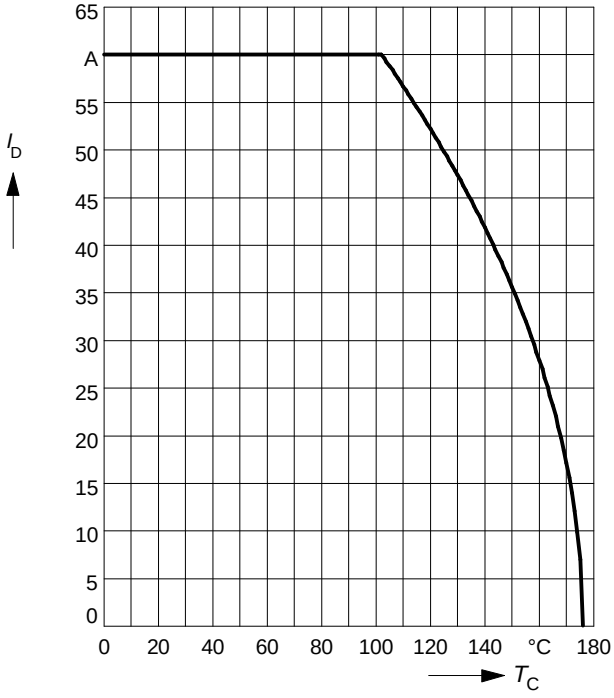
$P_{tot} = f(T_C)$



Drain current

$I_D = f(T_C)$

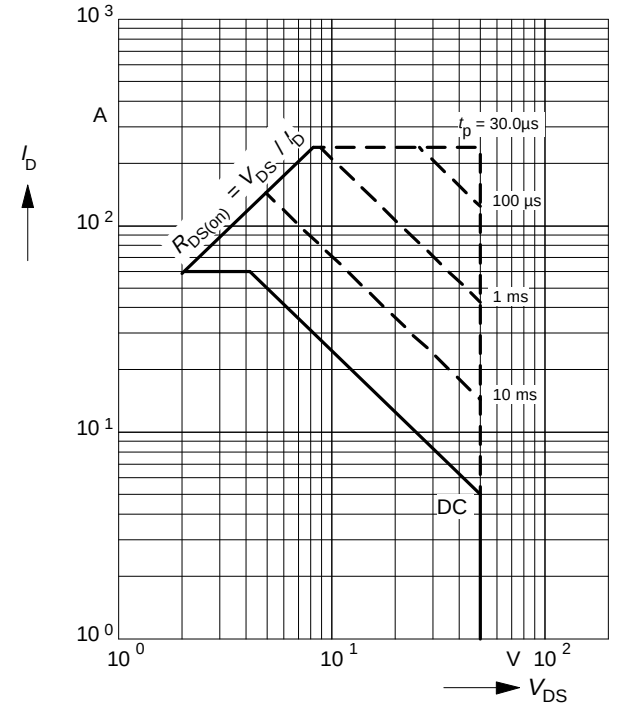
parameter: $V_{GS} \geq 10$ V



Safe operating area

$I_D = f(V_{DS})$

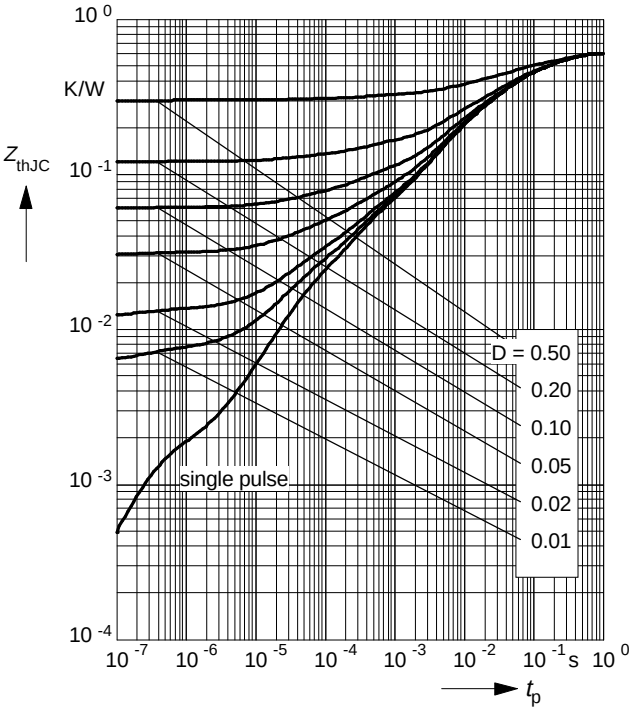
parameter: $D = 0.01$, $T_C = 25$°C



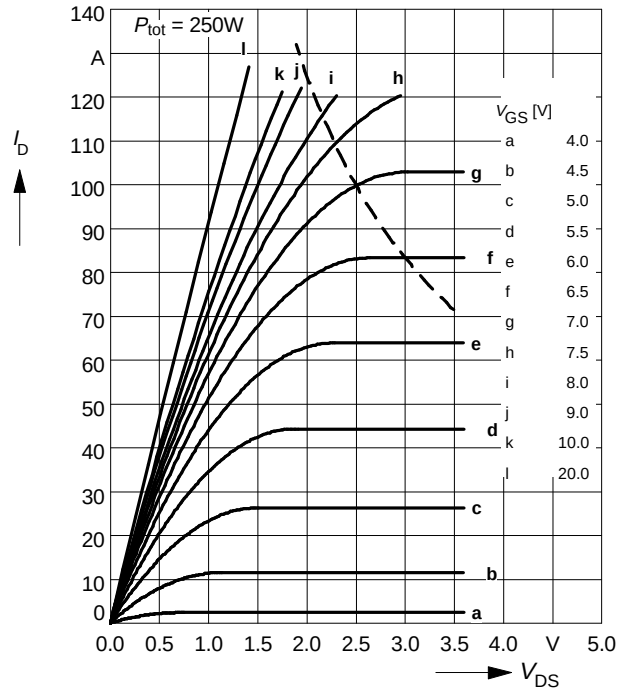
Transient thermal impedance

$Z_{th\,JC} = f(t_p)$

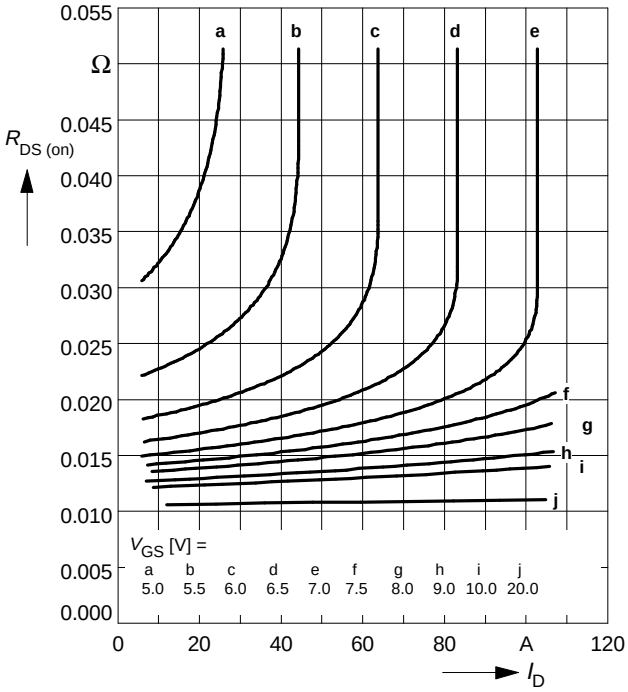
parameter: $D = t_p / T$



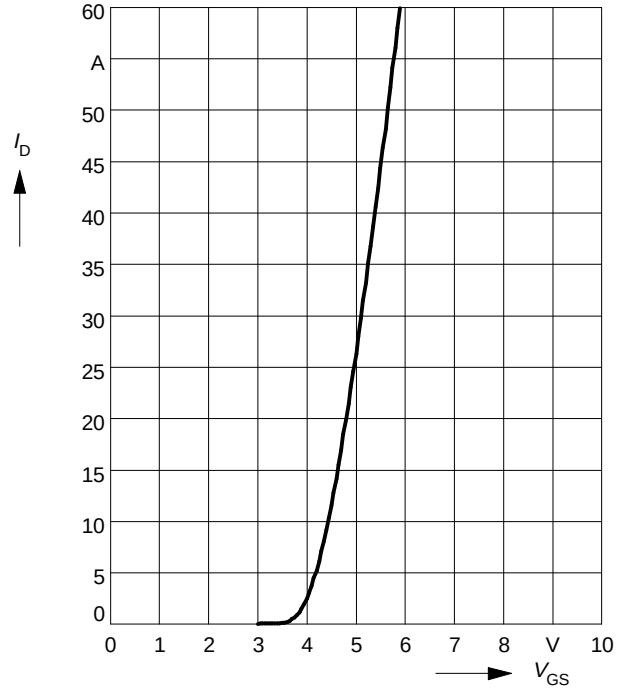
Typ. output characteristics
$I_D = f(V_{DS})$
parameter: t_p = 80 µs



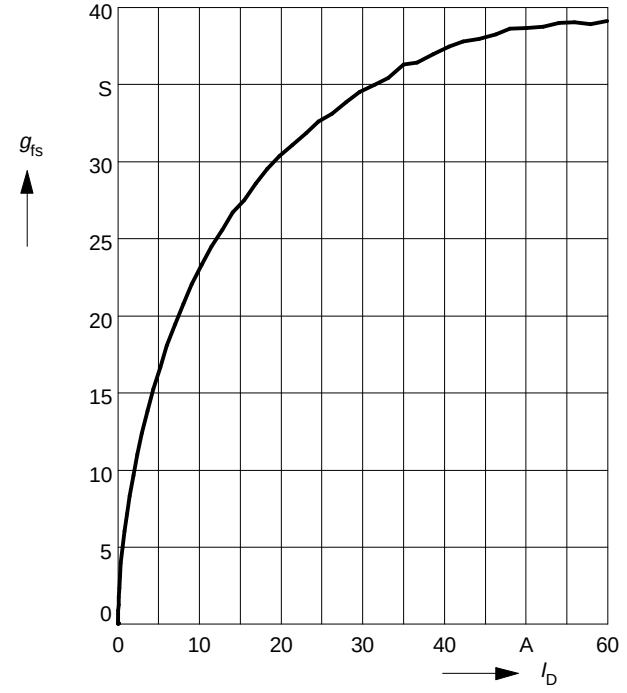
Typ. drain-source on-resistance
$R_{DS\ (on)} = f(I_D)$
parameter: V_{GS}



Typ. transfer characteristics $I_D = f(V_{GS})$
parameter: t_p = 80 µs
$V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$



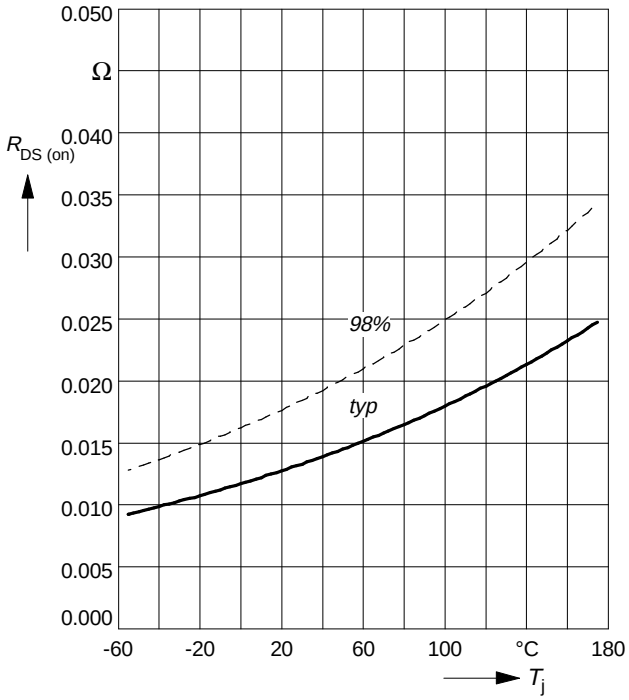
Typ. forward transconductance $g_{fs} = f(I_D)$
parameter: t_p = 80 µs,
$V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$



Drain-source on-resistance

$R_{DS\ (on)} = f(T_j)$

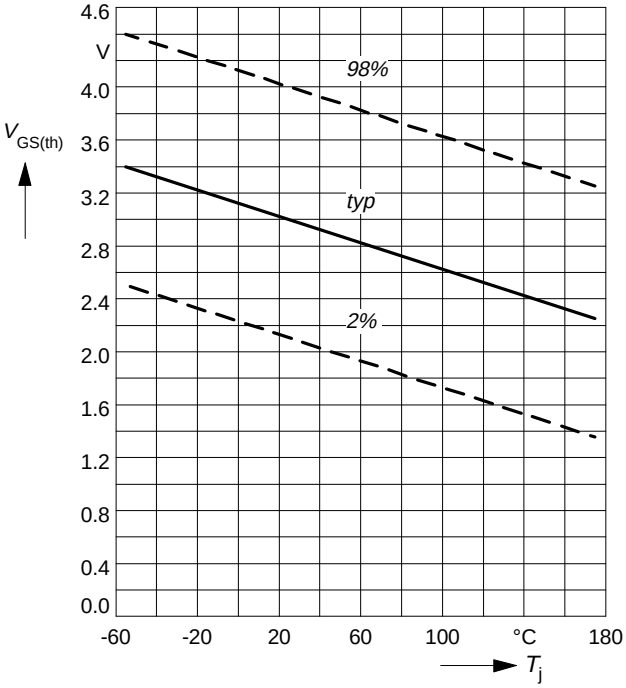
parameter: I_D = 60 A, V_{GS} = 10 V



Gate threshold voltage

$V_{GS\ (th)} = f(T_j)$

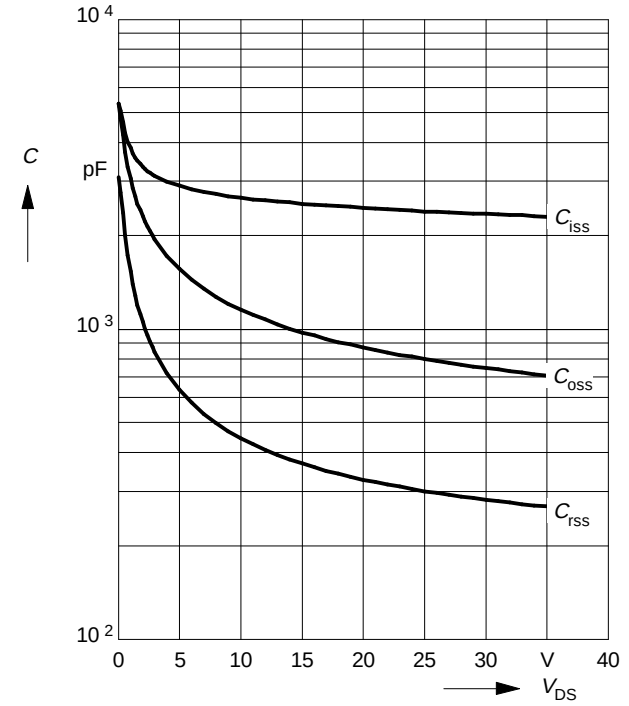
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA



Typ. capacitances

$C = f(V_{DS})$

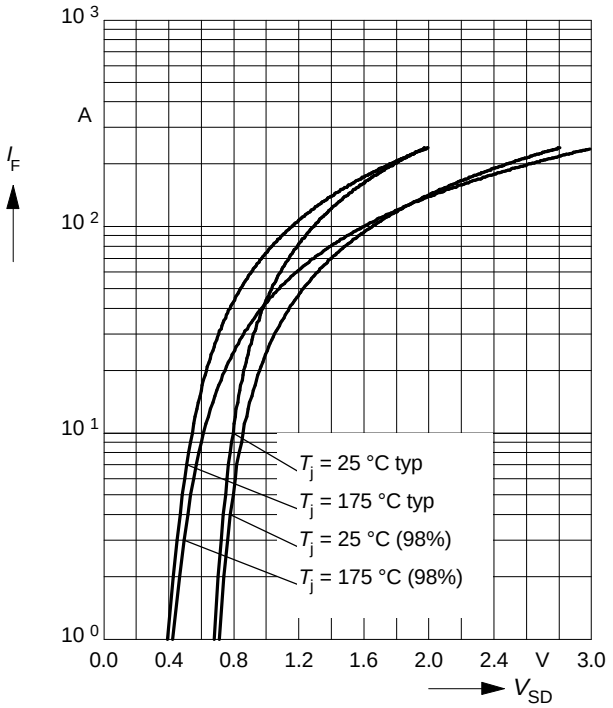
parameter: V_{GS} = 0V, f = 1MHz



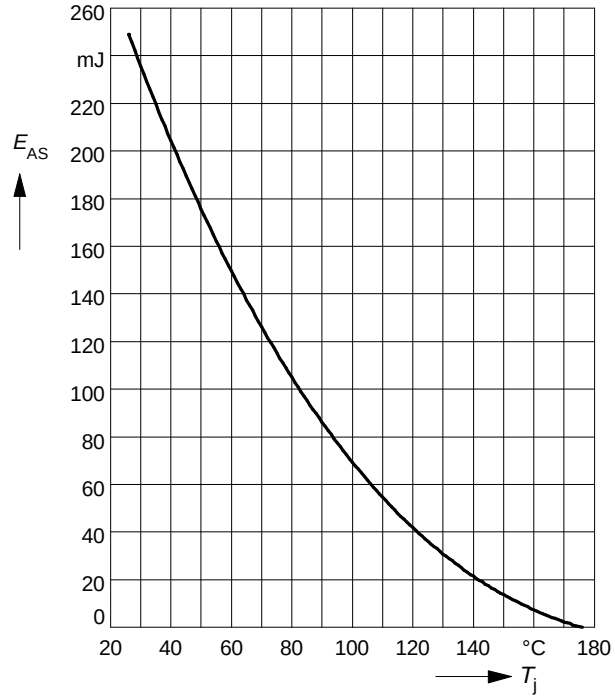
Forward characteristics of reverse diode

$I_F = f(V_{SD})$

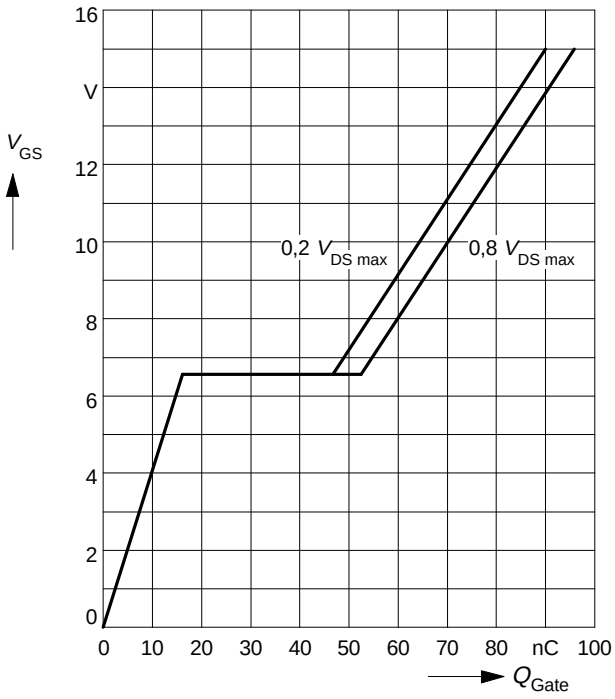
parameter: T_j, t_p = 80 µs



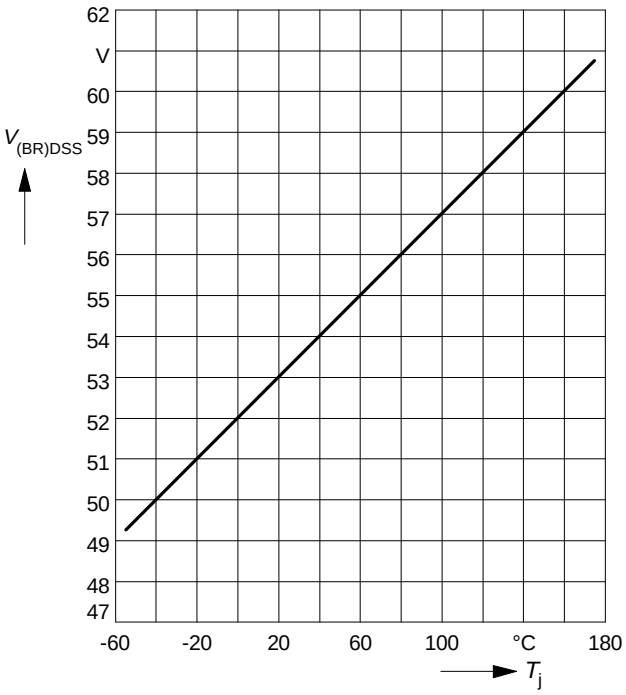
Avalanche energy $E_{AS} = f(T_j)$
parameter: I_D = 60 A, V_{DD} = 25 V
R_{GS} = 25 Ω, L = 70 µH



Typ. gate charge
$V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls}$ = 90 A



Drain-source breakdown voltage
$V_{(BR)DSS} = f(T_j)$



National Semiconductor

February 1988

CD4071BM/CD4071BC
Quad 2-Input OR Buffered B Series Gate
CD4081BM/CD4081BC
Quad 2-Input AND Buffered B Series Gate

General Description

These quad gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain.

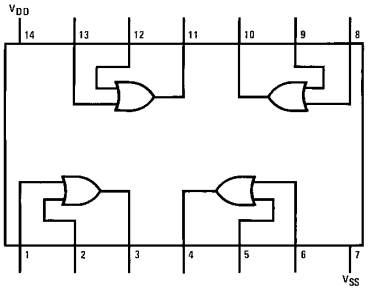
All inputs protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

- Low power TTL compatibility — Fan out of 2 driving 74L or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range

Connection Diagrams

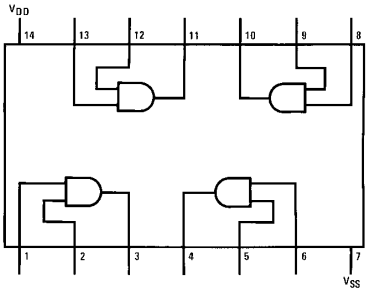
CD4071B Dual-In-Line Package



TL/F/5977–3

Top View

CD4081B Dual-In-Line Package



TL/F/5977–6

Top View

Order Number CD4071B or CD4081B

 TL/F/5977

RRD-B30M105/Printed in U. S. A.

CD4071BM/CD4071BC Quad 2-Input OR Buffered B Series Gate
CD4081BM/CD4081BC Quad 2-Input AND Buffered B Series Gate

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	$-0.5V$ to $V_{DD} + 0.5V$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
V_{DD} Range	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
Storage Temperature (T_S)	$-65°C$ to $+150°C$
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

Operating Range (V_{DD})	$3\ V_{DC}$ to $15\ V_{DC}$
Operating Temperature Range (T_A)	
CD4071BM, CD4081BM	$-55°C$ to $+125°C$
CD4071BC, CD4081BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4071BM/CD4081BM (Note 2)

Symbol	Parameter	Conditions	$-55°C$		$+25°C$			$+125°C$		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		0.25		0.004	0.25		7.5	μA
		$V_{DD} = 10V$		0.50		0.005	0.50		15	μA
		$V_{DD} = 15V$		1.0		0.006	1.0		30	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$ | $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$ | $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$ | $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$ | $\lvert I_O \rvert < 1\ \mu A$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$ | $\lvert I_O \rvert < 1\ \mu A$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$ | $\lvert I_O \rvert < 1\ \mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$		1.5		2	1.5		1.5	V
		$V_{DD} = 10V, V_O = 1.0V$		3.0		4	3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V, V_O = 4.5V$	3.5		3.5	3		3.5		V
		$V_{DD} = 10V, V_O = 9.0V$	7.0		7.0	6		7.0		V
		$V_{DD} = 15V, V_O = 13.5V$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	-0.64		-0.51	-0.88		-0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	-1.6		-1.3	-2.25		-0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	-4.2		-3.4	-8.8		-2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.10		-10^{-5}	-0.10		-1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.10		10^{-5}	0.10		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

DC Electrical Characteristics CD4071BC/CD4081BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		1		0.004	1		7.5	μA
		$V_{DD} = 10V$		2		0.005	2		15	μA
		$V_{DD} = 15V$		4		0.006	4		30	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$ } $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$ } $\lvert I_O \rvert < 1\ \mu A$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$		1.5		2	1.5		1.5	V
		$V_{DD} = 10V, V_O = 1.0V$		3.0		4	3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V, V_O = 4.5V$	3.5		3.5	3		3.5		V
		$V_{DD} = 10V, V_O = 9.0V$	7.0		7.0	6		7.0		V
		$V_{DD} = 15V, V_O = 13.5V$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	−1.3		−1.1	−2.25		−0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		−0.30		-10^{-5}	−0.30		−1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics* CD4071BC/CD4071BM

$T_A = 25°C$, Input t_r; $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200\ k\Omega$, Typical temperature coefficient is 0.3%/°C

Symbol	Parameter	Conditions	Typ	Max	Units
t_{PHL}	Propagation Delay Time, High-to-Low Level	$V_{DD} = 5V$	100	250	ns
		$V_{DD} = 10V$	40	100	ns
		$V_{DD} = 15V$	30	70	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level	$V_{DD} = 5V$	90	250	ns
		$V_{DD} = 10V$	40	100	ns
		$V_{DD} = 15V$	30	70	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$	90	200	ns
		$V_{DD} = 10V$	50	100	ns
		$V_{DD} = 15V$	40	80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	18		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

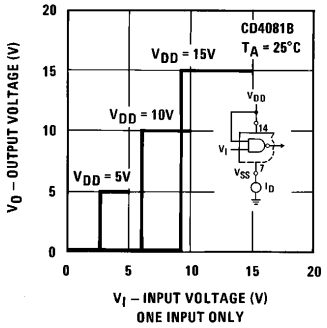
AC Electrical Characteristics* CD4081BC/CD4081BM

T_A = 25°C, Input t_r; t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ, Typical temperature coefficient is 0.3%/°C

Symbol	Parameter	Conditions	Typ	Max	Units
t_{PHL}	Propagation Delay Time, High-to-Low Level	V_{DD} = 5V	100	250	ns
		V_{DD} = 10V	40	100	ns
		V_{DD} = 15V	30	70	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level	V_{DD} = 5V	120	250	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	35	70	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V	90	200	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	40	80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	18		pF

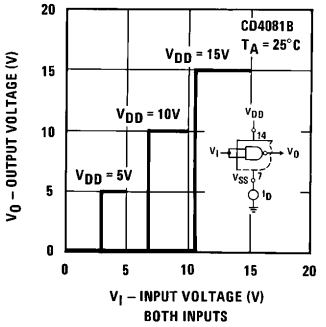
*AC Parameters are guaranteed by DC correlated testing.

Typical Performance Characteristics



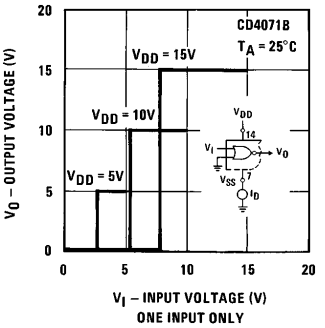
TL/F/5977–7

FIGURE 1. Typical Transfer Characteristics



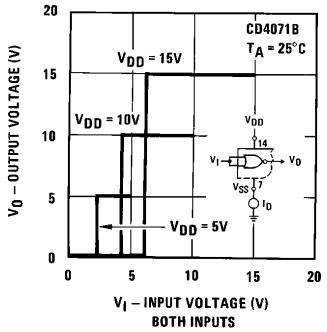
TL/F/5977–8

FIGURE 2. Typical Transfer Characteristics



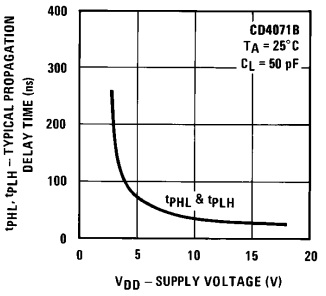
TL/F/5977–9

FIGURE 3. Typical Transfer Characteristics



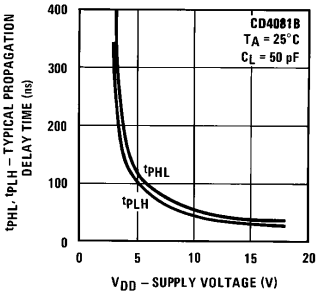
TL/F/5977–10

FIGURE 4. Typical Transfer Characteristics



TL/F/5977–11

FIGURE 5



TL/F/5977–12

FIGURE 6

National Semiconductor

February 1988

CD4538BM/CD4538BC Dual Precision Monostable

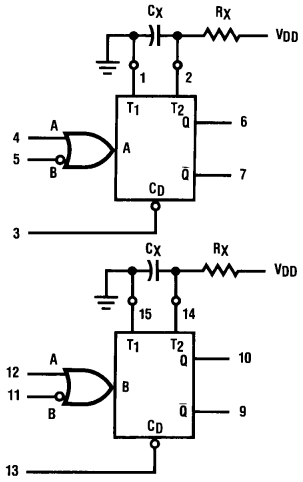
General Description

The CD4538B is a dual, precision monostable multivibrator with independent trigger and reset controls. The device is retriggerable and resettable, and the control inputs are internally latched. Two trigger inputs are provided to allow either rising or falling edge triggering. The reset inputs are active low and prevent triggering while active. Precise control of output pulse-width has been achieved using linear CMOS techniques. The pulse duration and accuracy are determined by external components R_X and C_X. The device does not allow the timing capacitor to discharge through the timing pin on power-down condition. For this reason, no external protection resistor is required in series with the timing pin. Input protection from static discharge is provided on all pins.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power — Fan out of 2 driving 74L
  TTL compatibility — or 1 driving 74LS
- New formula: $PW_{OUT} = RC$
  (PW in seconds, R in Ohms, C in Farads)
- ±1.0% pulse-width variation from part to part (typ.)
- Wide pulse-width range — 1 μs to ∞
- Separate latched reset inputs
- Symmetrical output sink and source capability
- Low standby current — 5 nA (typ.) @ 5 V_{DC}
- Pin compatible to CD4528B

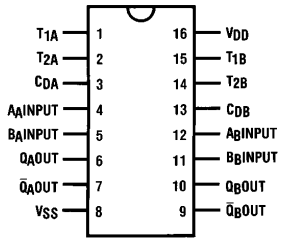
Block and Connection Diagrams



TL/F/6000–1

R_X and C_X are External Components
V_{DD} = Pin 16
V_{SS} = Pin 8

Dual-In-Line Package
CD4538BM
CD4538BC



TL/F/6000–2

Top View

Order Number CD4538B

Truth Table

Inputs			Outputs	
Clear	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⎍	⎎
H	↑	H	⎍	⎎

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⎍ = One High Level Pulse
⎎ = One Low Level Pulse
X = Irrelevant

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	-0.5 to $+18$ V_{DC}
Input Voltage (V_{IN})	$-0.5V$ to $V_{DD} + 0.5$ V_{DC}
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3 to 15 V_{DC}
Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD4538BM	$-55°C$ to $+125°C$
CD4538BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4538BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, All Outputs Open		5		0.005	5		150	μA
		$V_{DD} = 10V$, $V_{IL} = V_{SS}$, All Outputs Open		10		0.010	10		300	μA
		$V_{DD} = 15V$, $V_{IL} = V_{SS}$, All Outputs Open		20		0.015	20		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$, $\lvert I_O \rvert < 1\ \mu A$, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$, $\lvert I_O \rvert < 1\ \mu A$, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$, $\lvert I_O \rvert < 1\ \mu A$, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$, $\lvert I_O \rvert < 1\ \mu A$, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$, $\lvert I_O \rvert < 1\ \mu A$, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$, $\lvert I_O \rvert < 1\ \mu A$, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\lvert I_O \rvert < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$		3.0		4.50	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\lvert I_O \rvert < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$	7.0		7.0	5.50		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 0.4V$, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$	1.6		1.3	2.25		0.9		mA
		$V_D = 15V$, $V_O = 1.5V$, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 4.6V$, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$	-0.64		-0.51	-0.88		-0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$	-1.6		-1.3	-2.25		-0.9		mA
		$V_D = 15V$, $V_O = 13.5V$, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$	-4.2		-3.4	-8.8		-2.4		mA
I_{IN}	Input Current, Pin 2 or 14	$V_{DD} = 15V$, $V_{IN} = 0V$ or $15V$		± 0.02		$\pm 10^{-5}$	± 0.05		± 0.5	μA
I_{IN}	Input Current Other Inputs	$V_{DD} = 15V$, $V_{IN} = 0V$ or $15V$		± 0.1		$\pm 10^{-5}$	± 0.1		± 1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for acutal device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

DC Electrical Characteristics CD4538BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$ } $V_{IH} = V_{DD}$ $V_{DD} = 10V$ } $V_{IL} = V_{SS}$ $V_{DD} = 15V$ } All Outputs Open		20 40 80		0.005 0.010 0.015	20 40 80		150 300 600	μA μA μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$ } $\lvert I_O \rvert < 1\ \mu A$ $V_{DD} = 10V$ } $V_{IH} = V_{DD}, V_{IL} = V_{SS}$ $V_{DD} = 15V$		0.05 0.05 0.05		0 0 0	0.05 0.05 0.05		0.05 0.05 0.05	V V V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$ } $\lvert I_O \rvert < 1\ \mu A$ $V_{DD} = 10V$ } $V_{IH} = V_{DD}, V_{IL} = V_{SS}$ $V_{DD} = 15V$	4.95 9.95 14.95		4.95 9.95 14.95	5 10 15		4.95 9.95 14.95		V V V
V_{IL}	Low Level Input Voltage	$\lvert I_O \rvert < 1\ \mu A$ $V_{DD} = 5V, V_O = 0.5V$ or $4.5V$ $V_{DD} = 10V, V_O = 1.0V$ or $9.0V$ $V_{DD} = 15V, V_O = 1.5V$ or $13.5V$		 1.5 3.0 4.0		 2.25 4.50 6.75	 1.5 3.0 4.0		 1.5 3.0 4.0	 V V V
V_{IH}	High Level Input Voltage	$\lvert I_O \rvert < 1\ \mu A$ $V_{DD} = 5V, V_O = 0.5V$ or $4.5V$ $V_{DD} = 10V, V_O = 1.0V$ or $9.0V$ $V_{DD} = 15V, V_O = 1.5V$ or $13.5V$	 3.5 7.0 11.0		 3.5 7.0 11.0	 2.75 5.50 8.25		 3.5 7.0 11.0		 V V V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$ } $V_{IH} = V_{DD}$ $V_{DD} = 10V, V_O = 0.5V$ } $V_{IL} = V_{SS}$ $V_D = 15V, V_O = 1.5V$	0.52 1.3 3.6		0.44 1.1 3.0	0.88 2.25 8.8		0.36 0.9 2.4		mA mA mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$ } $V_{DD} = 10V, V_O = 9.5V$ } $V_{IL} = V_{SS}$ $V_D = 15V, V_O = 13.5V$	−0.52 −1.3 −3.6		−0.44 −1.1 −3.0	−0.88 −2.25 −8.8		−0.36 −0.9 −2.4		mA mA mA
I_{IN}	Input Current, Pin 2 or 14	$V_{DD} = 15V, V_{IN} = 0V$ or $15V$		±0.02		$\pm 10^{-5}$	±0.05		±0.5	μA
I_{IN}	Input Current Other Inputs	$V_{DD} = 15V, V_{IN} = 0V$ or $15V$		±0.3		$\pm 10^{-5}$	±0.3		±1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for acutal device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, and $t_r = t_f = 20$ ns unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{TLH}, t_{THL}	Output Transition Time	$V_{DD} = 5V$			100	200	ns
		$V_{DD} = 10V$			50	100	ns
		$V_{DD} = 15V$			40	80	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Trigger Operation— A or B to Q or $\overline{Q}$					
		$V_{DD} = 5V$			300	600	ns
		$V_{DD} = 10V$			150	300	ns
		$V_{DD} = 15V$			100	220	ns
		Reset Operation— C_D to Q or $\overline{Q}$					
		$V_{DD} = 5V$			250	500	ns
		$V_{DD} = 10V$			125	250	ns
		$V_{DD} = 15V$			95	190	ns
t_{WL}, t_{WH}	Minimum Input Pulse Width A, B, or C_D	$V_{DD} = 5V$			35	70	ns
		$V_{DD} = 10V$			30	60	ns
		$V_{DD} = 15V$			25	50	ns
t_{RR}	Minimum Retrigger Time	$V_{DD} = 5V$				0	ns
		$V_{DD} = 10V$			0	0	ns
		$V_{DD} = 15V$				0	ns
C_{IN}	Input Capacitance	Pin 2 or 14			10		pF
		Other Inputs			5	7.5	pF
PW_{OUT}	Output Pulse Width (Q or $\overline{Q}$) (**Note:** For Typical Distribution, see *Figure 9*)	$R_X = 100$ kΩ, $C_X = 0.002$ μF	$V_{DD} = 5V$	208	226	244	μs
			$V_{DD} = 10V$	211	230	248	μs
			$V_{DD} = 15V$	216	235	254	μs
		$R_X = 100$ kΩ, $C_X = 0.1$ μF	$V_{DD} = 5V$	8.83	9.60	10.37	ms
			$V_{DD} = 10V$	9.02	9.80	10.59	ms
			$V_{DD} = 15V$	9.20	10.00	10.80	ms
		$R_X = 100$ kΩ, $C_X = 10.0$ μF	$V_{DD} = 5V$	0.87	0.95	1.03	s
			$V_{DD} = 10V$	0.89	0.97	1.05	s
			$V_{DD} = 15V$	0.91	0.99	1.07	s
Pulse Width Match between Circuits in the Same Package $C_X = 0.1$ μF, $R_X = 100$ kΩ		$R_X = 100$ kΩ, $C_X = 0.1$ μF	$V_{DD} = 5V$		±1		%
			$V_{DD} = 10V$		±1		%
			$V_{DD} = 15V$		±1		%
Operating Conditions							
R_X	External Timing Resistance			5.0		**	kΩ
C_X	External Timing Capacitance			0		No Limit	pF

*AC parameters are guaranteed by DC correlated testing.

**The maximum usable resistance R_X is a function of the leakage of the Capacitor C_X, leakage of the CD4538B, and leakage due to board layout, surface resistance, etc.

Logic Diagram

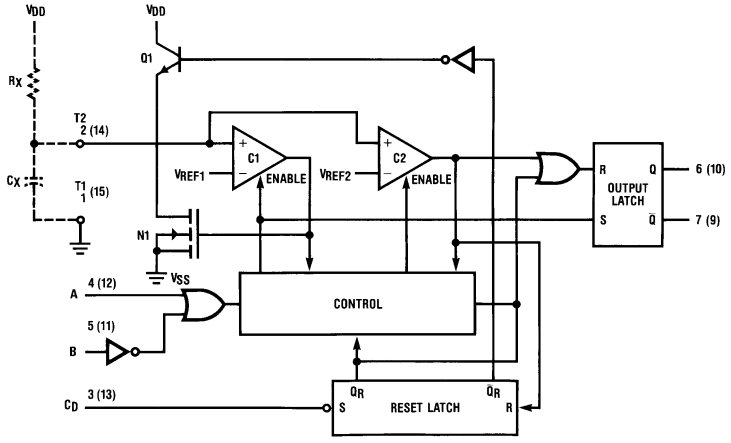


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FIGURE 1

Theory of Operation

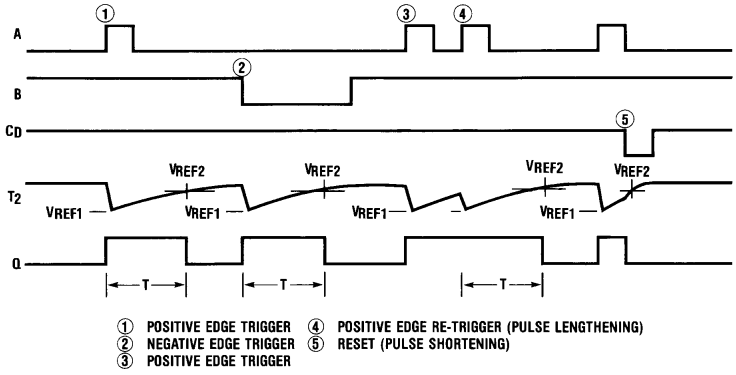

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FIGURE 2

Trigger Operation

The block diagram of the CD4538B is shown in *Figure 1*, with circuit operation following.

As shown in *Figures 1* and *2*, before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor C_X completely charged to V_{DD}. When the trigger input A goes from V_{SS} to V_{DD} (while inputs B and C_D are held to V_{DD}) a valid trigger is recognized, which turns on comparator C1 and N-Channel transistor N1①. At the same time the output latch is set. With transistor N1 on, the capacitor C_X rapidly discharges toward V_{SS} until V_{REF1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_X begins to charge through the timing resistor, R_X, toward V_{DD}. When the voltage across C_X equals V_{REF2}, comparator C2 changes state causing the output latch to reset (Q goes low) while at the same time disabling comparator C2. This ends the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

A valid trigger is also recognized when trigger input B goes from V_{DD} to V_{SS} (while input A is at V_{SS} and input C_D is at V_{DD})②.

It should be noted that in the quiescent state C_X is fully charged to V_{DD}, causing the current through resistor R_X to be zero. Both comparators are ''off'' with the total device current due only to reverse junction leakages. An added feature of the CD4538B is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_X, R_X, or the duty cycle of the input waveform.

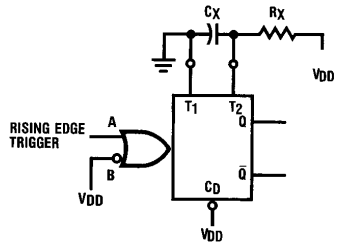
Retrigger Operation

The CD4538B is retriggered if a valid trigger occurs③ followed by another valid trigger④ before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from V_{REF1}, but has not yet reached V_{REF2}, will cause an increase in output pulse width T. When a valid retrigger is initiated④, the voltage at T2 will again drop to V_{REF1} before progressing along the RC charging curve toward V_{DD}. The Q output will remain high until time T, after the last valid retrigger.

Reset Operation

The CD4538B may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on C_D sets the reset latch and causes the capacitor to be fast charged to V_{DD} by turning on transistor Q1⑤. When the voltage on the capacitor reaches V_{REF2}, the reset latch will clear and then be ready to accept another pulse. If the C_D input is held low, any trigger inputs that occur will be inhibited and the Q and $\overline{Q}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the C_D input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

Typical Applications



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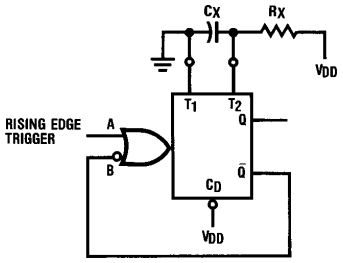
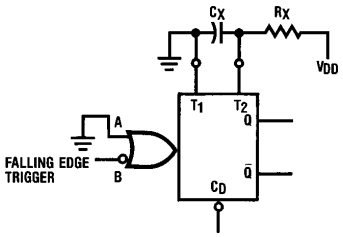


TL/F/6000–6



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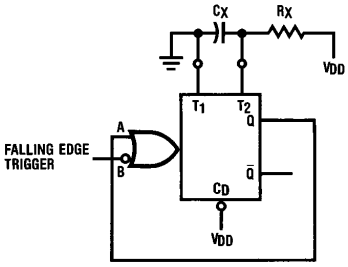

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FIGURE 3. Retriggerable Monostables Circuitry

FIGURE 4. Non-Retriggerable Monostables Circuitry

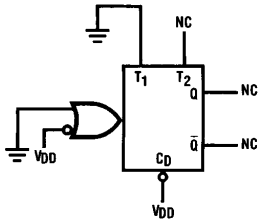

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FIGURE 5. Connection of Unused Sections

Typical Applications (Continued)

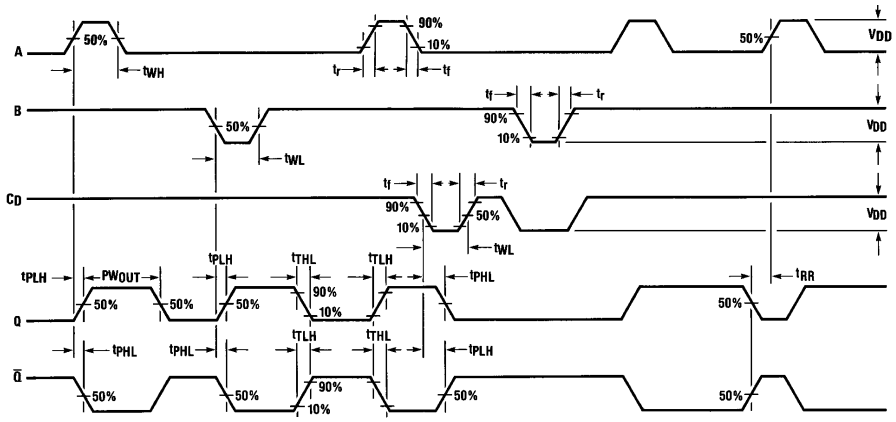

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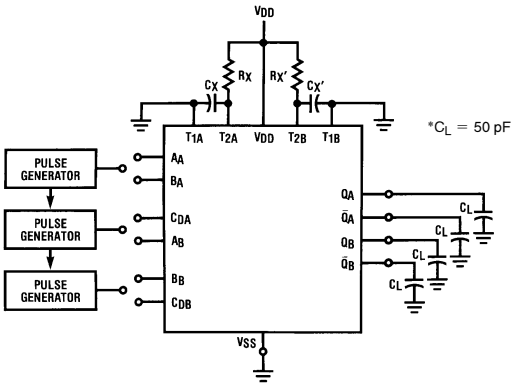
FIGURE 6. Switching Test Waveforms



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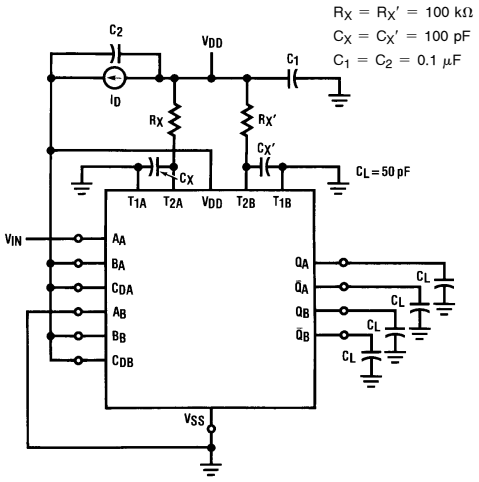

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Input Connections

Characteristics	CD	A	B
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL} PW_{OUT}, t_{WH}, t_{WL}	V_{DD}	PG1	V_{DD}
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL} PW_{OUT}, t_{WH}, t_{WL}	V_{DD}	V_{SS}	PG2
$t_{PLH(R)}$, $t_{PHL(R)}$, t_{WH}, t_{WL}	PG3	PG1	PG2

*Includes capacitance of probes, wiring, and fixture parasitic

Note: Switching test waveforms for PG1, PG2, PG3 are shown in *Figure 6*.

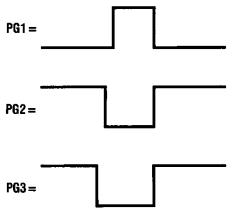

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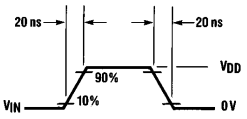
FIGURE 7. Switching Test Circuit



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Duty Cycle = 50%

FIGURE 8. Power Dissipation Test Circuit and Waveforms

Typical Applications (Continued)

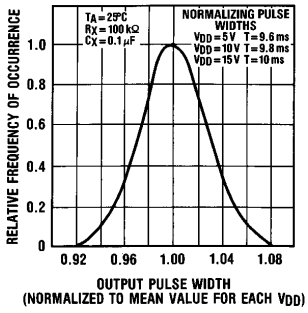

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FIGURE 9. Typical Normalized Distribution of Units for Output Pulse Width

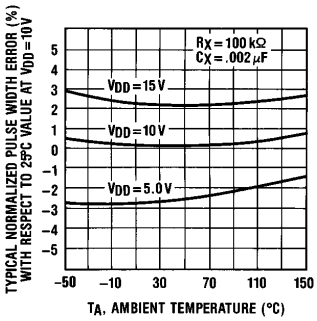

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FIGURE 12. Typical Pulse Width Error Versus Temperature

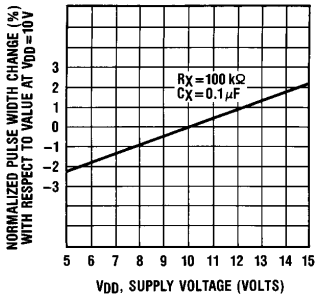

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FIGURE 10. Typical Pulse Width Variation as a Function of Supply Voltage V_{DD}

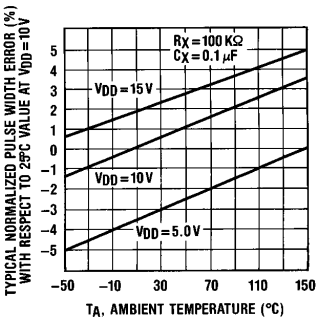

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FIGURE 13. Typical Pulse Width Error Versus Temperature

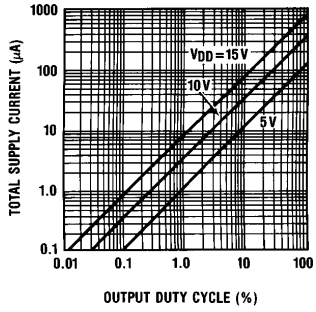

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FIGURE 11. Typical Total Supply Current Versus Output Duty Cycle, $R_X = 100\ k\Omega$, $C_L = 50\ pF$, $C_X = 100\ pF$, One Monostable Switching Only

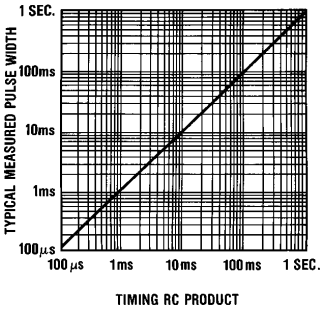

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FIGURE 14. Typical Pulse Width Versus Timing RC Product

National Semiconductor

February 1988

CD40106BM/CD40106BC Hex Schmitt Trigger

General Description

The CD40106B Hex Schmitt Trigger is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. The positive and negative-going threshold voltages, V_{T+} and V_{T-}, show low variation with respect to temperature (typ 0.0005V/°C at $V_{DD} = 10V$), and hysteresis, $V_{T+} - V_{T-} \geq 0.2\ V_{DD}$ is guaranteed.

All inputs are protected from damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

Features

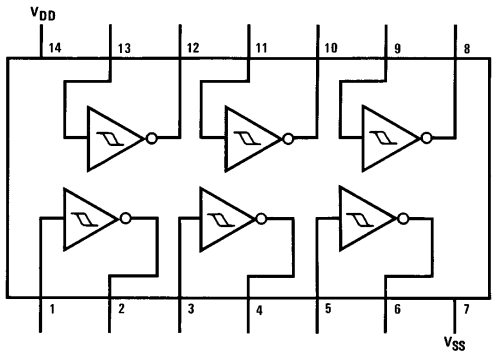
■ Wide supply voltage range	3V to 15V
■ High noise immunity	0.7 V_{DD} (typ.)
■ Low power TTL compatibility	Fan out of 2 driving 74L or 1 driving 74LS
■ Hysteresis	0.4 V_{DD} (typ.) 0.2 V_{DD} guaranteed

■ Equivalent to MM54C14/MM74C14

■ Equivalent to MC14584B

Connection Diagram

Dual-In-Line Package



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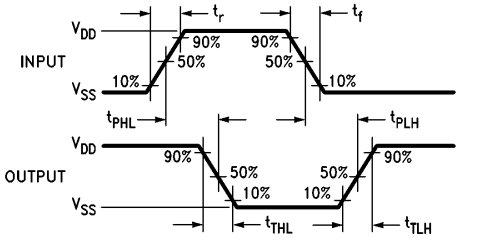
Top View

Switching Time Waveforms

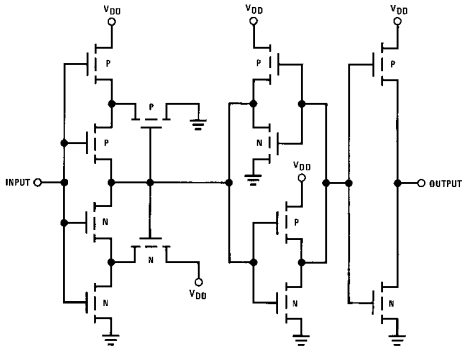


TL/F/5985–3

$t_r = t_f = 20$ ns

Order Number CD40106B

Schematic Diagram



TL/F/5985–1

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	-0.5 to $+18$ V_{DC}
Input Voltage (V_{IN})	-0.5 to V_{DD} $+0.5$ V_{DC}
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3 to 15 V_{DC}
Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD40106BM	$-55°C$ to $+125°C$
CD40106BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD40106BM (Note 2)

Symbol	Parameter	Conditions	$-55°C$		$+25°C$			$+125°C$		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$, $V_{IN} = V_{DD}$ or V_{SS}		1.0			1.0		30	μA
		$V_{DD} = 10V$, $V_{IN} = V_{DD}$ or V_{SS}		2.0			2.0		60	μA
		$V_{DD} = 15V$, $V_{IN} = V_{DD}$ or V_{SS}		4.0			4.0		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$		0.05			0.05		0.05	V
		$V_{DD} = 10V$		0.05			0.05		0.05	V
		$V_{DD} = 15V$		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		0.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{T-}	Negative-Going Threshold Voltage	$V_{DD} = 5V$, $V_O = 4.5V$	0.7	2.0	0.7	1.4	2.0	0.7	2.0	V
		$V_{DD} = 10V$, $V_O = 9V$	1.4	4.0	1.4	3.2	4.0	1.4	4.0	V
		$V_{DD} = 15V$, $V_O = 13.5V$	2.1	6.0	2.1	5.0	6.0	2.1	6.0	V
V_{T+}	Positive-Going Threshold Voltage	$V_{DD} = 5V$, $V_O = 0.5V$	3.0	4.3	3.0	3.6	4.3	3.0	4.3	V
		$V_{DD} = 10V$, $V_O = 1V$	6.0	8.6	6.0	6.8	8.6	6.0	8.6	V
		$V_{DD} = 15V$, $V_O = 1.5V$	9.0	12.9	9.0	10.0	12.9	9.0	12.9	V
V_H	Hysteresis ($V_{T+} - V_{T-}$)	$V_{DD} = 5V$	1.0	3.6	1.0	2.2	3.6	1.0	3.6	V
		$V_{DD} = 10V$	2.0	7.2	2.0	3.6	7.2	2.0	7.2	V
		$V_{DD} = 15V$	3.0	10.8	3.0	5.0	10.8	3.0	10.8	V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 4.6V$	-0.64		-0.51	-0.88		-0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	-1.6		-1.3	-2.25		-0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	-4.2		-3.4	-8.8		-2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		-0.10		-10^{-5}	-0.10		-1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.10		10^{-5}	0.10		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

DC Electrical Characteristics CD40106BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		4.0			4.0		30	μA
		$V_{DD} = 10V$		8.0			8.0		60	μA
		$V_{DD} = 15V$		16.0			16.0		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$		0.05			0.05		0.05	V
		$V_{DD} = 10V$		0.05			0.05		0.05	V
		$V_{DD} = 15V$		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		0.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{T-}	Negative-Going Threshold Voltage	$V_{DD} = 5V, V_O = 4.5V$	0.7	2.0	0.7	1.4	2.0	0.7	2.0	V
		$V_{DD} = 10V, V_O = 9V$	1.4	4.0	1.4	3.2	4.0	1.4	4.0	V
		$V_{DD} = 15V, V_O = 13.5V$	2.1	6.0	2.1	5.0	6.0	2.1	6.0	V
V_{T+}	Positive-Going Threshold Voltage	$V_{DD} = 5V, V_O = 0.5V$	3.0	4.3	3.0	3.6	4.3	3.0	4.3	V
		$V_{DD} = 10V, V_O = 1V$	6.0	8.6	6.0	6.8	8.6	6.0	8.6	V
		$V_{DD} = 15V, V_O = 1.5V$	9.0	12.9	9.0	10.0	12.9	9.0	12.9	V
V_H	Hysteresis ($V_{T+} - V_{T-}$) Voltage	$V_{DD} = 5V$	1.0	3.6	1.0	2.2	3.6	1.0	3.6	V
		$V_{DD} = 10V$	2.0	7.2	2.0	3.6	7.2	2.0	7.2	V
		$V_{DD} = 15V$	3.0	10.8	3.0	5.0	10.8	3.0	10.8	V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	−1.3		−1.1	−2.25		−0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		−0.30		-10^{-5}	−0.30		−1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics*

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, t_r and $t_f = 20$ ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL} or t_{PLH}	Propagation Delay Time from Input to Output	$V_{DD} = 5V$		220	400	ns
		$V_{DD} = 10V$		80	200	ns
		$V_{DD} = 15V$		70	160	ns
t_{THL} or t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate (Note 4)		14		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

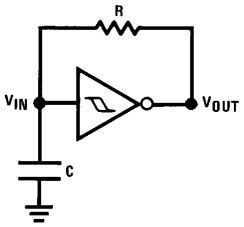
Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note, AN-90.

Typical Applications

Low Power Oscillator



$$t_1 \approx RC \ell n \frac{V_{T+}}{V_{T-}}$$

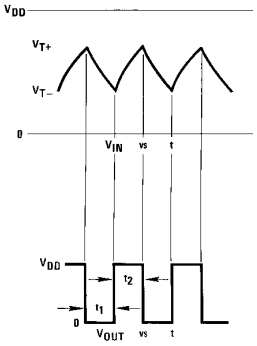
$$t_2 \approx RC \ell n \frac{V_{DD} - V_{T-}}{V_{DD} - V_{T+}}$$

$$f \approx \frac{1}{RC \ell n \frac{V_{T+}(V_{DD} - V_{T-})}{V_{T-}(V_{DD} - V_{T+})}}$$

Note: The equations assume

$t_1 + t_2 >> t_{PHL} + t_{PLH}$

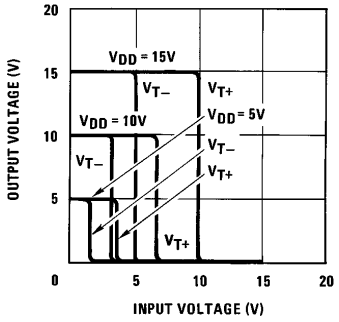
TL/F/5985–4



TL/F/5985–5

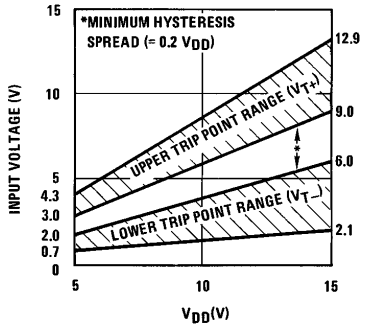
Typical Performance Characteristics

Typical Transfer Characteristics

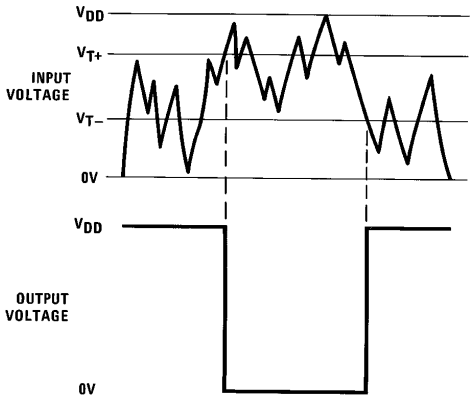


TL/F/5985–6

Guaranteed Trip Point Range



TL/F/5985–7



TL/F/5985–8

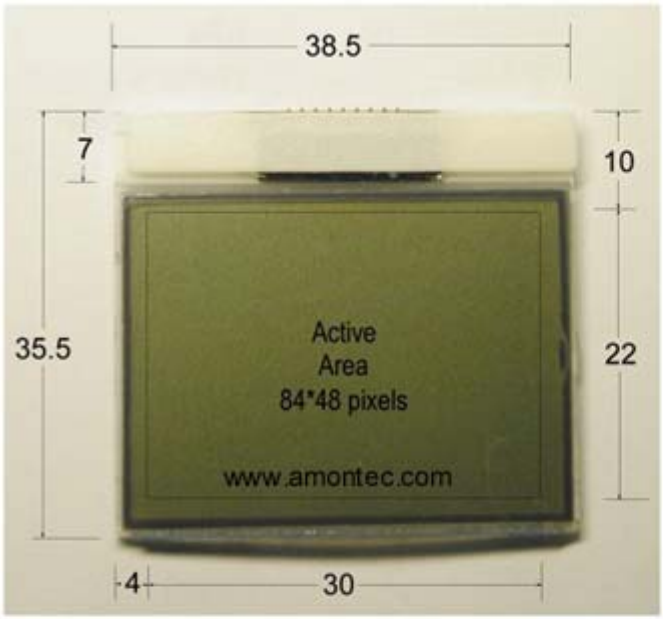
lcd_controller_pcd8544.pdf

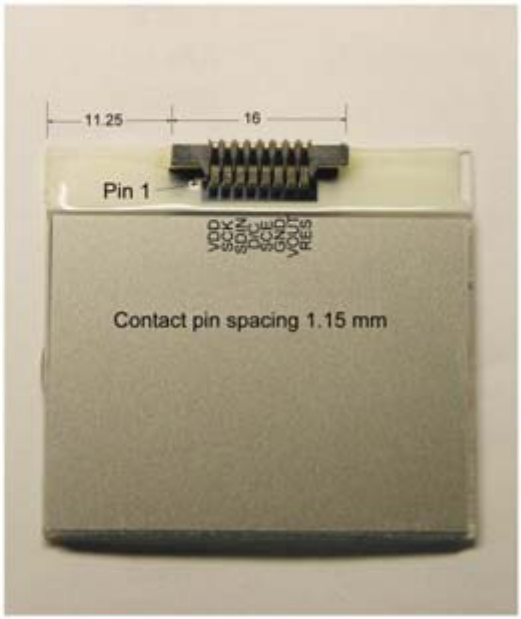
Features

The Nokia 3310 LCD is a nice small graphical LCD, suitable for a lot of various projects.
The display is 38*35 mm, with an active display surface of 30*22 mm, and a 84*48 pixel resolution.
The display is easy to interface, using standard SPI communication. A 1-10 uF electrolytic capacitor from VOUT to GND, is the only external component needed.

- Logic supply voltage range VDD to VSS : 2.7 to 3.3 V
- Low power consumption, suitable for battery operated systems
- Temperature range: -25 to +70 °C

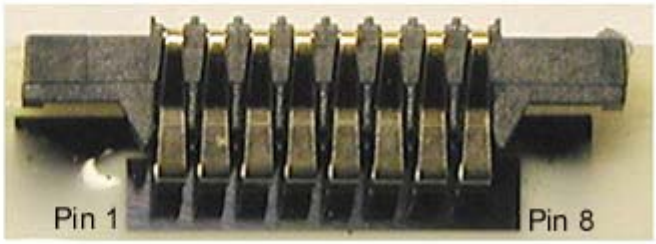
Mechanical specification





Nokia 3310 LCD
84x48 pixels
with Philips PCD8544 Controller

on Amontec Online Shop
www.amontec.com



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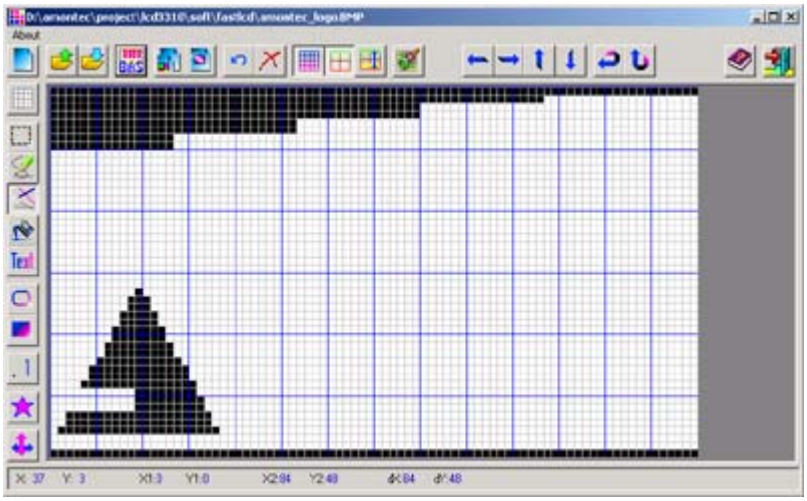
Electrical Interface specification

Pin	Signal	Description	Port
1	VDD	Power Input. Logic supply voltage range VDD to GND : 2.7 to 3.3 V	Power
2	SCLK	Serial clock. Input for the clock signal: 0.0 to 4.0 Mbits/s.	Input
3	SDIN	Serial data. Input for the data line.	Input
4	D/C	Mode Select. To select either command/address or data input.	Input
5	SCE	Chip enable input. The enable pin allows data to be clocked in. The signal is active LOW.	Input
6	GND	Ground	Power
7	VOUT	Ouptut voltage. **Add external 1-10 uF electrolytic capacitor from VOUT to GND**	Power
8	RES	External reset. This signal will reset the device and must be applied to properly initialize the chip. The signal is active LOW.	Input

FastLCD for Creating Bitmap pictures

You can download FastLCD



National Semiconductor

December 2001

LF155/LF156/LF256/LF257/LF355/LF356/LF357 JFET Input Operational Amplifiers

General Description

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BI-FET™ Technology). These amplifiers feature low input bias and offset currents/low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

Features

Advantages

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance — very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (5,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

Applications

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

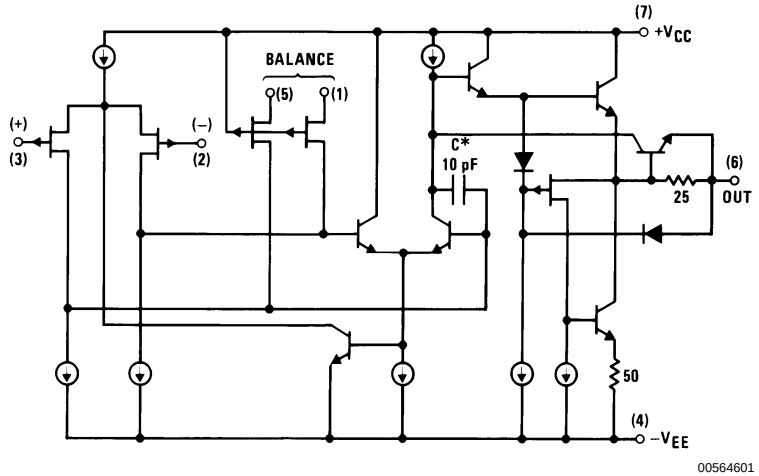
Common Features

- Low input bias current: 30pA
- Low Input Offset Current: 3pA
- High input impedance: $10^{12}\Omega$
- Low input noise current: $0.01\ pA/\sqrt{Hz}$
- High common-mode rejection ratio: 100 dB
- Large dc voltage gain: 106 dB

Uncommon Features

	LF155/ LF355	LF156/ LF256/ LF356	LF257/ LF357 (A_V=5)	Units
■ Extremely fast settling time to 0.01%	4	1.5	1.5	µs
■ Fast slew rate	5	12	50	V/µs
■ Wide gain bandwidth	2.5	5	20	MHz
■ Low input noise voltage	20	12	12	$nV/\sqrt{Hz}$

Simplified Schematic



00564601

*3pF in LF357 series.

BI-FET™, BI-FET II™ are trademarks of National Semiconductor Corporation.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LF155/6	LF256/7/LF356B	LF355/6/7
Supply Voltage	±22V	±22V	±18V
Differential Input Voltage	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±16V
Output Short Circuit Duration	Continuous	Continuous	Continuous
T_{JMAX}			
H-Package	150˚C	115˚C	115˚C
N-Package		100˚C	100˚C
M-Package		100˚C	100˚C
Power Dissipation at T_A = 25˚C (Notes 1, 8)			
H-Package (Still Air)	560 mW	400 mW	400 mW
H-Package (400 LF/Min Air Flow)	1200 mW	1000 mW	1000 mW
N-Package		670 mW	670 mW
M-Package		380 mW	380 mW
Thermal Resistance (Typical) θ_{JA}			
H-Package (Still Air)	160˚C/W	160˚C/W	160˚C/W
H-Package (400 LF/Min Air Flow)	65˚C/W	65˚C/W	65˚C/W
N-Package		130˚C/W	130˚C/W
M-Package		195˚C/W	195˚C/W
(Typical) θ_{JC}			
H-Package	23˚C/W	23˚C/W	23˚C/W
Storage Temperature Range	−65˚C to +150˚C	−65˚C to +150˚C	−65˚C to +150˚C
Soldering Information (Lead Temp.)			
Metal Can Package			
Soldering (10 sec.)	300˚C	300˚C	300˚C
Dual-In-Line Package			
Soldering (10 sec.)	260˚C	260˚C	260˚C
Small Outline Package			
Vapor Phase (60 sec.)		215˚C	215˚C
Infrared (15 sec.)		220˚C	220˚C
See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.			
ESD tolerance			
(100 pF discharged through 1.5kΩ)	1000V	1000V	1000V

DC Electrical Characteristics

(Note 3)

Symbol	Parameter	Conditions	LF155/6			LF256/7 LF356B			LF355/6/7			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S=50Ω, T_A=25˚C		3	5		3	5		3	10	mV
		Over Temperature			7			6.5			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=50Ω		5			5			5		µV/˚C
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	R_S=50Ω, (Note 4)		0.5			0.5			0.5		µV/˚C per mV
I_{OS}	Input Offset Current	T_J=25˚C, (Notes 3, 5)		3	20		3	20		3	50	pA
		$T_J \leq T_{HIGH}$			20			1			2	nA

DC Electrical Characteristics (Continued)

(Note 3)

Symbol	Parameter	Conditions	LF155/6			LF256/7 LF356B			LF355/6/7			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_B	Input Bias Current	T_J=25˚C, (Notes 3, 5)		30	100		30	100		30	200	pA
		$T_J \leq T_{HIGH}$			50			5			8	nA
R_{IN}	Input Resistance	T_J=25˚C		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, T_A=25˚C	50	200		50	200		25	200		V/mV
		V_O=±10V, R_L=2k										
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10k	±12	±13		±12	±13		±12	±13		V
		V_S=±15V, R_L=2k	±10	±12		±10	±12		±10	±12		V
V_{CM}	Input Common-Mode Voltage Range	V_S=±15V	±11	+15.1 −12		±11	±15.1 −12		+10	+15.1 −12		V V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		80	100		dB

DC Electrical Characteristics

$T_A = T_J = 25˚C$, $V_S = ±15V$

Parameter	LF155		LF355		LF156/256/257/356B		LF356		LF357		Units
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Supply Current	2	4	2	4	5	7	5	10	5	10	mA

AC Electrical Characteristics

$T_A = T_J = 25˚C$, $V_S = ±15V$

Symbol	Parameter	Conditions	LF155/355	LF156/256/ 356B	LF156/256/356/ LF356B	LF257/357	Units
			Typ	Min	Typ	Typ	
SR	Slew Rate	LF155/6: A_V=1,	5	7.5	12		V/µs
		LF357: A_V=5				50	V/µs
GBW	Gain Bandwidth Product		2.5		5	20	MHz
t_s	Settling Time to 0.01%	(Note 7)	4		1.5	1.5	µs
e_n	Equivalent Input Noise Voltage	R_S=100Ω					
		f=100 Hz	25		15	15	$nV/\sqrt{Hz}$
		f=1000 Hz	20		12	12	$nV/\sqrt{Hz}$
i_n	Equivalent Input Current Noise	f=100 Hz	0.01		0.01	0.01	$pA/\sqrt{Hz}$
		f=1000 Hz	0.01		0.01	0.01	$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance		3		3	3	pF

Notes for Electrical Characteristics

Note 1: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_D=(T_{JMAX}-T_A)/\theta_{JA}$ or the 25˚C P_{dMAX}, whichever is less.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: Unless otherwise stated, these test conditions apply:

Notes for Electrical Characteristics (Continued)

	LF155/156	LF256/257	LF356B	LF355/6/7
Supply Voltage, V_S	$\pm 15V \le V_S \le \pm 20V$	$\pm 15V \le V_S \le \pm 20V$	$\pm 15V \le V_S \pm 20V$	$V_S = \pm 15V$
T_A	$-55^\circ C \le T_A \le +125^\circ C$	$-25^\circ C \le T_A \le +85^\circ C$	$0^\circ C \le T_A \le +70^\circ C$	$0^\circ C \le T_A \le +70^\circ C$
T_{HIGH}	$+125^\circ C$	$+85^\circ C$	$+70^\circ C$	$+70^\circ C$

and V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

Note 4: The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5µV/˚C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10˚C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + \theta_{JA}$ Pd where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

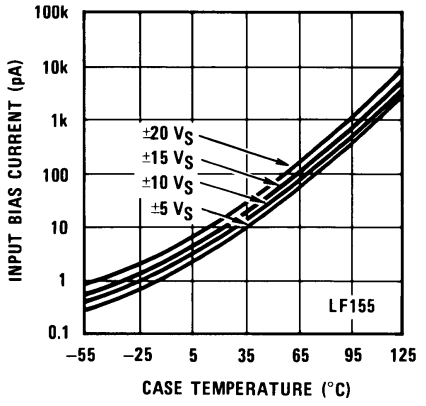
Note 7: Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF357, $A_V = -5$, the feedback resistor from output to input is 2kΩ and the output step is 10V (See Settling Time Test Circuit).

Note 8: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Typical DC Performance Characteristics

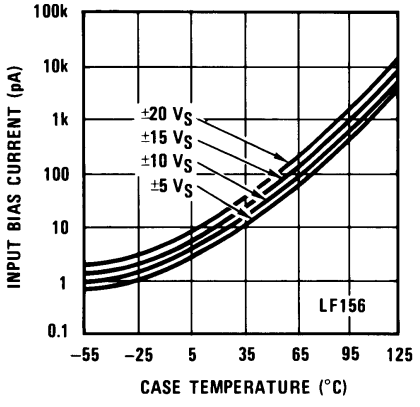
Curves are for LF155 and LF156 unless otherwise specified.

Input Bias Current



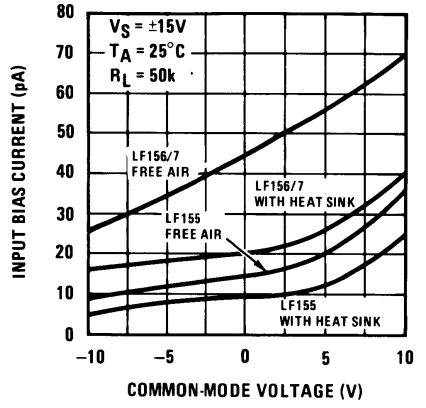
00564637

Input Bias Current



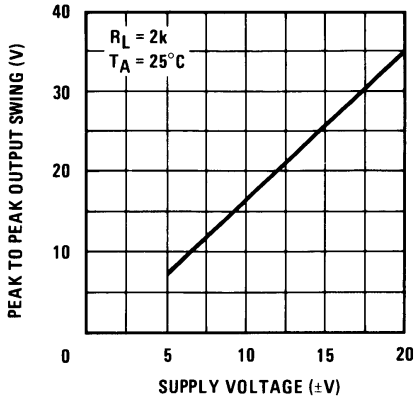
00564638

Input Bias Current



00564639

Voltage Swing

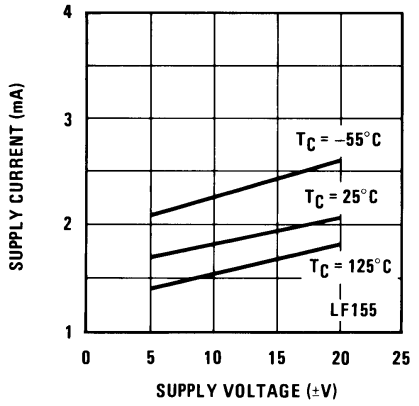


00564640

Typical DC Performance Characteristics

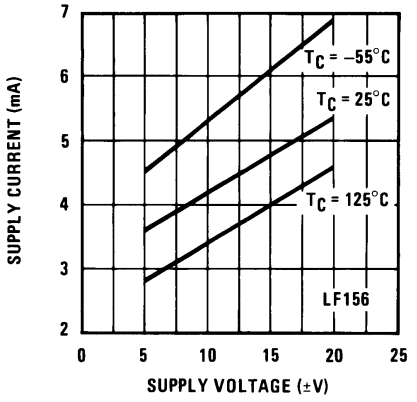
Curves are for LF155 and LF156 unless otherwise specified. (Continued)

Supply Current



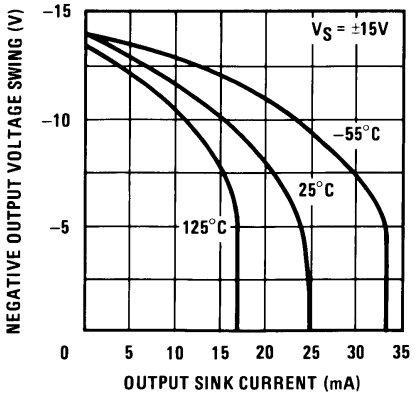
00564641

Supply Current



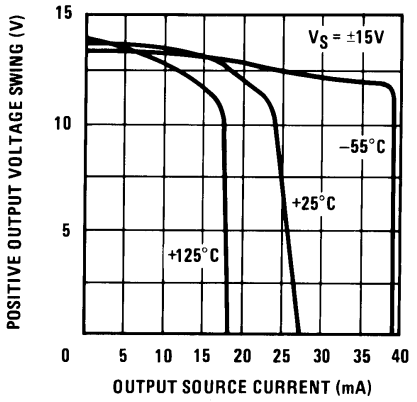
00564642

Negative Current Limit



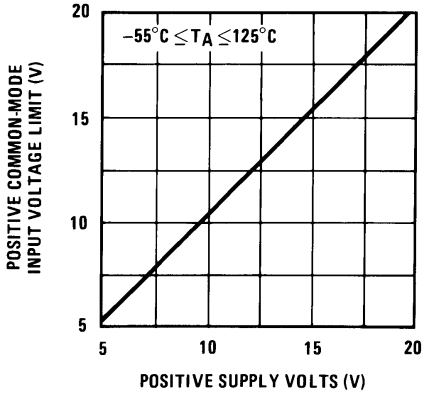
00564643

Positive Current Limit



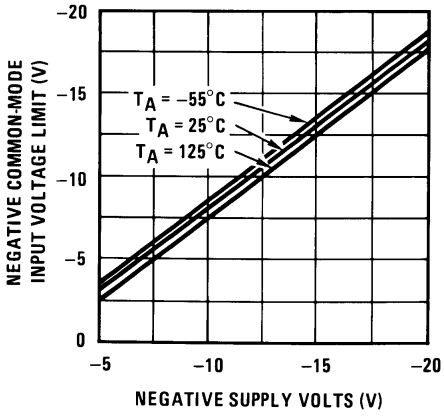
00564644

Positive Common-Mode Input Voltage Limit



00564645

Negative Common-Mode Input Voltage Limit

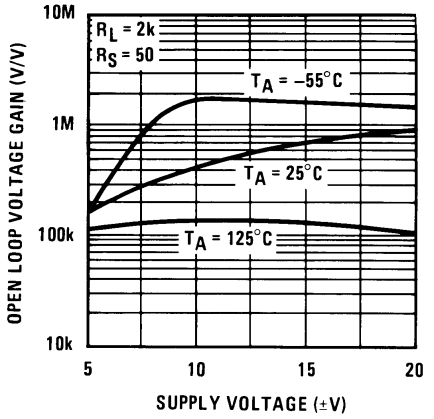


00564646

Typical DC Performance Characteristics

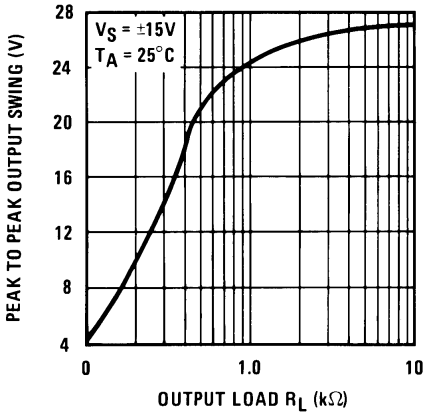
Curves are for LF155 and LF156 unless otherwise specified. (Continued)

Open Loop Voltage Gain



00564647

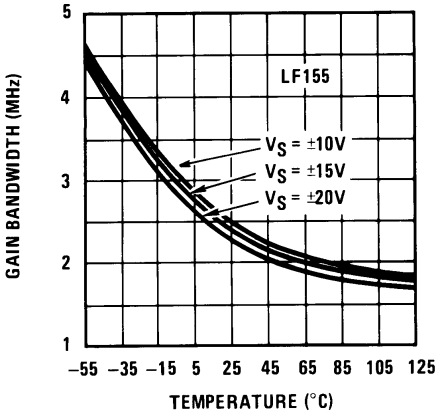
Output Voltage Swing



00564648

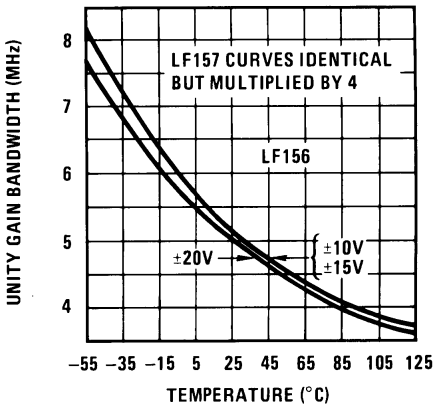
Typical AC Performance Characteristics

Gain Bandwidth



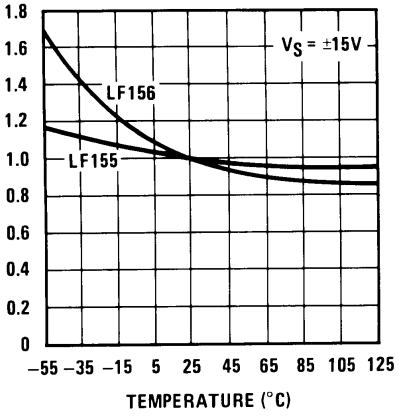
00564649

Gain Bandwidth



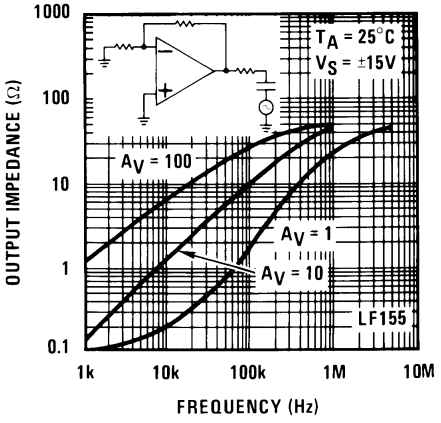
00564650

Normalized Slew Rate



00564651

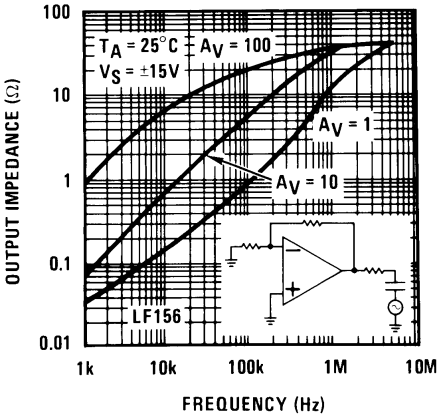
Output Impedance



00564652

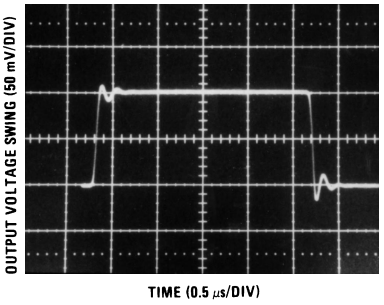
Typical AC Performance Characteristics (Continued)

Output Impedance



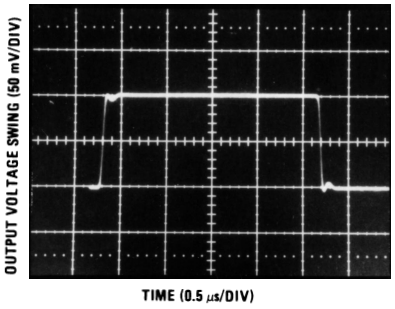
00564653

LF155 Small Signal Pulse Response, A_V = +1



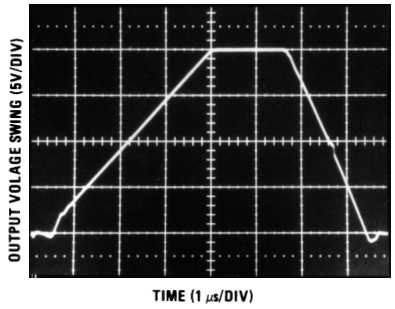
00564605

LF156 Small Signal Pulse Response, A_V = +1



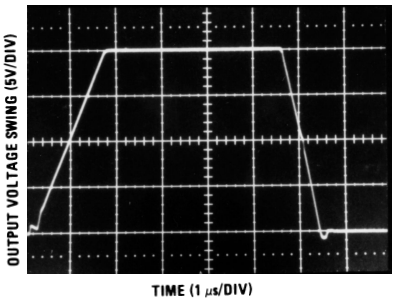
00564606

LF155 Large Signal Pulse Response, A_V = +1



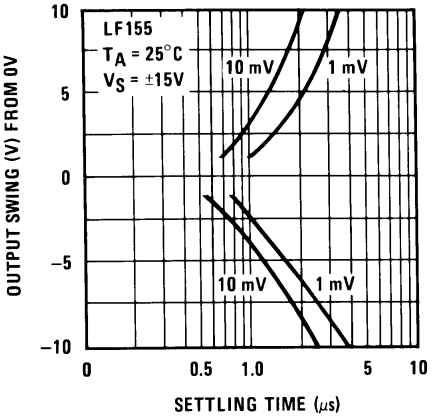
00564608

LF156 Large Signal Puls Response, A_V = +1



00564609

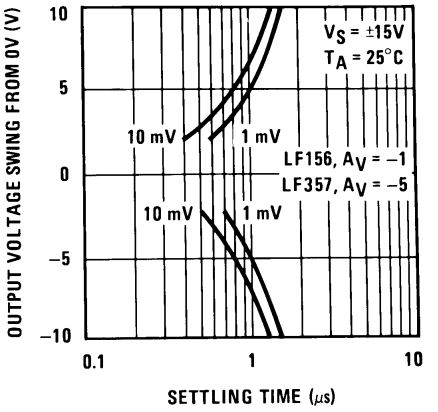
Inverter Settling Time



00564655

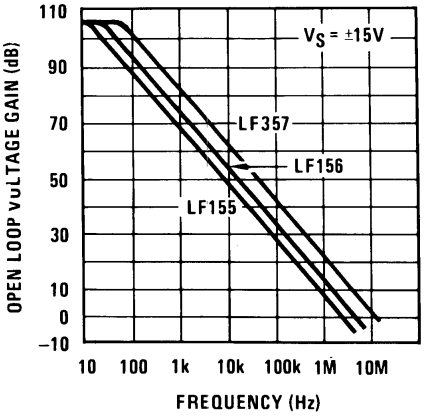
Typical AC Performance Characteristics (Continued)

Inverter Settling Time



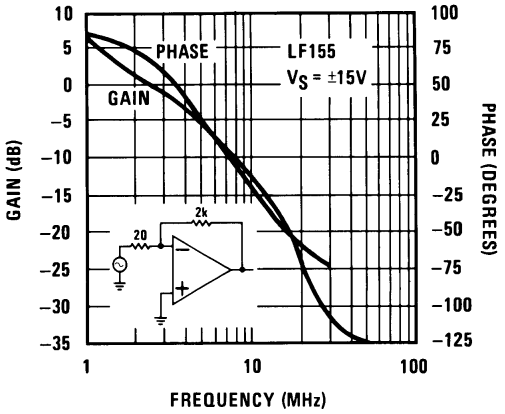
00564656

Open Loop Frequency Response



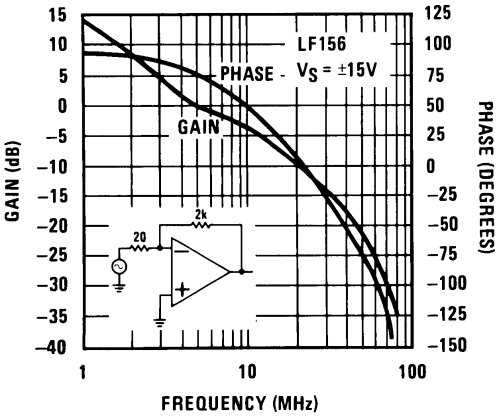
00564657

Bode Plot



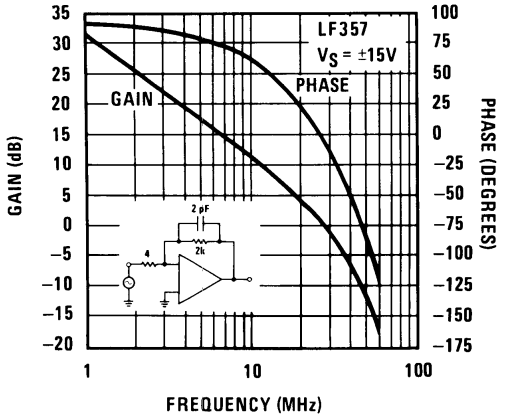
00564658

Bode Plot



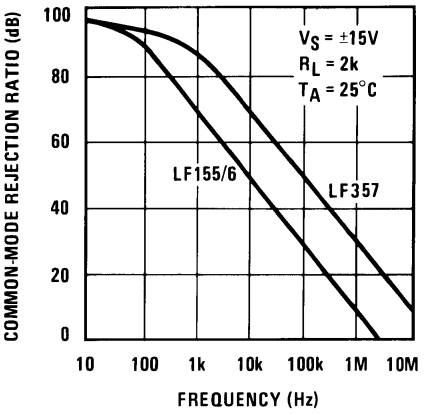
00564659

Bode Plot



00564660

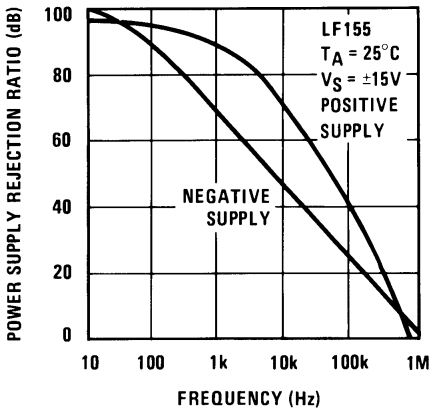
Common-Mode Rejection Ratio



00564661

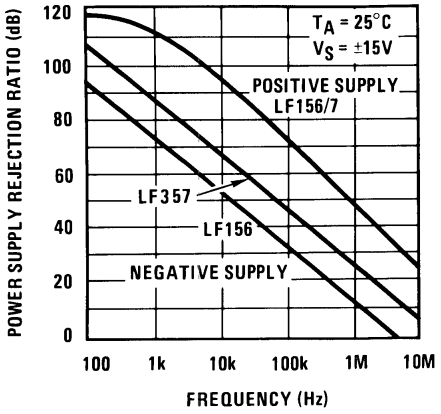
Typical AC Performance Characteristics (Continued)

Power Supply Rejection Ratio



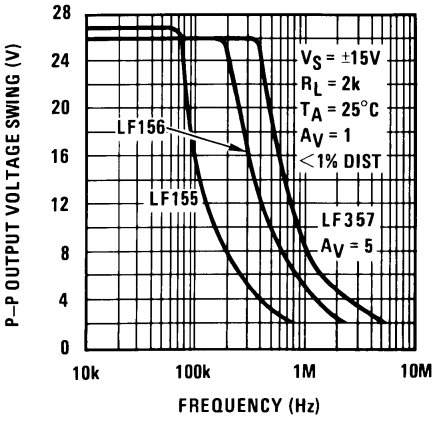
00564662

Power Supply Rejection Ratio



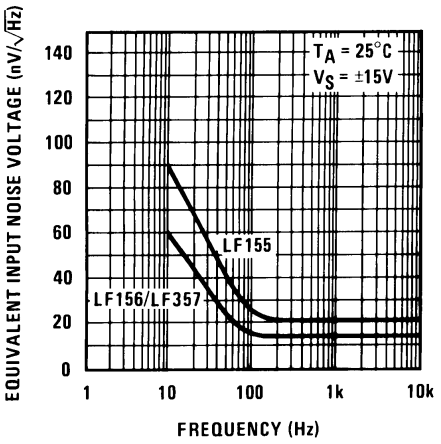
00564663

Undistorted Output Voltage Swing



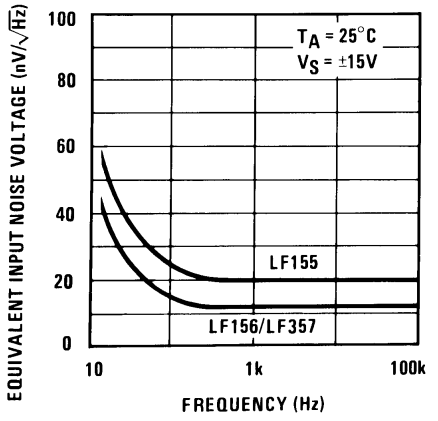
00564664

Equivalent Input Noise Voltage



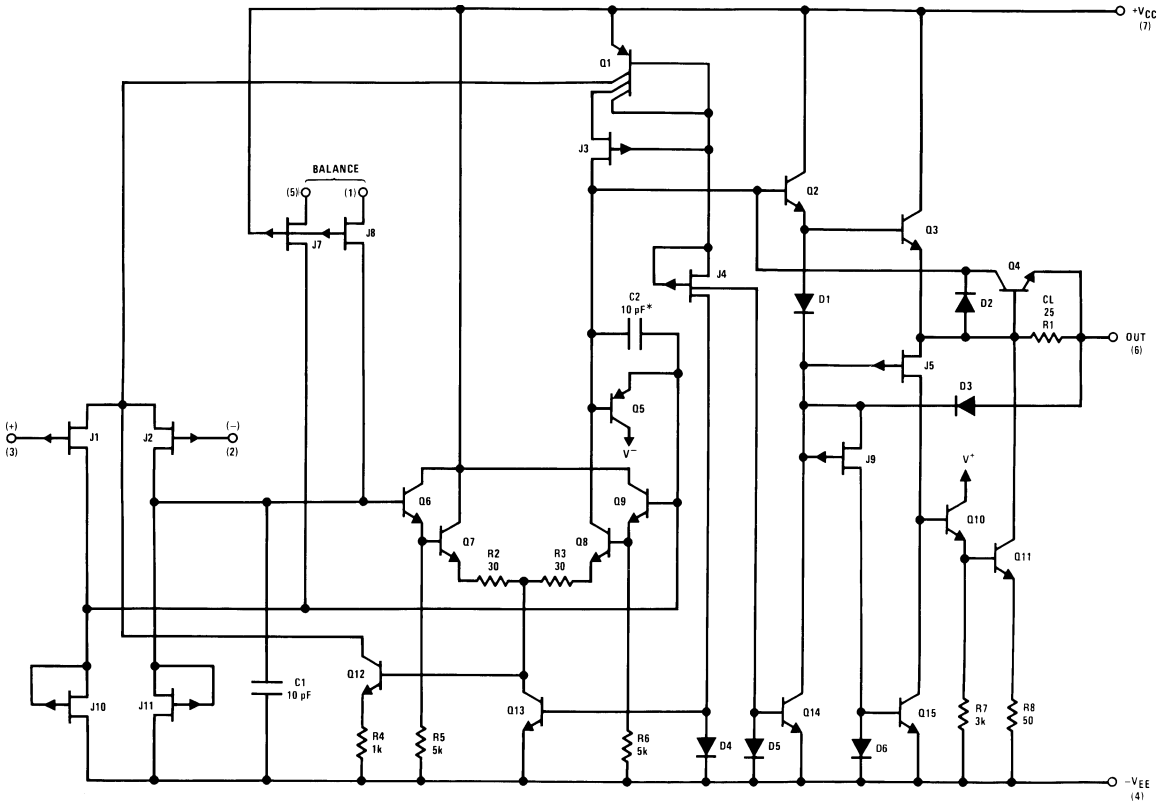
00564665

Equivalent Input Noise Voltage (Expanded Scale)



00564666

Detailed Schematic

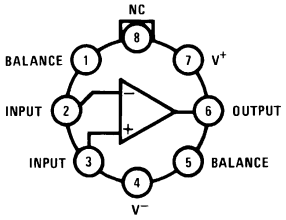


00564613

*C = 3pF in LF357 series.

Connection Diagrams (Top Views)

Metal Can Package (H)

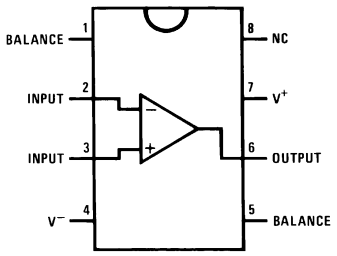


00564614

Order Number LF155H, LF156H, LF256H, LF257H, LF356BH, LF356H, or LF357H
See NS Package Number H08C

*Available per JM38510/11401 or JM38510/11402

Dual-In-Line Package (M and N)



00564629

Order Number LF356M, LF356MX, LF355N, or LF356N
See NS Package Number M08A or N08E

Application Hints

These are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a

Application Hints (Continued)

reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

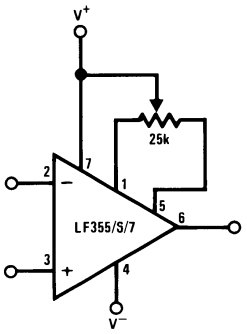
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pickup” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Circuit Connections

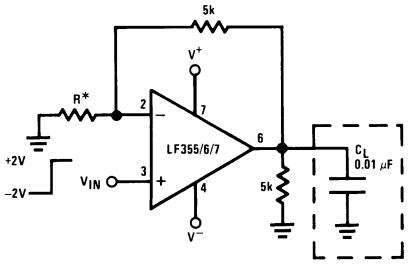
V_{OS} Adjustment



00564667

- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V^+
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5µV/°C/mV of adjustment
- Typical overall drift: 5µV/°C ±(0.5µV/°C/mV of adj.)

Driving Capacitive Loads



00564668

* LF155/6 R = 5k

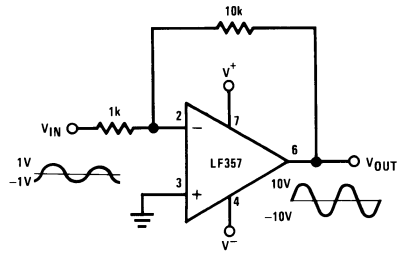
LF357 R = 1.25k

Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_{L(MAX)} \simeq 0.01\mu F$.

Overshoot ≤ 20%

Settling time (t_s) ≃ 5µs

LF357. A Large Power BW Amplifier



00564615

For distortion ≤ 1% and a 20 Vp-p V_{OUT} swing, power bandwidth is: 500kHz.

National Semiconductor

February 1995

LM2907/LM2917 Frequency to Voltage Converter

General Description

The LM2907, LM2917 series are monolithic frequency to voltage converters with a high gain op amp/comparator designed to operate a relay, lamp, or other load when the input frequency reaches or exceeds a selected rate. The tachometer uses a charge pump technique and offers frequency doubling for low ripple, full input protection in two versions (LM2907-8, LM2917-8) and its output swings to ground for a zero frequency input.

Advantages

- Output swings to ground for zero frequency input
- Easy to use; $V_{OUT} = f_{IN} \times V_{CC} \times R1 \times C1$
- Only one RC network provides frequency doubling
- Zener regulator on chip allows accurate and stable frequency to voltage or current conversion (LM2917)

Features

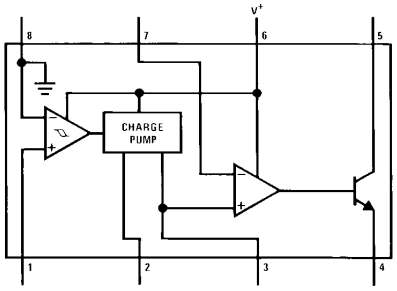
- Ground referenced tachometer input interfaces directly with variable reluctance magnetic pickups
- Op amp/comparator has floating transistor output
- 50 mA sink or source to operate relays, solenoids, meters, or LEDs
- Frequency doubling for low ripple
- Tachometer has built-in hysteresis with either differential input or ground referenced input
- Built-in zener on LM2917
- ±0.3% linearity typical
- Ground referenced tachometer is fully protected from damage due to swings above V_{CC} and below ground

Applications

- Over/under speed sensing
- Frequency to voltage conversion (tachometer)
- Speedometers
- Breaker point dwell meters
- Hand-held tachometer
- Speed governors
- Cruise control
- Automotive door lock control
- Clutch control
- Horn control
- Touch or sound switches

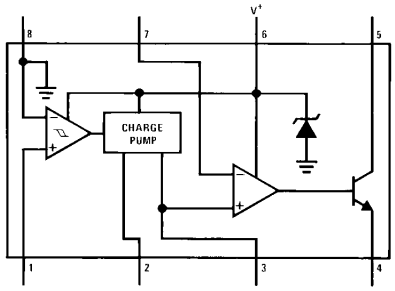
Block and Connection Diagrams

Dual-In-Line and Small Outline Packages, Top Views



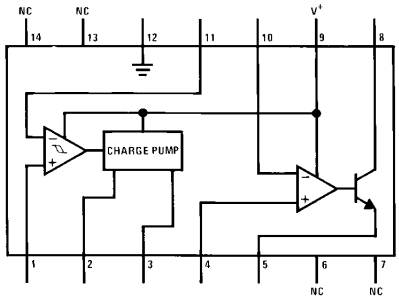
TL/H/7942–1

Order Number LM2907M-8 or LM2907N-8
See NS Package Number M08A or N08E



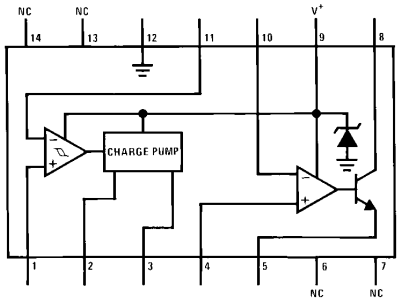
TL/H/7942–2

Order Number LM2917M-8 or LM2917N-8
See NS Package Number M08A or N08E



TL/H/7942–3

Order Number LM2907N
See NS Package Number N14A



TL/H/7942–4

Order Number LM2917M or LM2917N
See NS Package Number M14A or N14A

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	28V
Supply Current (Zener Options)	25 mA
Collector Voltage	28V
Differential Input Voltage	
Tachometer	28V
Op Amp/Comparator	28V
Input Voltage Range	
Tachometer LM2907-8, LM2917-8	±28V
LM2907, LM2917	0.0V to +28V
Op Amp/Comparator	0.0V to +28V
Power Dissipation	
LM2907-8, LM2917-8	1200 mW
LM2907-14, LM2917-14 (See Note 1)	1580 mW
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics V_{CC} = 12 V_{DC}, T_A = 25°C, see test circuit

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TACHOMETER						
	Input Thresholds	V_{IN} = 250 mVp-p @ 1 kHz (Note 2)	±10	±25	±40	mV
	Hysteresis	V_{IN} = 250 mVp-p @ 1 kHz (Note 2)		30		mV
	Offset Voltage	V_{IN} = 250 mVp-p @ 1 kHz (Note 2)				
	LM2907/LM2917			3.5	10	mV
	LM2907-8/LM2917-8			5	15	mV
	Input Bias Current	V_{IN} = ±50 mV_{DC}		0.1	1	μA
V_{OH}	Pin 2	V_{IN} = +125 mV_{DC} (Note 3)		8.3		V
V_{OL}	Pin 2	V_{IN} = −125 mV_{DC} (Note 3)		2.3		V
I_2, I_3	Output Current	V2 = V3 = 6.0V (Note 4)	140	180	240	μA
I_3	Leakage Current	I2 = 0, V3 = 0			0.1	μA
K	Gain Constant	(Note 3)	0.9	1.0	1.1	
	Linearity	f_{IN} = 1 kHz, 5 kHz, 10 kHz (Note 5)	−1.0	0.3	+1.0	%
OP/AMP COMPARATOR						
V_{OS}		V_{IN} = 6.0V		3	10	mV
I_{BIAS}		V_{IN} = 6.0V		50	500	nA
	Input Common-Mode Voltage		0		V_{CC}−1.5V	V
	Voltage Gain			200		V/mV
	Output Sink Current	V_C = 1.0	40	50		mA
	Output Source Current	V_E = V_{CC} −2.0		10		mA
	Saturation Voltage	I_{SINK} = 5 mA		0.1	0.5	V
		I_{SINK} = 20 mA			1.0	V
		I_{SINK} = 50 mA		1.0	1.5	V

Electrical Characteristics V_{CC} = 12 V_{DC}, T_A = 25°C, see test circuit (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ZENER REGULATOR						
	Regulator Voltage	R_{DROP} = 470Ω		7.56		V
	Series Resistance			10.5	15	Ω
	Temperature Stability			+1		mV/°C
	TOTAL SUPPLY CURRENT			3.8	6	mA

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 101°C/W junction to ambient for LM2907-8 and LM2917-8, and 79°C/W junction to ambient for LM2907-14 and LM2917-14.

Note 2: Hysteresis is the sum $+V_{TH} - (-V_{TH})$, offset voltage is their difference. See test circuit.

Note 3: V_{OH} is equal to ¾ × V_{CC} − 1 V_{BE}, V_{OL} is equal to ¼ × V_{CC} − 1 V_{BE} therefore $V_{OH} - V_{OL} = V_{CC}/2$. The difference, $V_{OH} - V_{OL}$, and the mirror gain, I_2/I_3, are the two factors that cause the tachometer gain constant to vary from 1.0.

Note 4: Be sure when choosing the time constant R1 × C1 that R1 is such that the maximum anticipated output voltage at pin 3 can be reached with I_3 × R1. The maximum value for R1 is limited by the output resistance of pin 3 which is greater than 10 MΩ typically.

Note 5: Nonlinearity is defined as the deviation of V_{OUT} (@ pin 3) for f_{IN} = 5 kHz from a straight line defined by the V_{OUT} @ 1 kHz and V_{OUT} @ 10 kHz. C1 = 1000 pF, R1 = 68k and C2 = 0.22 mFd.

General Description (Continued)

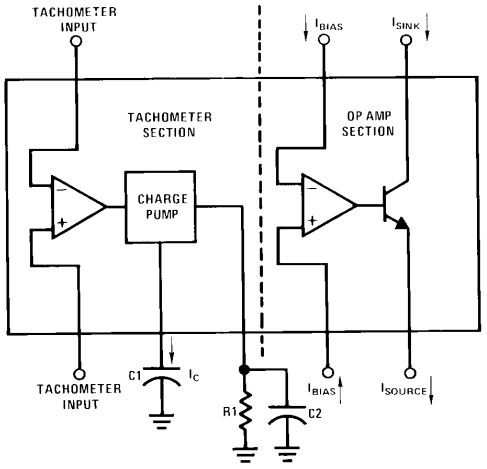
The op amp/comparator is fully compatible with the tachometer and has a floating transistor as its output. This feature allows either a ground or supply referred load of up to 50 mA. The collector may be taken above V_{CC} up to a maximum V_{CE} of 28V.

The two basic configurations offered include an 8-pin device with a *ground referenced tachometer* input and an internal connection between the tachometer output and the op amp non-inverting input. This version is well suited for single speed or frequency switching or fully buffered frequency to voltage conversion applications.

The more versatile configurations provide differential tachometer input and uncommitted op amp inputs. With this version the tachometer input may be floated and the op amp becomes suitable for active filter conditioning of the tachometer output.

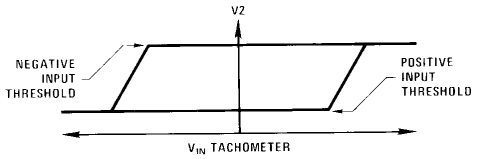
Both of these configurations are available with an active shunt regulator connected across the power leads. The regulator clamps the supply such that stable frequency to voltage and frequency to current operations are possible with any supply voltage and a suitable resistor.

Test Circuit and Waveform



TL/H/7942–6

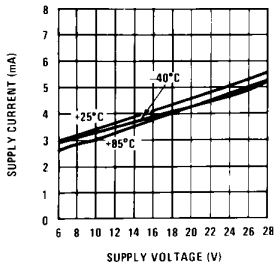
Tachometer Input Threshold Measurement



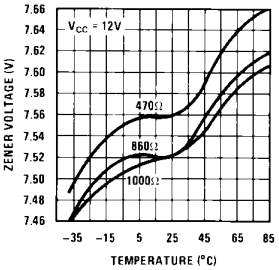
TL/H/7942–7

Typical Performance Characteristics

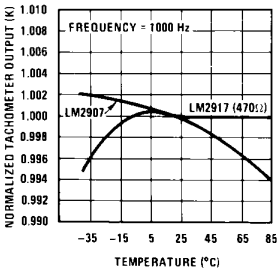
Total Supply Current



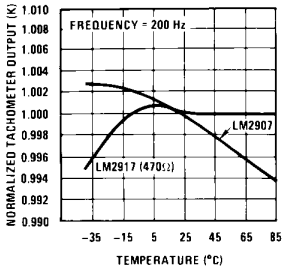
Zener Voltage vs Temperature



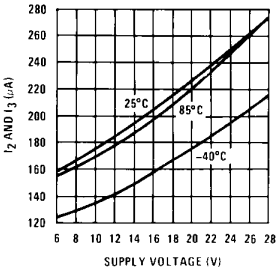
Normalized Tachometer Output vs Temperature



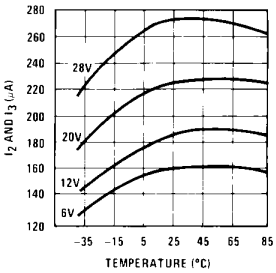
Normalized Tachometer Output vs Temperature



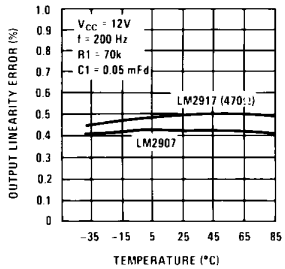
Tachometer Currents I_2 and I_3 vs Supply Voltage



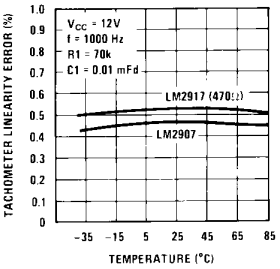
Tachometer Currents I_2 and I_3 vs Temperature



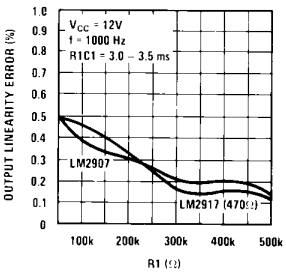
Tachometer Linearity vs Temperature



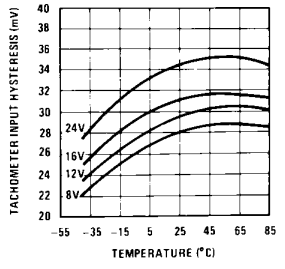
Tachometer Linearity vs Temperature



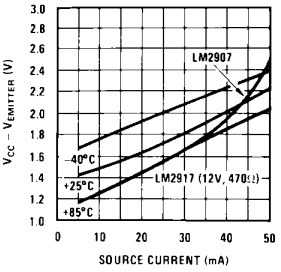
Tachometer Linearity vs R1



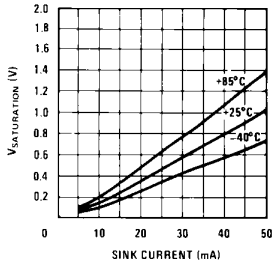
Tachometer Input Hysteresis vs Temperature



Op Amp Output Transistor Characteristics



Op Amp Output Transistor Characteristics



TL/H/7942–5

Applications Information

The LM2907 series of tachometer circuits is designed for minimum external part count applications and maximum versatility. In order to fully exploit its features and advantages let's examine its theory of operation. The first stage of operation is a differential amplifier driving a positive feedback flip-flop circuit. The input threshold voltage is the amount of differential input voltage at which the output of this stage changes state. Two options (LM2907-8, LM2917-8) have one input internally grounded so that an input signal must swing above and below ground and exceed the input thresholds to produce an output. This is offered specifically for magnetic variable reluctance pickups which typically provide a single-ended ac output. This single input is also fully protected against voltage swings to ± 28V, which are easily attained with these types of pickups.

The differential input options (LM2907, LM2917) give the user the option of setting his own input switching level and still have the hysteresis around that level for excellent noise rejection in any application. Of course in order to allow the inputs to attain common-mode voltages above ground, input protection is removed and neither input should be taken outside the limits of the supply voltage being used. It is very important that an input not go below ground without some resistance in its lead to limit the current that will then flow in the epi-substrate diode.

Following the input stage is the charge pump where the input frequency is converted to a dc voltage. To do this requires one timing capacitor, one output resistor, and an integrating or filter capacitor. When the input stage changes state (due to a suitable zero crossing or differential voltage on the input) the timing capacitor is either charged or discharged linearly between two voltages whose difference is $V_{CC}/2$. Then in one half cycle of the input frequency or a time equal to $1/2\ f_{IN}$ the change in charge on the timing capacitor is equal to $V_{CC}/2 \times C1$. The average amount of current pumped into or out of the capacitor then is:

$$\frac{\Delta Q}{T} = i_{c(AVG)} = C1 \times \frac{V_{CC}}{2} \times (2f_{IN}) = V_{CC} \times f_{IN} \times C1$$

The output circuit mirrors this current very accurately into the load resistor R1, connected to ground, such that if the pulses of current are integrated with a filter capacitor, then $V_O = i_c \times R1$, and the total conversion equation becomes:

$$V_O = V_{CC} \times f_{IN} \times C1 \times R1 \times K$$

Where K is the gain constant—typically 1.0.

The size of C2 is dependent only on the amount of ripple voltage allowable and the required response time.

CHOOSING R1 AND C1

There are some limitations on the choice of R1 and C1 which should be considered for optimum performance. The timing capacitor also provides internal compensation for the charge pump and should be kept larger than 500 pF for very accurate operation. Smaller values can cause an error current on R1, especially at low temperatures. Several considerations must be met when choosing R1. The output current at pin 3 is internally fixed and therefore $V_O/R1$ must be less than or equal to this value. If R1 is too large, it can become a significant fraction of the output impedance at pin 3 which degrades linearity. Also output ripple voltage must be considered and the size of C2 is affected by R1. An expression that describes the ripple content on pin 3 for a single R1C2 combination is:

$$V_{RIPPLE} = \frac{V_{CC}}{2} \times \frac{C1}{C2} \times \left(1 - \frac{V_{CC} \times f_{IN} \times C1}{I_2}\right) \text{ pk-pk}$$

It appears R1 can be chosen independent of ripple, however response time, or the time it takes V_{OUT} to stabilize at a new voltage increases as the size of C2 increases, so a compromise between ripple, response time, and linearity must be chosen carefully.

As a final consideration, the maximum attainable input frequency is determined by V_{CC}, C1 and I_2:

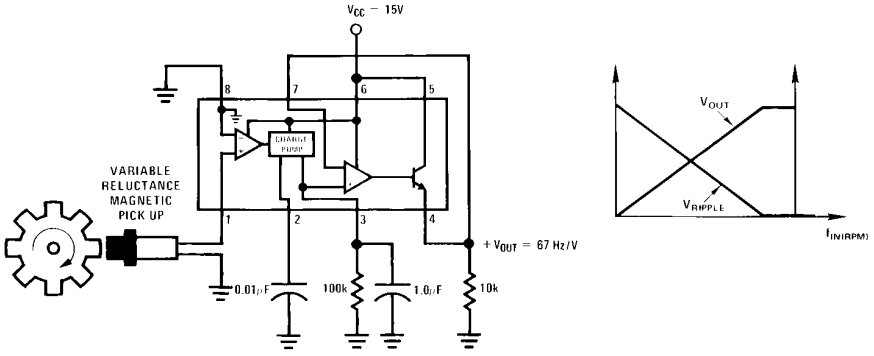
$$f_{MAX} = \frac{I_2}{C1 \times V_{CC}}$$

USING ZENER REGULATED OPTIONS (LM2917)

For those applications where an output voltage or current must be obtained independent of supply voltage variations, the LM2917 is offered. The most important consideration in choosing a dropping resistor from the unregulated supply to the device is that the tachometer and op amp circuitry alone require about 3 mA at the voltage level provided by the zener. At low supply voltages there must be some current flowing in the resistor above the 3 mA circuit current to operate the regulator. As an example, if the raw supply varies from 9V to 16V, a resistance of 470Ω will minimize the zener voltage variation to 160 mV. If the resistance goes under 400Ω or over 600Ω the zener variation quickly rises above 200 mV for the same input variation.

Typical Applications

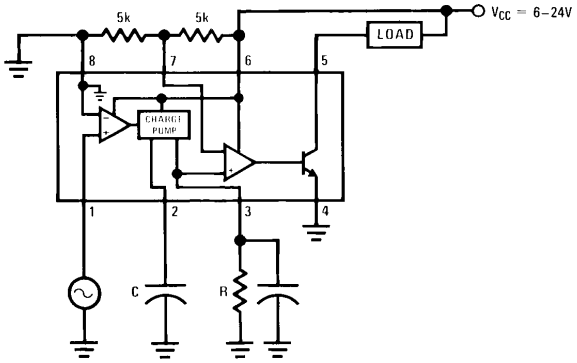
Minimum Component Tachometer



TL/H/7942–8

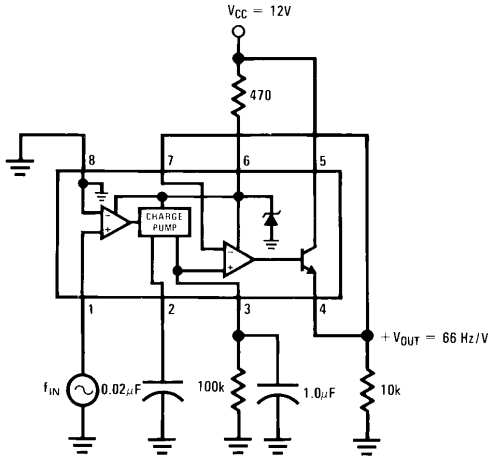
Typical Applications (Continued)

"Speed Switch" Load is Energized When $f_{IN} \geq \frac{1}{2RC}$



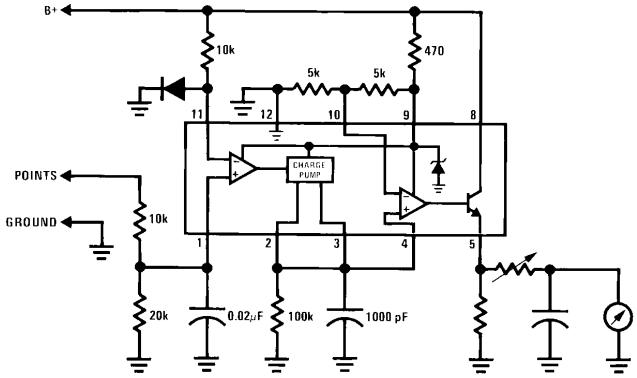
TL/H/7942–9

Zener Regulated Frequency to Voltage Converter



TL/H/7942–10

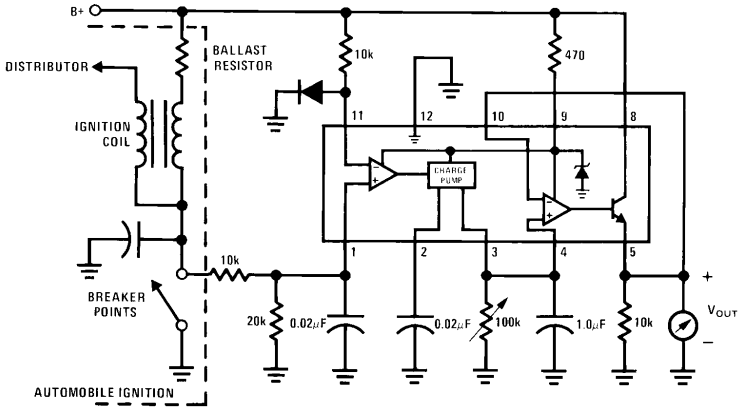
Breaker Point Dwell Meter



TL/H/7942–11

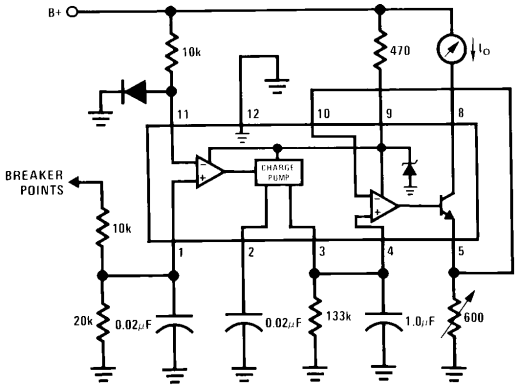
Typical Applications (Continued)

Voltage Driven Meter Indicating Engine RPM
V_O = 6V @ 400 Hz or 6000 ERPM (8 Cylinder Engine)



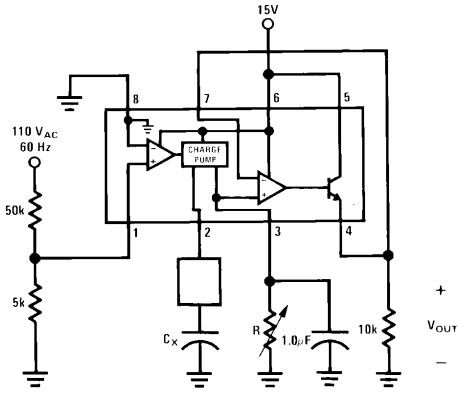
TL/H/7942–12

Current Driven Meter Indicating Engine RPM
I_O = 10 mA @ 300 Hz or 6000 ERPM (6 Cylinder Engine)



TL/H/7942–13

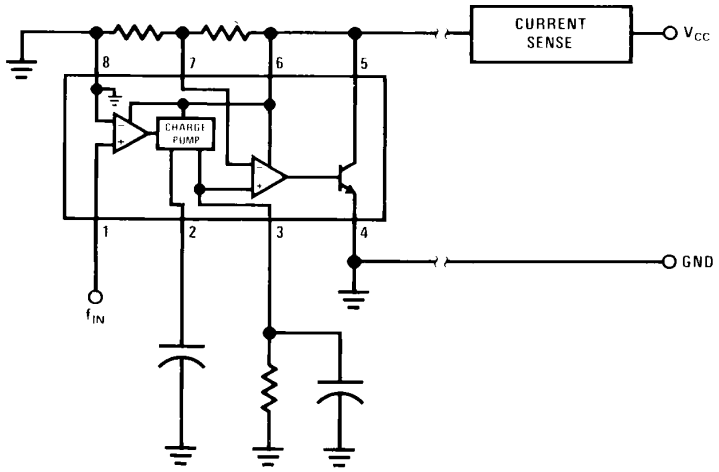
Capacitance Meter
V_{OUT} = 1V–10V for C_X = 0.01 to 0.1 mFd
(R = 111k)



TL/H/7942–14

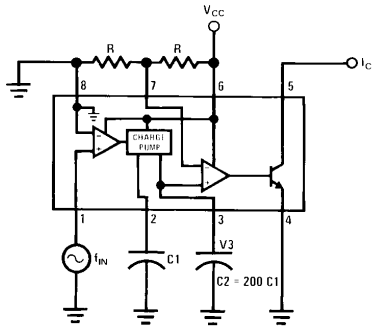
Typical Applications (Continued)

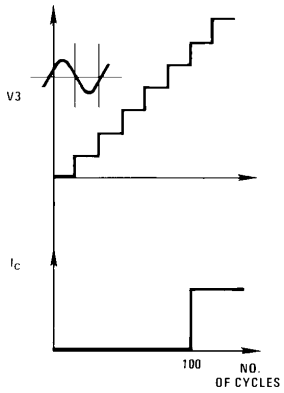
Two-Wire Remote Speed Switch



TL/H/7942–15

100 Cycle Delay Switch





TL/H/7942–16

V3 steps up in voltage by the amount $\frac{V_{CC} \times C1}{C2}$

for each complete input cycle (2 zero crossings)

Example:

If C2 = 200 C1 after 100 consecutive input cycles.

V3 = 1/2 V_{CC}

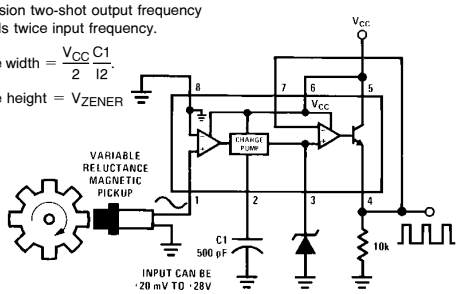
Typical Applications (Continued)

Variable Reluctance Magnetic Pickup Buffer Circuits

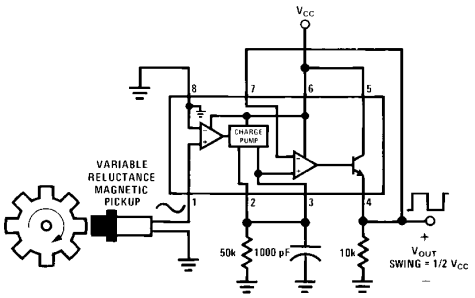
Precision two-shot output frequency equals twice input frequency.

Pulse width = $\frac{V_{CC}}{2}\frac{C1}{I2}$.

Pulse height = V_{ZENER}

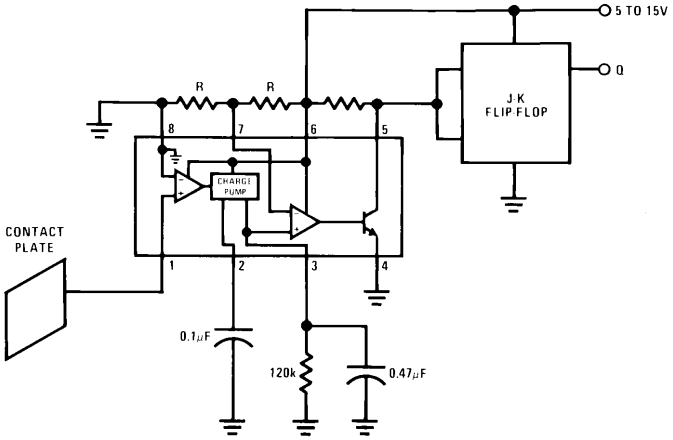


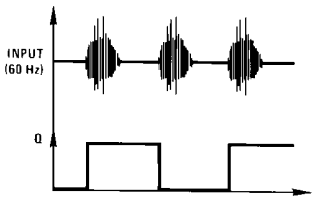
TL/H/7942–39



TL/H/7942–17

Finger Touch or Contact Switch

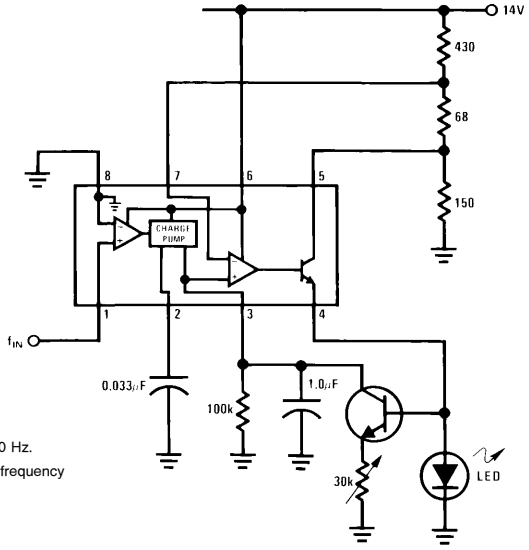




TL/H/7942–19

TL/H/7942–18

Flashing LED Indicates Overspeed



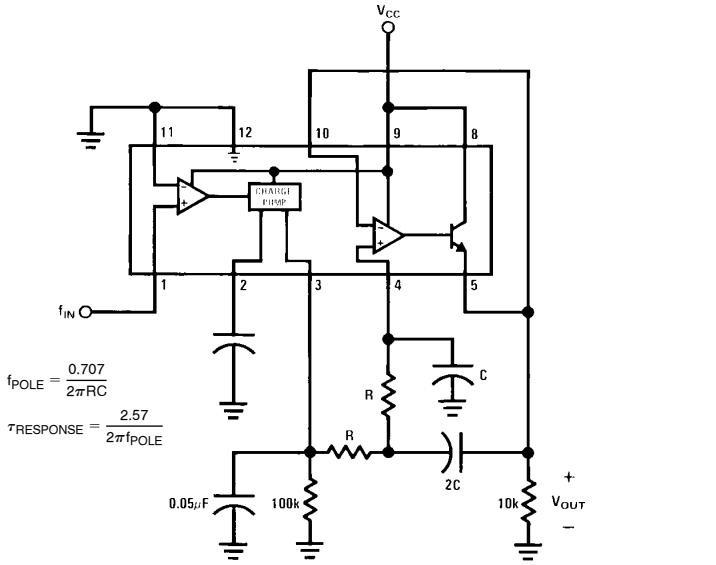
Flashing begins when $f_{IN} \geq 100$ Hz.

Flash rate increases with input frequency increase beyond trip point.

TL/H/7942–20

Typical Applications (Continued)

Frequency to Voltage Converter with 2 Pole Butterworth Filter to Reduce Ripple

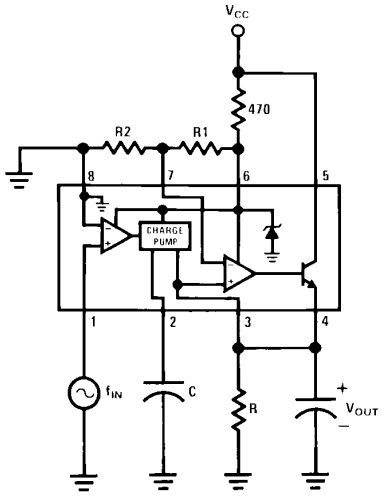


$$f_{POLE} = \frac{0.707}{2\pi RC}$$

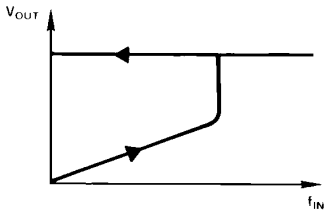
$$\tau_{RESPONSE} = \frac{2.57}{2\pi f_{POLE}}$$

TL/H/7942–21

Overspeed Latch



TL/H/7942–22



TL/H/7942–23

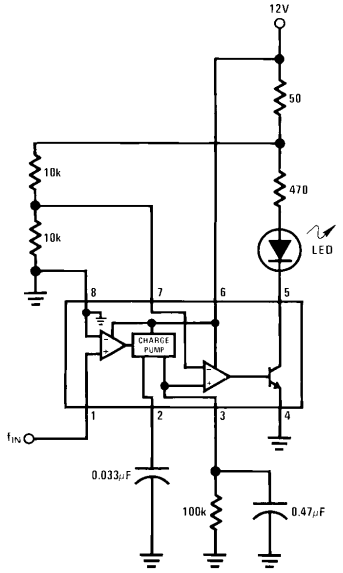
Output latches when

$$f_{IN} = \frac{R2}{R1 + R2}\frac{1}{RC}$$

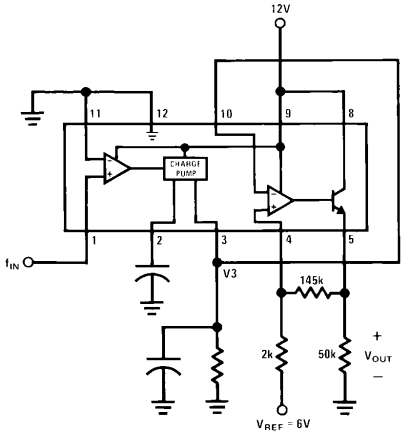
Reset by removing V_{CC}.

Typical Applications (Continued)

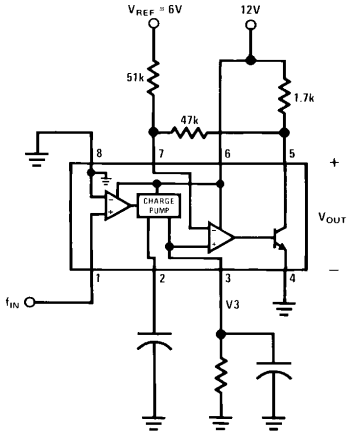
Some Frequency Switch Applications May Require Hysteresis in the Comparator Function Which can be Implemented in Several Ways:



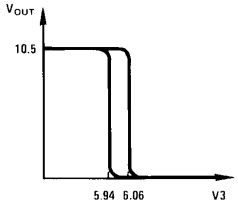
TL/H/7942–24



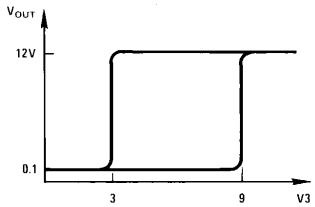
TL/H/7942–25



TL/H/7942–26



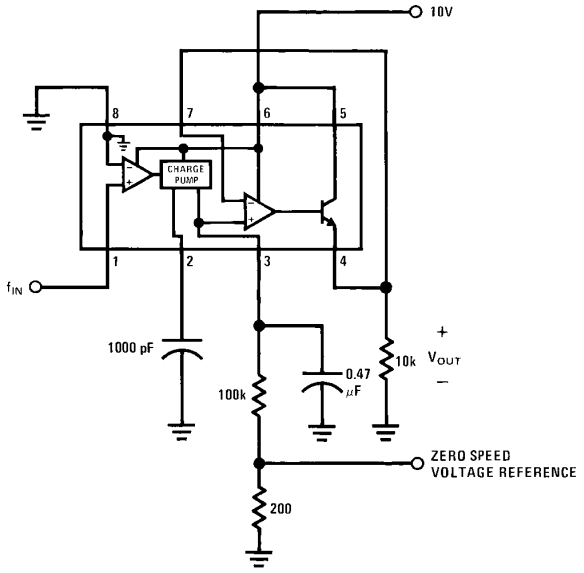
TL/H/7942–27



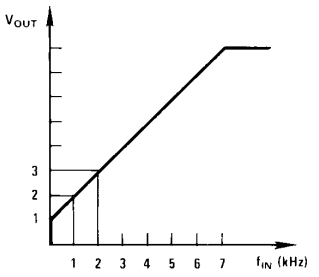
TL/H/7942–28

Typical Applications (Continued)

Changing the Output Voltage for an Input Frequency of Zero

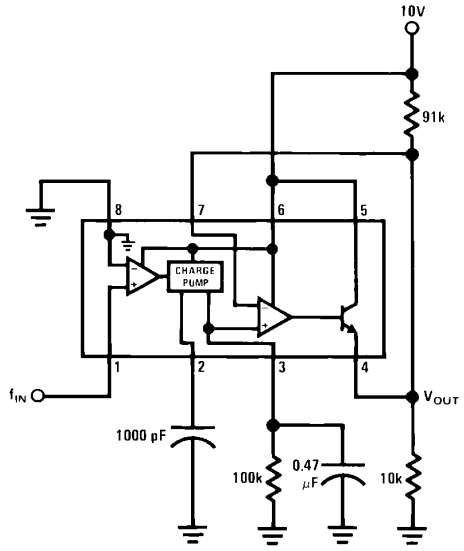


TL/H/7942–29

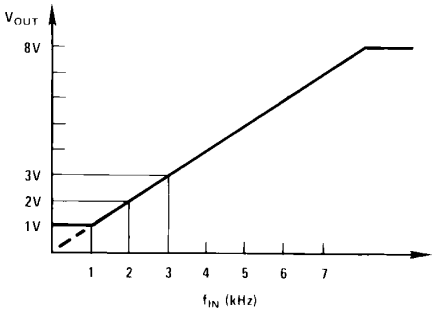


TL/H/7942–30

Changing Tachometer Gain Curve or Clamping the Minimum Output Voltage



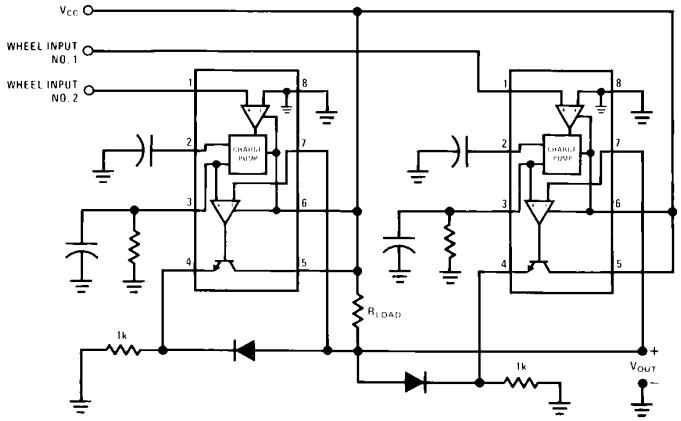
TL/H/7942–31



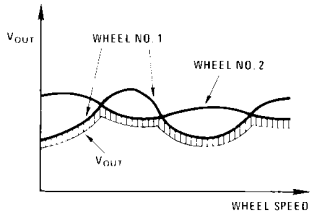
TL/H/7942–32

Anti-Skid Circuit Functions

"Select-Low" Circuit



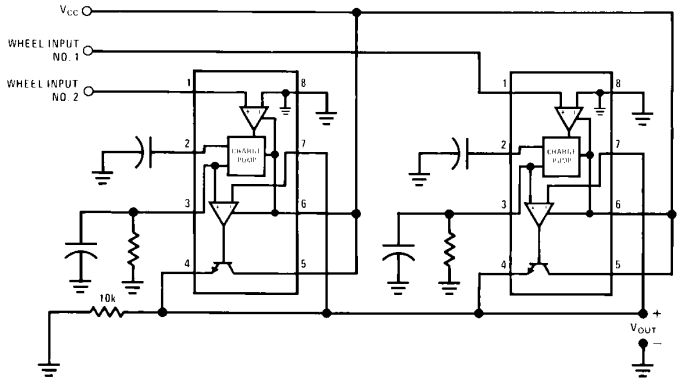
TL/H/7942–33



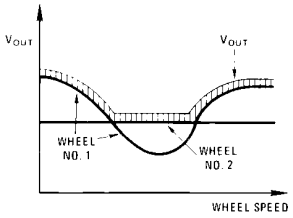
TL/H/7942–34

V_{OUT} is proportional to the lower of the two input wheel speeds.

"Select-High" Circuit



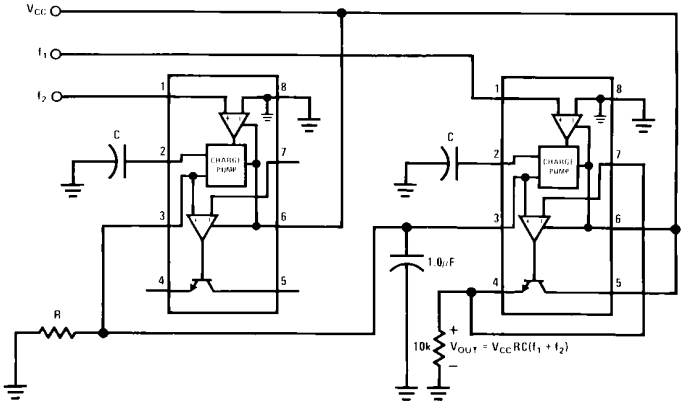
TL/H/7942–35



TL/H/7942–36

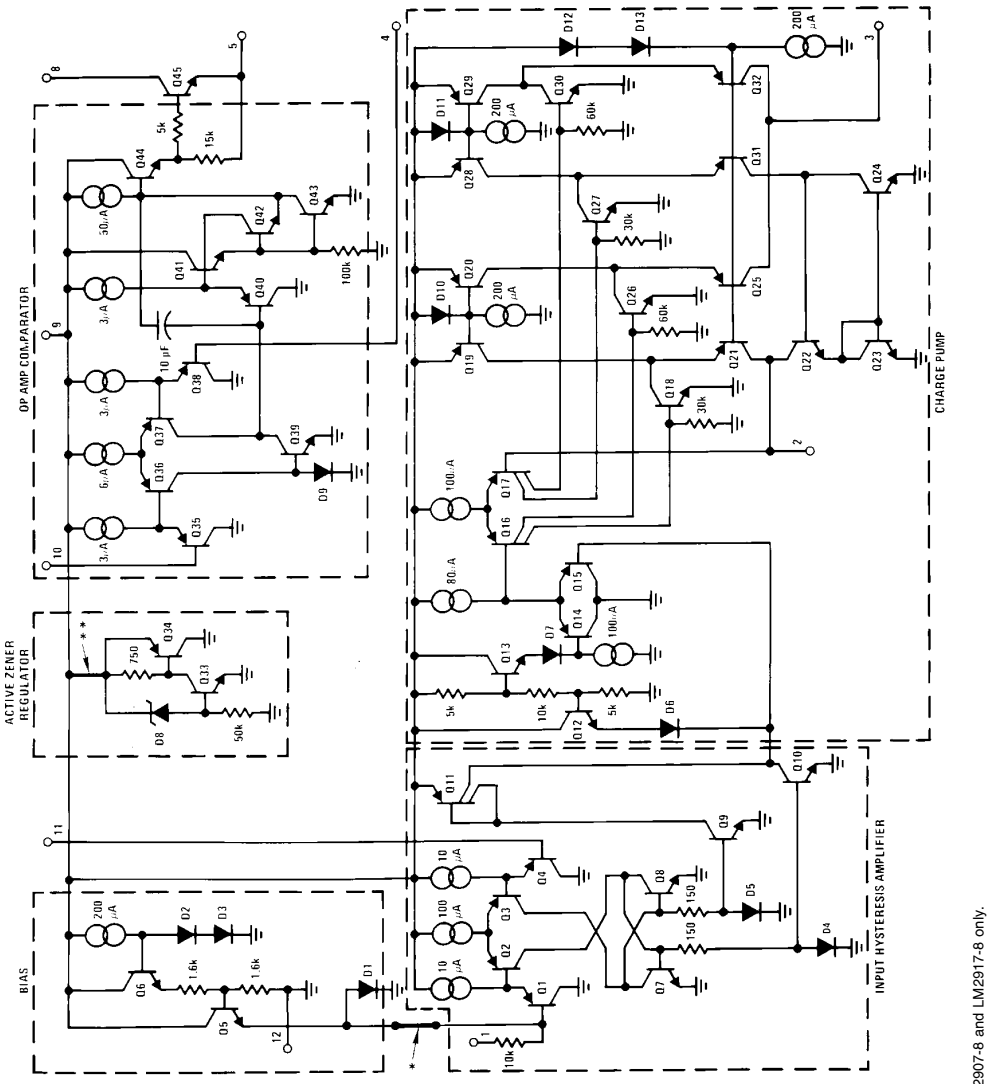
V_{OUT} is proportional to the higher of the two input wheel speeds.

"Select-Average" Circuit



TL/H/7942–37

Equivalent Schematic Diagram



TL/H/7942–38

*This connection made on LM2907-8 and LM2917-8 only.

**This connection made on LM2917 and LM2917-8 only.

Tone decoder/phase-locked loop | NE/SE567

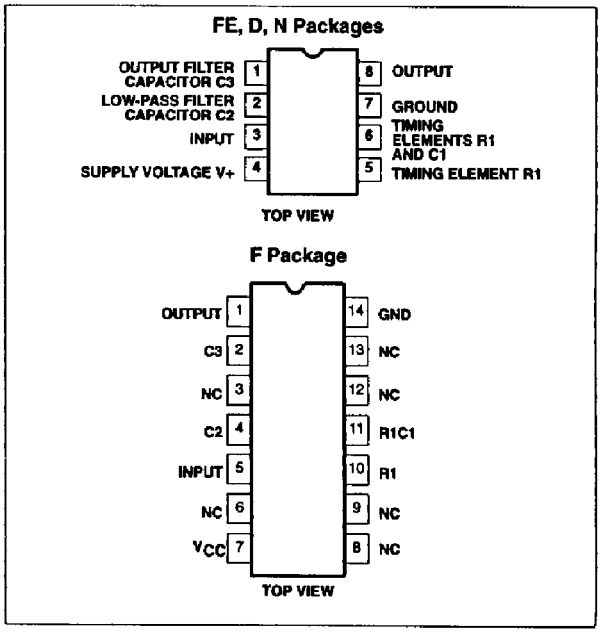
DESCRIPTION

The NE/SE567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the self-biased input. The bandwidth center frequency and output delay are independently determined by means of four external components.

FEATURES

- Wide frequency range (.01Hz to 500kHz)
- High stability of center frequency
- Independently controllable bandwidth (up to 14%)
- High out-band signal and noise rejection
- Logic-compatible output with 100mA current sinking capability
- Inherent immunity to false signals
- Frequency adjustment over a 20-to-1 range with an external resistor
- Military processing available

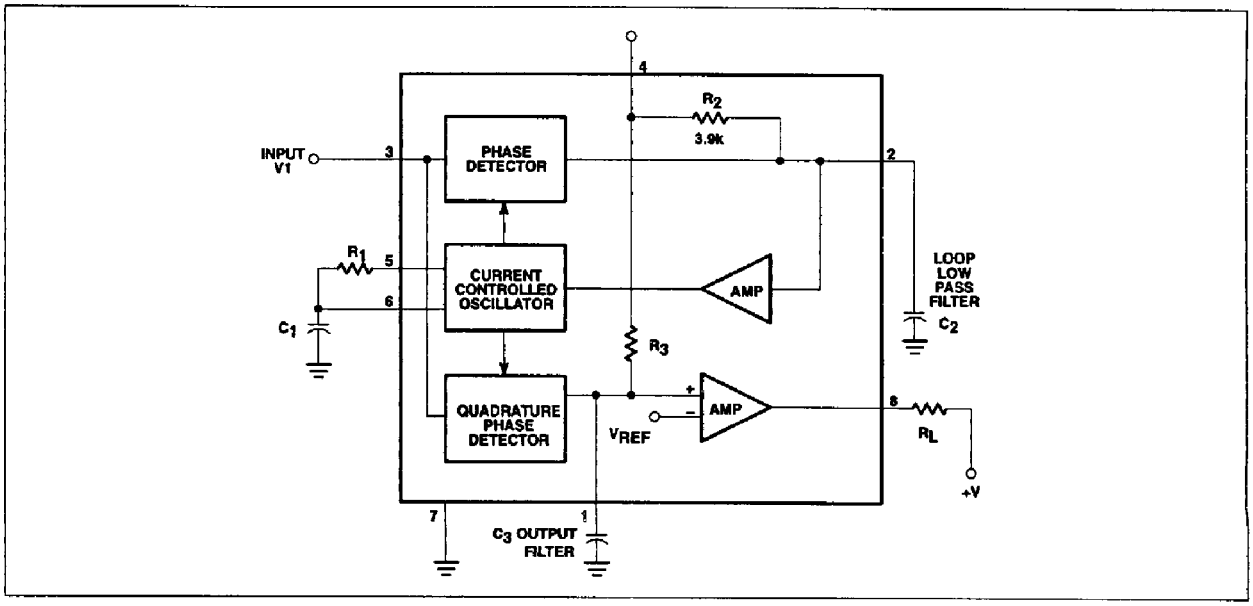
PIN CONFIGURATIONS



APPLICATIONS

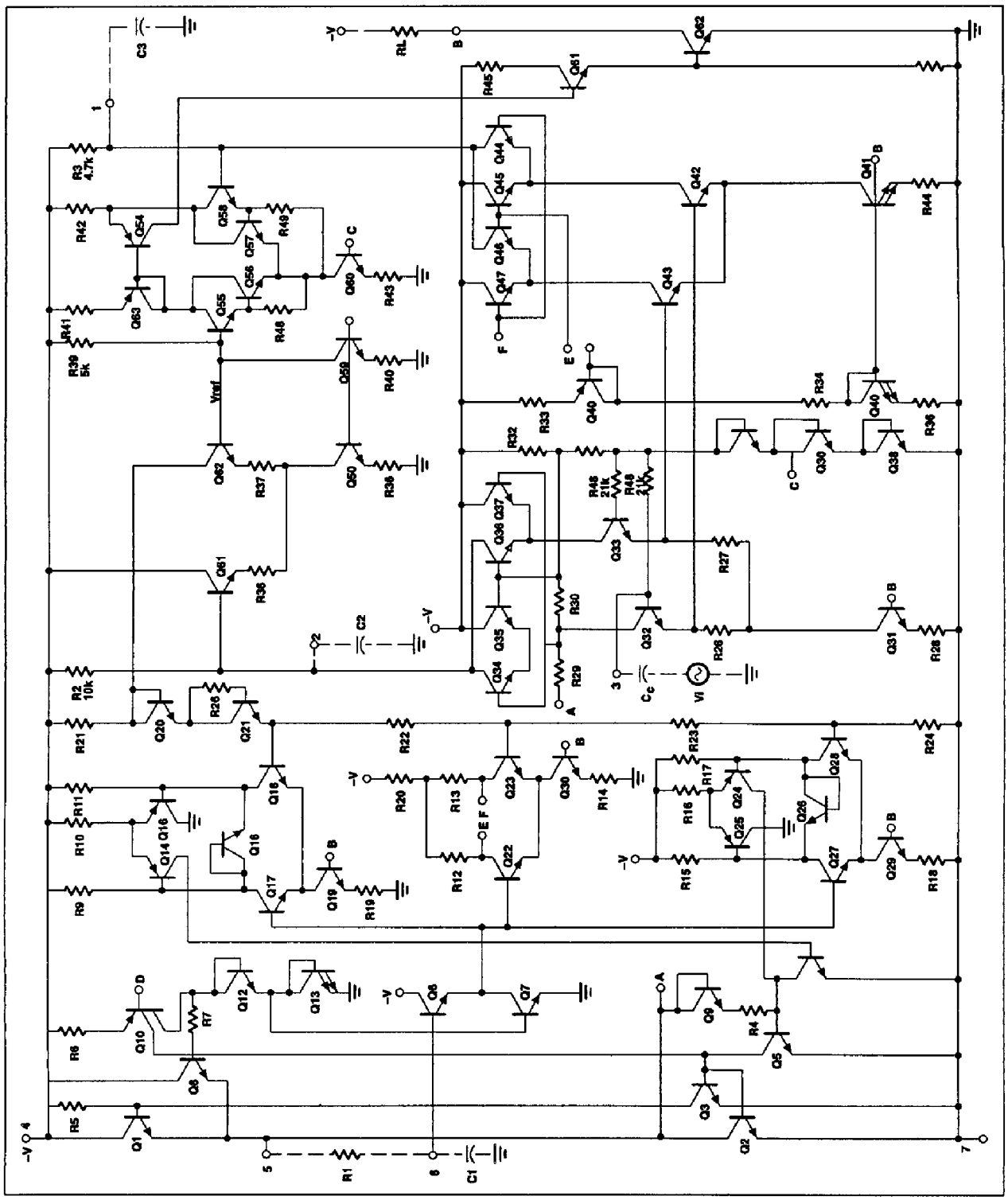
- Touch-Tone® decoding
- Carrier current remote controls
- Ultrasonic controls (remote TV, etc.)
- Communications paging
- Frequency monitoring and control
- Wireless intercom
- Precision oscillator

BLOCK DIAGRAM



®Touch-Tone is a registered trademark of AT&T.

EQUIVALENT SCHEMATIC



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic SO	0 to +70°C	NE567D	0174C
14-Pin Cerdip	0 to +70°C	NE567F	0581B
8-Pin Plastic DIP	0 to +70°C	NE567N	0404B
8-Pin Plastic SO	-55°C to +125°C	SE567D	0174C
8-Pin Cerdip	-55°C to +125°C	SE567FE	0581B
8-Pin Plastic DIP	-55°C to +125°C	SE567N	0404B

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating temperature		
	NE567	0 to +70	°C
	SE567	-55 to +125	°C
V_{CC}	Operating voltage	10	V
V+	Positive voltage at input	0.5 +V_S	V
V-	Negative voltage at input	-10	V_{DC}
V_{OUT}	Output voltage (collector of output transistor)	15	V_{DC}
T_{STG}	Storage temperature range	-65 to +150	°C
P_D	Power dissipation	300	mW

DC ELECTRICAL CHARACTERISTICS

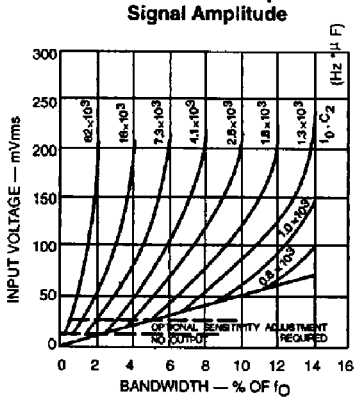
V +=5.0V; T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE567			NE567			UNIT
			Min	Typ	Max	Min	Typ	Max	
Center frequency[1]									
f_O	Highest center frequency			500			500		kHz
f_O	Center frequency stability[2]	-55 to +125°C		35 ±140			35 ±140		ppm/°C
		0 to +70°C		35 ±60			35 ±60		ppm/°C
f_O	Center frequency distribution	$f_O = 100kHz = \frac{1}{1.1R_1C_1}$	-10	0	+10	-10	0	+10	%
f_O	Center frequency shift with supply voltage	$f_O = 100kHz = \frac{1}{1.1R_1C_1}$		0.5	1		0.7	2	%/V
Detection bandwidth									
BW	Largest detection bandwidth	$f_O = 100kHz = \frac{1}{1.1R_1C_1}$	12	14	16	10	14	18	% of f_O
BW	Largest detection bandwidth skew			2	4		3	6	% of f_O
BW	Largest detection bandwidth—variation with temperature	V_I=300mV$_{RMS}$		±0.1			±0.1		%/°C
BW	Largest detection bandwidth—variation with supply voltage	V_I=300mV$_{RMS}$		±2			±2		%/V
Input									
R_{IN}	Input resistance		15	20	25	15	20	25	kΩ
V_I	Smallest detectable input voltage[4]	I_L=100mA, $f_I=f_O$		20	25		20	25	mV$_{RMS}$
	Largest no-output input voltage[4]	I_L=100mA, $f_I=f_O$	10	15		10	15		mV$_{RMS}$
	Greatest simultaneous out-band signal-to-in-band signal ratio			+6			+6		dB
	Minimum input signal to wide-band noise ratio	B_n=140kHz		-6			-6		dB
Output									
	Fastest on-off cycling rate			f_O/20			f_O/20		
	"1" output leakage current	V_8=15V		0.01	25		0.01	25	µA
	"0" output voltage	I_L=30mA		0.2	0.4		0.2	0.4	V
		I_L=100mA		0.6	1.0		0.6	1.0	V
t_F	Output fall time[3]	R_L=50Ω		30			30		ns
t_R	Output rise time[3]	R_L=50Ω		150			150		ns
General									
V_{CC}	Operating voltage range		4.75		9.0	4.75		9.0	V
	Supply current quiescent			6	8		7	10	mA
	Supply current—activated	R_L=20kΩ		11	13		12	15	mA
t_{PD}	Quiescent power dissipation			30			35		mW

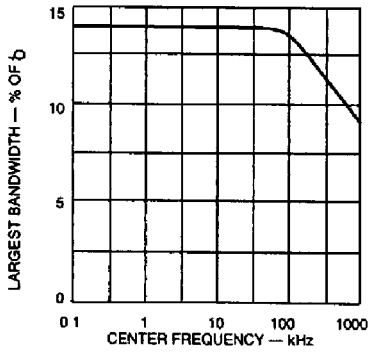
NOTES:
1. Frequency determining resistor R_1 should be between 2 and 20kΩ
2. Applicable over 4.75V to 5.75V. See graphs for more detailed information.
3. Pin 8 to Pin 1 feedback R_L network selected to eliminate pulsing during turn-on and turn-off.
4. With R_2=130kΩ from Pin 1 to V+. See Figure 1.

TYPICAL PERFORMANCE CHARACTERISTICS

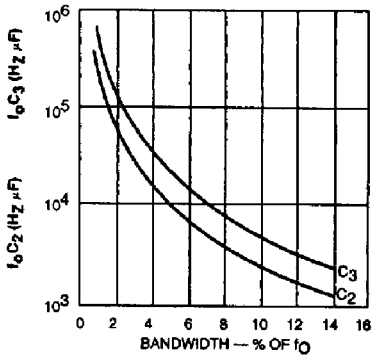
Bandwidth vs Input Signal Amplitude



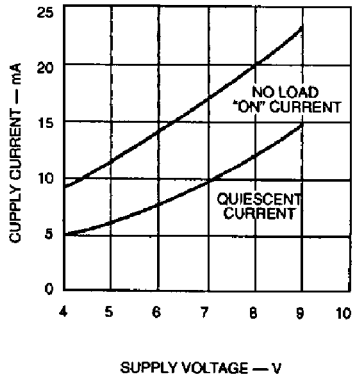
Largest Detection bandwidth vs Operating Frequency



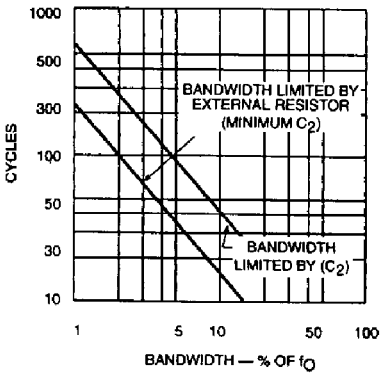
Detection bandwidth as a Function of C_2 and C_3



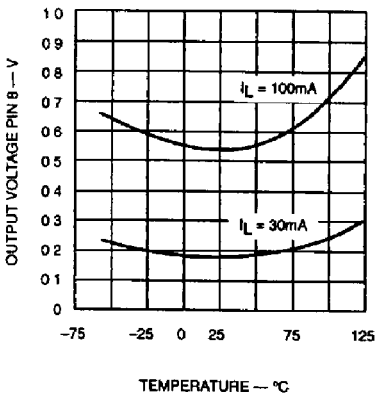
Typical Supply Current vs Supply Voltage



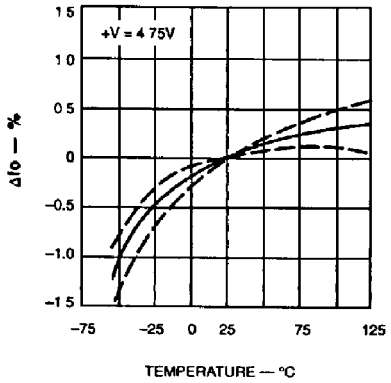
Greatest Number of Cycles Before Output



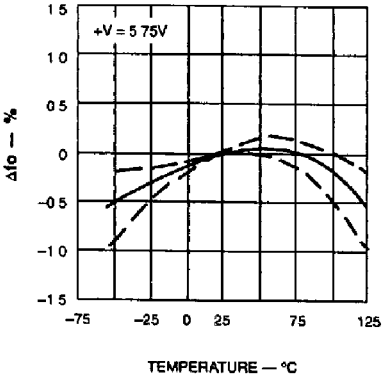
Typical Output Voltage vs Temperature



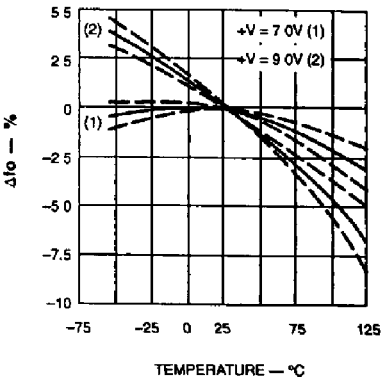
Typical Frequency Drift With Temperature (Mean and SD)



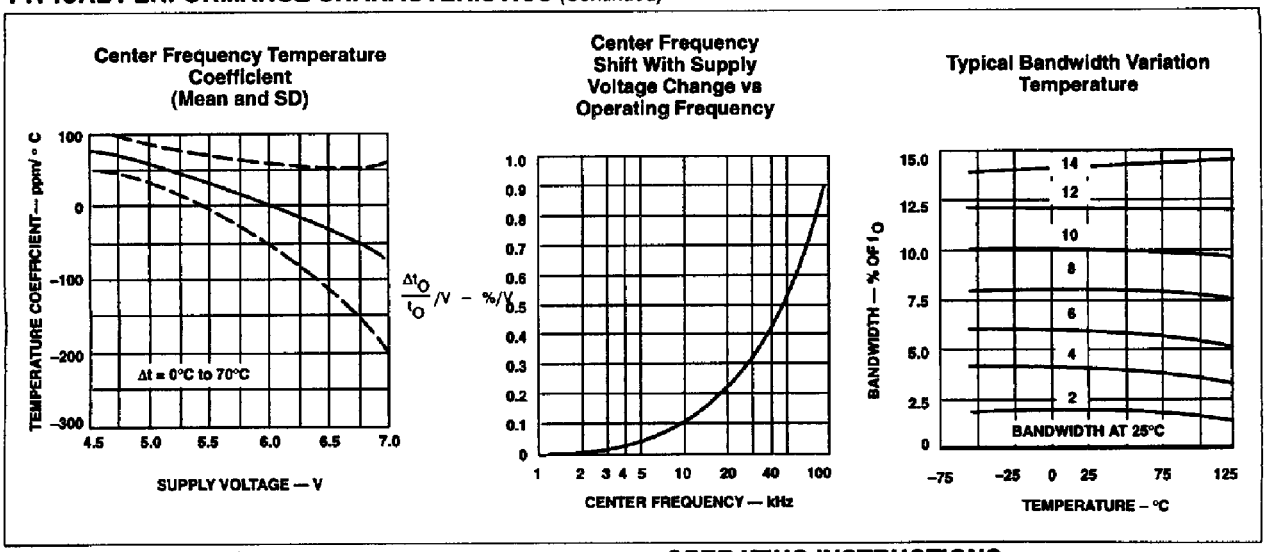
Typical Frequency Drift With Temperature (Mean and SD)



Typical Frequency Drift With Temperature (Mean and SD)



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



DESIGN FORMULAS

$$f_O \approx \frac{1}{1.1R_1 C_1}$$

$$BW \approx 1070 \sqrt{\frac{V_I}{f_O C_2}} \text{ in \% of } f_O$$

$$V_I \leq 200mV_{RMS}$$

Where
V_I=Input voltage (V_{RMS})
C_2=Low-pass filter capacitor (μF)

PHASE-LOCKED LOOP TERMINOLOGY CENTER FREQUENCY (f_O)

The free-running frequency of the current controlled oscillator (CCO) in the absence of an input signal.

Detection Bandwidth (BW)

The frequency range, centered about f_O, within which an input signal above the threshold voltage (typically $20mV_{RMS}$) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

Lock Range

The largest frequency range within which an input signal above the threshold voltage will hold a logical zero state on the output.

Detection Band Skew

A measure of how well the detection band is centered about the center frequency, f_O. The skew is defined as $(f_{MAX}+f_{MIN}-2f_O)/2f_O$ where fmax and fmin are the frequencies corresponding to the edges of the detection band. The skew can be reduced to zero if necessary by means of an optional centering adjustment.

OPERATING INSTRUCTIONS

Figure 1 shows a typical connection diagram for the 567. For most applications, the following three-step procedure will be sufficient for choosing the external components R_1, C_1, C_2 and C_3.

1. Select R1 and C1 for the desired center frequency. For best temperature stability, R1 should be between 2K and 20K ohm, and the combined temperature coefficient of the R1C1 product should have sufficient stability over the projected temperature range to meet the necessary requirements.
2. Select the low-pass capacitor, C_2, by referring to the Bandwidth versus Input Signal Amplitude graph. If the input amplitude Variation is known, the appropriate value of $f_O \cdot C_2$ necessary to give the desired bandwidth may be found. Conversely, an area of operation may be selected on this graph and the input level and C2 may be adjusted accordingly. For example, constant bandwidth operation requires that input amplitude be above $200mV_{RMS}$. The bandwidth, as noted on the graph, is then controlled solely by the $f_O \cdot C_2$ product (f_O (Hz), C2(μF)).

TYPICAL RESPONSE

NOTE:
R_L = 100Ω

Response to 100mV$_{RMS}$ Tone Burst

NOTES:
S/N = –6dB
R_L = 100Ω
Noise Bandwidth = 140Hz

Response to Same Input Tone Burst With Wideband Noise

3. The value of C3 is generally non-critical. C3 sets the band edge of a low-pass filter which attenuates frequencies outside the detection band to eliminate spurious outputs. If C3 is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency, or the output may pulse on and off during the turn-on transient. If C3 is too large, turn-on and turn-off of the

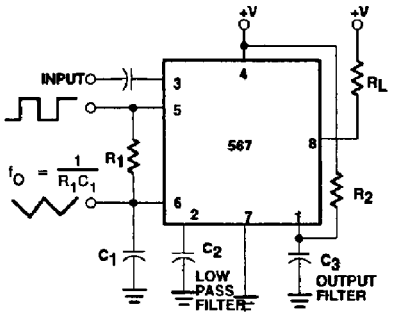


Figure 1.

output stage will be delayed until the voltage on C_3 passes the threshold voltage. (Such delay may be desirable to avoid spurious outputs due to transient frequencies.) A typical minimum value for C_3 is $2C_2$.

4. Optional resistor R2 sets the threshold for the largest "no output" input voltage. A value of 130kΩ is used to assure the tested limit of 10mV$_{RMS}$ min. This resistor can be referenced to ground for increased sensitivity. The explanation can be found in the "optional controls" section which follows.

AVAILABLE OUTPUTS (Figure 1)

The primary output is the uncommitted output transistor collector, Pin 8. When an in-band input signal is present, this transistor saturates; its collector voltage being less than 1.0 volt (typically 0.6V) at full output current (100mA). The voltage at Pin 2 is the phase detector output which is a linear function of frequency over the range of 0.95 to 1.05 f_O with a slope of about 20mV per percent of frequency deviation. The average voltage at Pin 1 is, during lock, a function of the in-band input amplitude in accordance with the transfer characteristic given. Pin 5 is the controlled oscillator square wave output of magnitude (+V -2V$_{BE}$)≅(+V-1.4V) having a DC average of +V/2. A 1kΩ load may be driven from pin 5. Pin 6 is an exponential triangle of 1V$_{P-P}$ with an average DC level of +V/2. Only high impedance loads may be

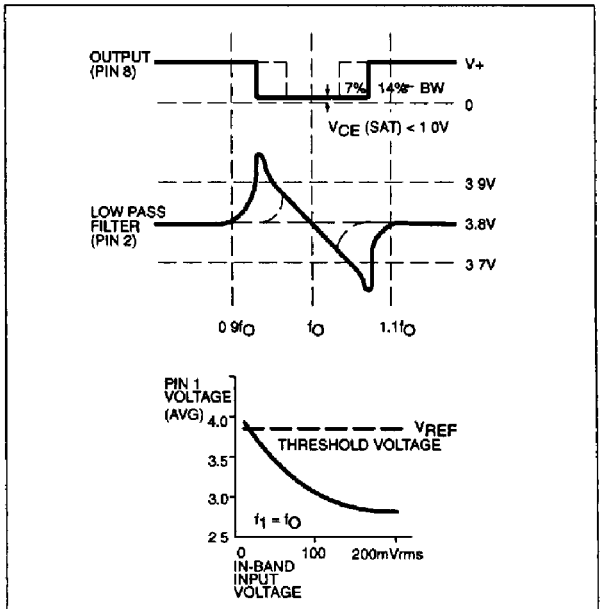


Figure 2. Typical Output Response

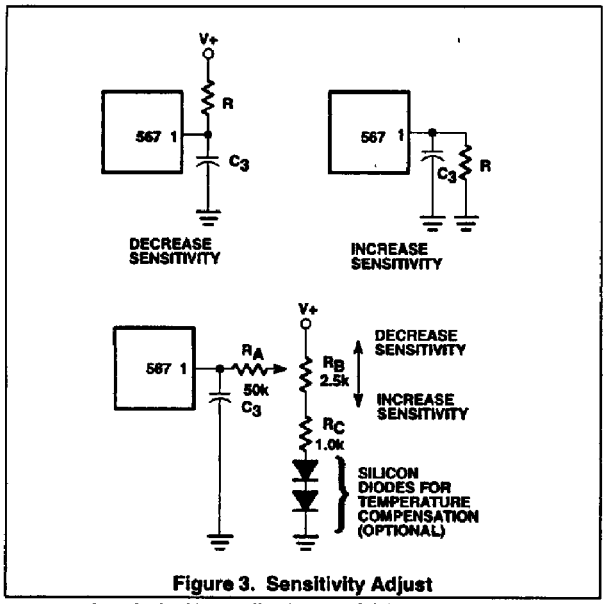


Figure 3. Sensitivity Adjust

connected to pin 6 without affecting the CCO duty cycle or temperature stability.

OPERATING PRECAUTIONS

A brief review of the following precautions will help the user achieve the high level of performance of which the 567 is capable.

1. Operation in the high input level mode (above 200mV) will free the user from bandwidth variations due to changes in the in-band signal amplitude. The input stage is now limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the inband signal is suppressed. Also, the limiting action will create in-band components from sub-harmonic signals, so the 567 becomes sensitive to signals at $f_O/3$, $f_O/5$, etc.
2. The 567 will lock onto signals near $(2n+1)\ f_O$, and will give an output for signals near $(4n+1)\ f_O$ where n=0, 1, 2, etc. Thus, signals at $5f_O$ and $9f_O$ can cause an unwanted output. If such signals are anticipated, they should be attenuated before reaching the 567 input.
3. Maximum immunity from noise and out-band signals is afforded in the low input level (below $200mV_{RMS}$) and reduced bandwidth operating mode. However, decreased loop damping causes the worst-case lock-up time to increase, as shown by the Greatest Number of Cycles Before Output vs Bandwidth graph.
4. Due to the high switching speeds (20ns) associated with 567 operation, care should be taken in lead routing. Lead lengths should be kept to a minimum. The power supply should be adequately bypassed close to the 567 with a 0.01µF or greater capacitor; grounding paths should be carefully chosen to avoid ground loops and unwanted voltage variations. Another factor which must be considered is the effect of load energization on the power supply. For example, an incandescent lamp typically draws 10 times rated current at turn-on. This can be somewhat greater when the output stage is made less sensitive, rejection of third harmonics or in-band harmonics (of lower frequency signals) is also improved.

cause supply voltage fluctuations which could, for example, shift the detection band of narrow-band systems sufficiently to cause momentary loss of lock. The result is a low-frequency oscillation into and out of lock. Such effects can be prevented by supplying heavy load currents from a separate supply or increasing the supply filter capacitor.

SPEED OF OPERATION

Minimum lock-up time is related to the natural frequency of the loop. The lower it is, the longer becomes the turn-on transient. Thus, maximum operating speed is obtained when C_2 is at a minimum. When the signal is first applied, the phase may be such as to initially drive the controlled oscillator away from the incoming frequency rather than toward it. Under this condition, which is of course unpredictable, the lock-up transient is at its worst and the theoretical minimum lock-up time is not achievable. We must simply wait for the transient to die out.

The following expressions give the values of C_2 and C_3 which allow highest operating speeds for various band center frequencies. The minimum rate at which digital information may be detected without information loss due to the turn-on transient or output chatter is about 10 cycles per bit, corresponding to an information transfer rate of $f_O/10$ baud.

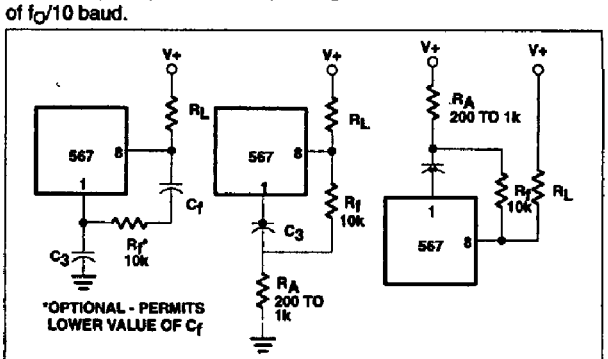


Figure 4. Chatter Prevention

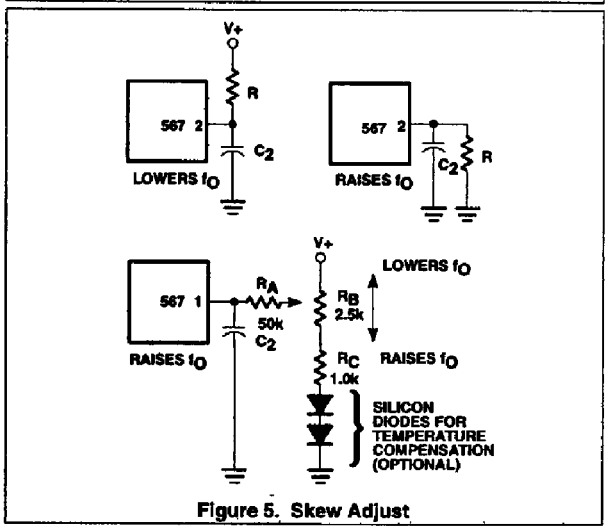


Figure 5. Skew Adjust

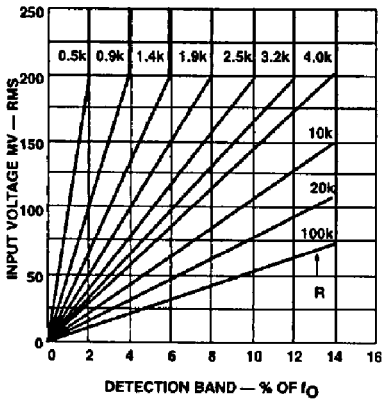
$$C_2 = \frac{130}{f_O}\ \mu F$$

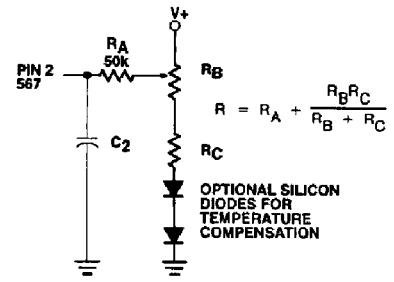
$$C_3 = \frac{260}{f_O}\ \mu F$$

In cases where turn-off time can be sacrificed to achieve fast turn-on, the optional sensitivity adjustment circuit can be used to move the quiescent C_3 voltage lower (closer to the threshold voltage). However, sensitivity to beat frequencies, noise and extraneous signals will be increased.

OPTIONAL CONTROLS (Figure 3)

The 567 has been designed so that, for most applications, no external adjustments are required. Certain applications, however, will be greatly facilitated if full advantage is taken of the added control possibilities available through the use of additional external components. In the diagrams given, typical values are suggested where applicable. For best results the resistors used, except where noted, should have the same temperature coefficient. Ideally, silicon diodes would be low-resistivity types, such as forward-biased transistor base-emitter junctions. However, ordinary low-voltage diodes should be adequate for most applications.





$$R = R_A + \frac{R_B R_C}{R_B + R_C}$$

NOTE:

$$\frac{130}{f_O}\left(\frac{10k + R}{R}\right) < C_2 < \frac{1300}{f_O}\left(\frac{10k + R}{R}\right)$$

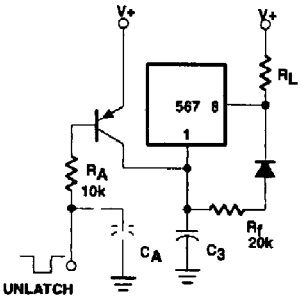
Adjust control for symmetry of detection band edges about f_O.

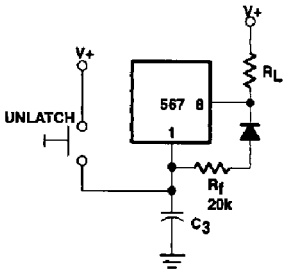
Figure 6. BW Reduction

SENSITIVITY ADJUSTMENT (Figure 3)

When operated as a very narrow-band detector (less than 8 percent), both C_2 and C_3 are made quite large in order to improve noise and out-band signal rejection. This will inevitably slow the response time. If, however, the output stage is biased closer to the threshold level, the turn-on time can be improved. This is accomplished by drawing additional current to terminal 1. Under this condition, the 567 will also give an output for lower-level signals (10mV or lower).

By adding current to terminal 1, the output stage is biased further away from the threshold voltage. This is most useful when, to obtain maximum operating speed, C_2 and C_3 are made very small. Normally, frequencies just outside the detection band could cause false outputs under this condition. By desensitizing the output stage, the out-band beat notes do not feed through to the output stage. Since the input level must





NOTE:
C_A prevents latch-up when power supply is turned on

Figure 7. Output Latching

CHATTER PREVENTION (Figure 4)

Chatter occurs in the output stage when C_3 is relatively small, so that the lock transient and the AC components at the quadrature phase detector (lock detector) output cause the output stage to move through its threshold more than once. Many loads, for example lamps and relays, will not respond to the chatter. However, logic may recognize the chatter as a series of outputs. By feeding the output stage output back to its input (Pin 1) the chatter can be eliminated. Three schemes for doing this are given in Figure 4. All operate by feeding the first output step (either on or off) back to the input, pushing the input past the threshold until the transient conditions are over. It is only necessary to assure that the feedback time constant is not so large as to prevent operation at the highest anticipated speed. Although chatter can always be eliminated by making C_3 large, the feedback circuit will enable faster operation of the 567 by allowing C_3 to be kept small. Note that if the feedback time constant is made quite large, a short burst at the input frequency can be stretched into a long output pulse. This may be useful to drive, for example, stepping relays.

DETECTION BAND CENTERING (OR SKEW) ADJUSTMENT (Figure 5)

When it is desired to alter the location of the detection band (corresponding to the loop capture range) within the lock range, the circuits shown above can be used. By moving the detection band to one edge of the range, for example, input signal variations will expand the detection band in only one direction. This may prove useful when a strong but undesirable signal is expected on one side or the other of the center frequency. Since R_B also alters the duty cycle slightly, this method may be used to obtain a precise duty cycle when the 567 is used as an oscillator.

ALTERNATE METHOD OF BANDWIDTH REDUCTION (Figure 6)

Although a large value of C_2 will reduce the bandwidth, it also reduces the loop damping so as to slow the circuit response time. This may be undesirable. Bandwidth can be reduced by reducing the loop gain. This scheme will improve damping and permit faster operation under narrow-band conditions. Note that the reduced impedance level at terminal 2 will require that a larger value of C_2 be used for a given filter cutoff
frequency. If more than three 567s are to be used, the network of R_B and R_C can be eliminated and the R_A resistors connected together. A capacitor between this junction and ground may be required to shunt high frequency components.

OUTPUT LATCHING (Figure 7)

To latch the output on after a signal is received, it is necessary to provide a feedback resistor around the output stage (between Pins 8 and 1). Pin 1 is pulled up to unlatch the output stage.

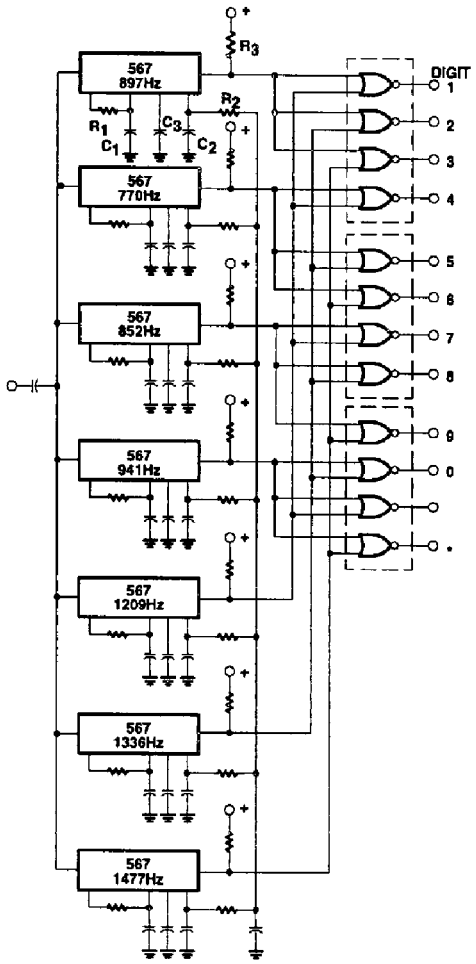
REDUCTION OF C1 VALUE

For precision very low-frequency applications, where the value of C_1 becomes large, an overall cost savings may be achieved by inserting a voltage-follower between the R_1 C_1 junction and Pin 6, so as to allow a higher value of R_1 and a lower value of C_1 for a given frequency.

PROGRAMMING

To change the center frequency, the value of R_1 can be changed with a mechanical or solid state switch, or additional C_1 capacitors may be added by grounding them through saturating NPN transistors.

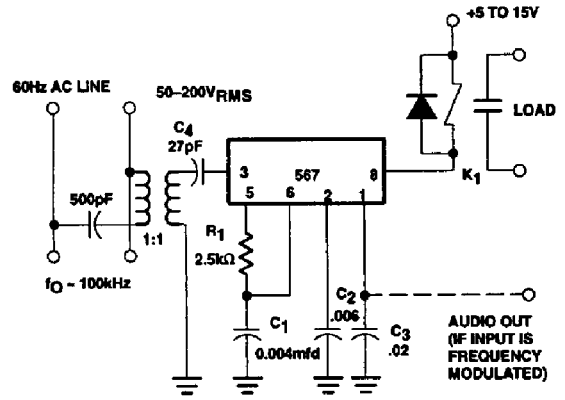
TYPICAL APPLICATIONS



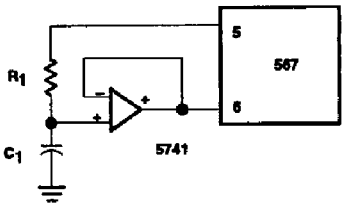
NOTES:
Component values (Typical)
R_1 = 26 8 to 15kΩ
R_2 = 24 7kΩ
R_3 = 20kΩ
C_1 = 0 10mF
C_2 = 1.0mF 5V
C_3 = 2.2mF 6V
C_4 = 250µF 6V

Touch-Tone® Decoder

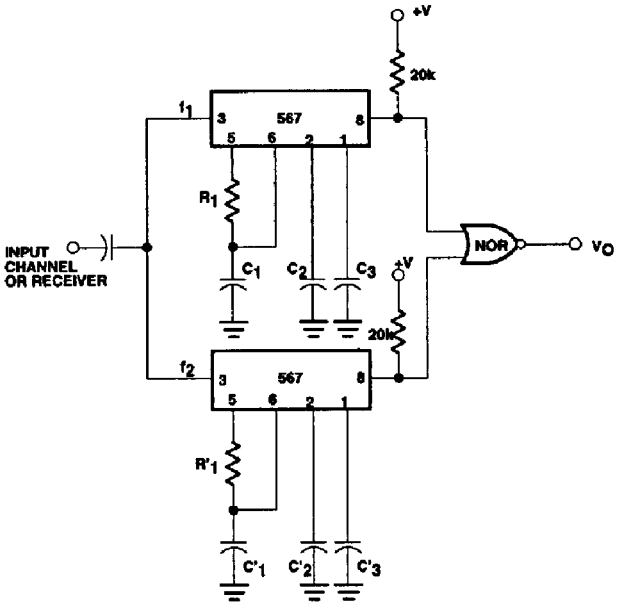
TYPICAL APPLICATIONS (Continued)



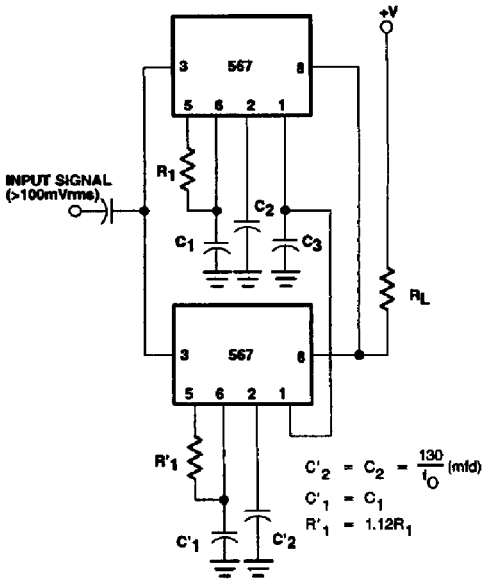
Carrier-Current Remote Control or Intercom



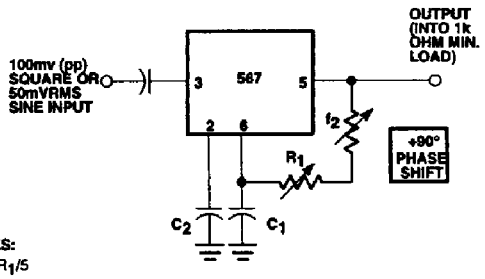
Precision VLF



Dual-Tone Decoder



24% Bandwidth Tone Decoder

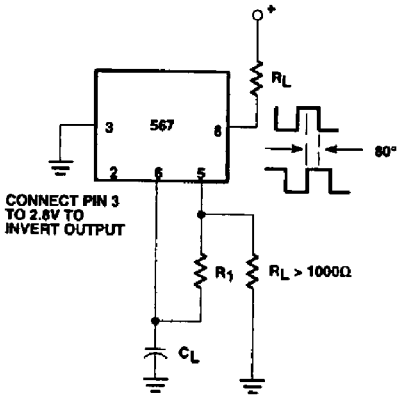


NOTES:
$R_2 = R_1/5$
Adjust R_1 so that $\phi = 90°$ with control midway.

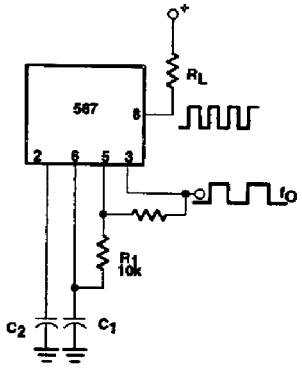
0° to 180° Phase Shifter

NOTES:
1. Resistor and capacitor values chosen for desired frequencies and bandwidth.
2. If C3 is made large so as to delay turn-on of the top 567, decoding of sequential (f_1 f_2) tones is possible.

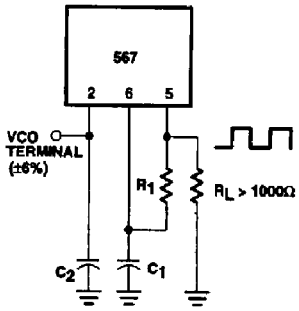
TYPICAL APPLICATIONS (Continued)



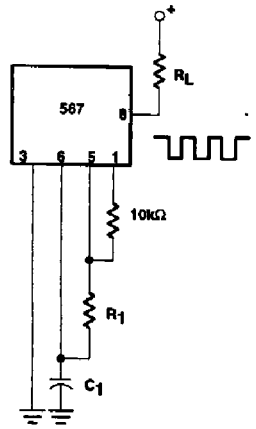
Oscillator With Quadrature Output



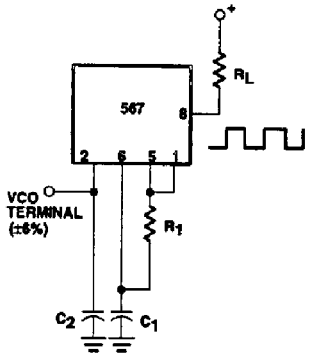
Oscillator With Double Frequency Output



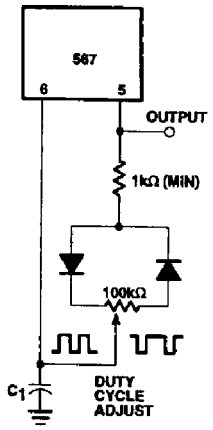
Precision Oscillator With 20ns Switching



Pulse Generator With 25% Duty Cycle



Precision Oscillator to Switch 100mA Loads

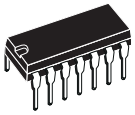


Pulse Generator

NE556
SA556 - SE556

GENERAL PURPOSE DUAL BIPOLAR TIMERS

- LOW TURN OFF TIME
- MAXIMUM OPERATING FREQUENCY GREATER THAN 500kHz
- TIMING FROM MICROSECONDS TO HOURS
- OPERATES IN BOTH ASTABLE AND MONOSTABLE MODES
- HIGH OUTPUT CURRENT CAN SOURCE OR SINK 200mA
- ADJUSTABLE DUTY CYCLE
- TTL COMPATIBLE
- TEMPERATURE STABILITY OF 0.005% PER°C



N
DIP14
(Plastic Package)

D
SO14
(Plastic Micropackage)

DESCRIPTION

The NE556 dual monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor.

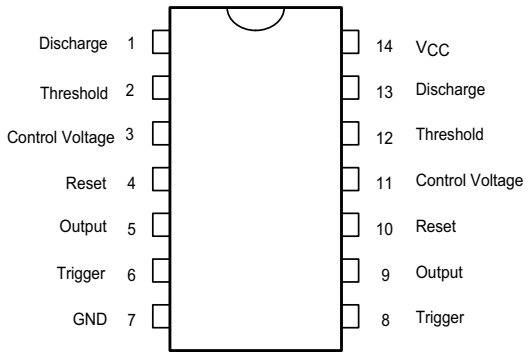
The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA.

ORDER CODE

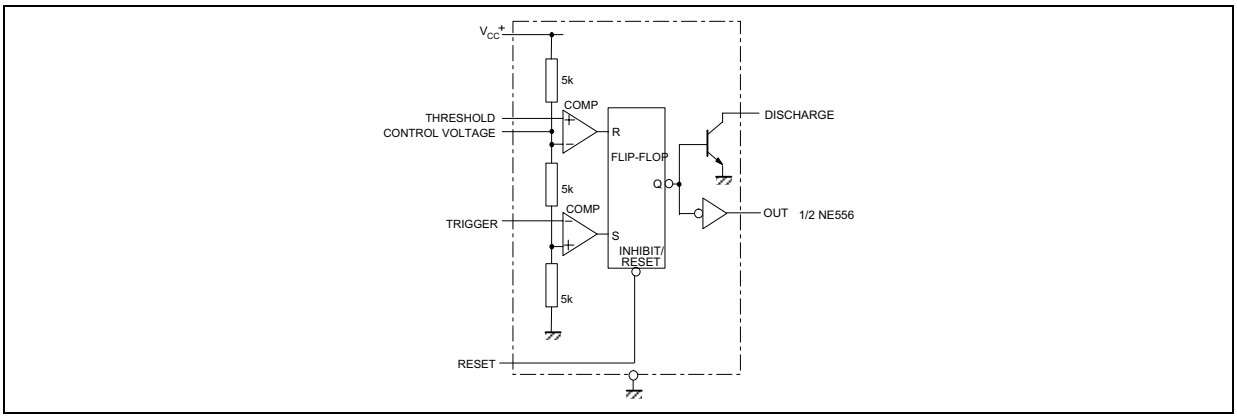
Part Number	Temperature Range	Package	
		N	D
NE556	0°C, 70°C	•	•
SA556	-40°C, 105°C	•	•
SE556	-55°C, 125°C	•	•

N = Dual in Line Package (DIP)
D = Small Outline Package (SO) - also available in Tape & Reel (DT)

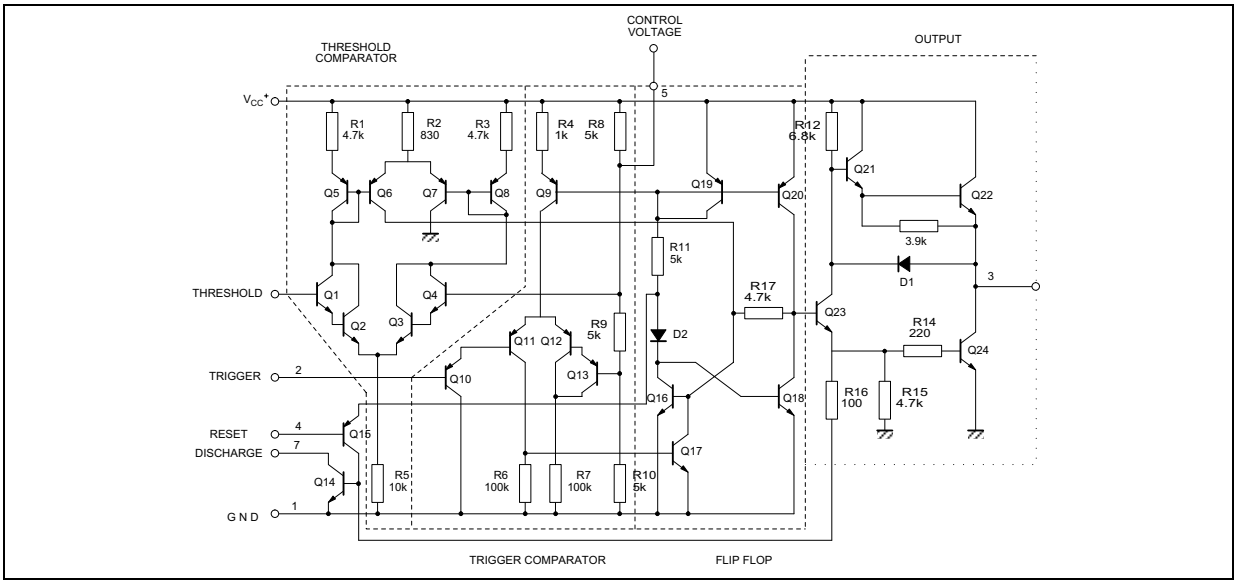
PIN CONNECTIONS (top view)



BLOCK DIAGRAM



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	18	V
T_j	Junction Temperature	150	°C
T_{stg}	Storage Temperature Range	-65 to 150	°C

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage NE556 SA556 SE556	4.5 to 16 4.5 to 16 4.5 to 18	V
V_{th}, V_{trig}, V_{cl}, V_{reset}	Maximum Input Voltage	V_{CC}	V
T_{oper}	Operating Free Air Temperature Range for NE556 for SA556 for SE556	 0 to 70 -40 to 105 -55 to 125	°C

ELECTRICAL CHARACTERISTICS T_{amb} = +25°C, V_{CC} = +5V to +15V (unless otherwise specified)

Symbol	Parameter	SE556			NE556 - SA556			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{CC}	Supply Current (RL ∞) - note [1] (2 timers) Low Stage V_{CC} = +5V V_{CC} = +15V High State V_{CC} = +5V		6 20 4	10 24		6 20 4	12 30	mA
	Timing Error (monostable) (R_A = 2k to 100kΩ, C = 0.1µF) Initial Accuracy - note [2] Drift with Temperature Drift with Supply Voltage		 0.5 30 0.05	 2 100 0.2		 1 50 0.1	 3 0.5	 % ppm/°C %/V
	Timing Error (astable) (R_A, R_B = 1kΩ to 100kΩ, C = 0.1µF, V_{CC} = +15V) Initial Accuracy - see note 2 Drift with Temperature Drift with Supply Voltage		 1.5 90 0.15			 2.25 150 0.3		 % ppm/°C %/V
V_{CL}	Control Voltage Level V_{CC} = +15V V_{CC} = +5V	 9.6 2.9	 10 3.33	 10.4 3.8	 9 2.6	 10 3.33	 11 4	 V
V_{th}	Threshold Voltage V_{CC} = +15V V_{CC} = +5V	 9.4 2.7	 10 3.33	 10.6 4	 8.8 2.4	 10 3.33	 11.2 4.2	 V
I_{th}	Threshold Current - note [3]		0.1	0.25		0.1	0.25	µA
V_{trig}	Trigger Voltage V_{CC} = +15V V_{CC} = +5V	 4.8 1.45	 5 1.67	 5.2 1.9	 4.5 1.1	 5 1.67	 5.6 2.2	 V
I_{trig}	Trigger Current (V_{trig} = 0V)		0.5	0.9		0.5	2.0	µA
V_{reset}	Reset Voltage [4]	0.4	0.7	1	0.4	0.7	1	V
I_{reset}	Reset Current V_{reset} = +0.4V V_{reset} = 0V		 0.1 0.4	 0.4 1		 0.1 0.4	 0.4 1.5	 mA
V_{OL}	Low Level Output Voltage V_{CC} = +15V $I_{O(sink)}$ = 10mA $I_{O(sink)}$ = 50mA $I_{O(sink)}$ = 100mA $I_{O(sink)}$ = 200mA V_{CC} = +5V $I_{O(sink)}$ = 8mA $I_{O(sink)}$ = 5mA		 0.1 0.4 2 2.5 0.1 0.05	 0.15 0.5 2.2 0.25 0.2		 0.1 0.4 2 2.5 0.3 0.25	 0.25 0.75 2.5 0.4 0.35	 V
V_{OH}	High Level Output Voltage V_{CC} = +15V $I_{O(sink)}$ = 200mA $I_{O(sink)}$ = 100mA V_{CC} = +5V $I_{O(sink)}$ = 100mA	 13 3	 12.5 13.3 3.3		 12.75 2.75	 12.5 13.3 3.3		 V
$I_{dis(off)}$	Discharge Pin Leakage Current (output high) (V_{dis} = 10V)		20	100		20	100	nA
$V_{dis(sat)}$	Discharge pin Saturation Voltage (output low) - note [5] V_{CC} = +15V, I_{dis} = 15mA V_{CC} = +5V, I_{dis} = 4.5mA		 180 80	 480 200		 180 80	 480 200	 mV
t_r t_f	Output rise Time Output Fall Time		100 100	200 200		100 100	300 300	ns
toff	Turn off Time - note [6] (V_{reset} = V_{CC})		0.5			0.5		µs

1. Supply current when output is high is typically 1mA less.
2. Tested at V_{CC} = +5V and V_{CC} = +15V
3. This will determine the maximum value of R_A + R_B for +15V operation the max total is R = 20MΩ and for 5V operation the max total R = 3.5MΩ
4. Specified with trigger input high
5. No protection against excessive pin 7 current is necessary, providing the package dissipation rating will not be exceeded
6. Time measured from a positive going input pulse from 0 to 0.8x Vcc into the threshold to the drop from high to low of the output trigger is tied to threshold.

Figure 1 : Minimum Pulse Width Required for Triggering

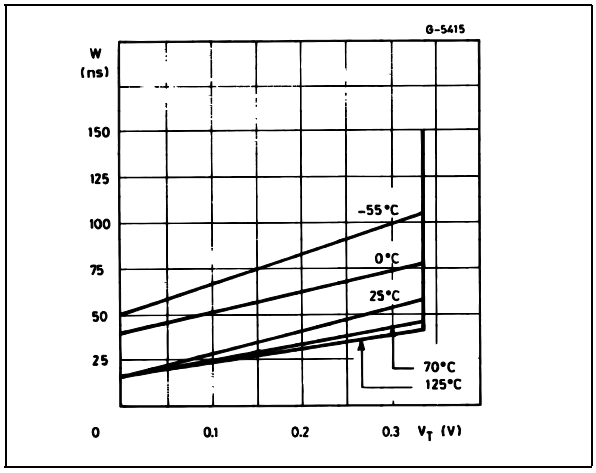


Figure 2 : Supply Current versus Supply Voltage

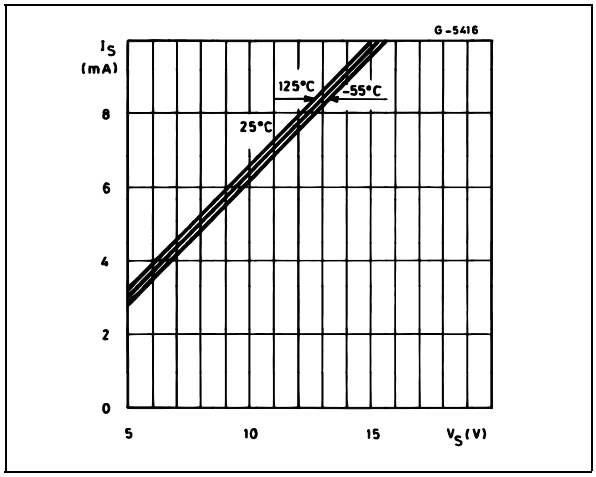


Figure 3 : Delay Time versus Temperature

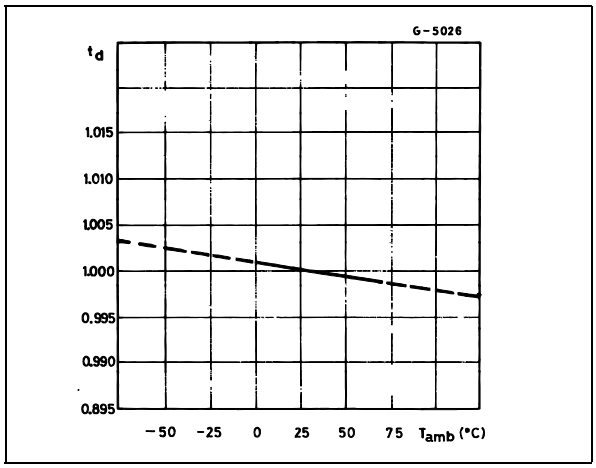


Figure 4 : Low Output Voltage versus Output Sink Current

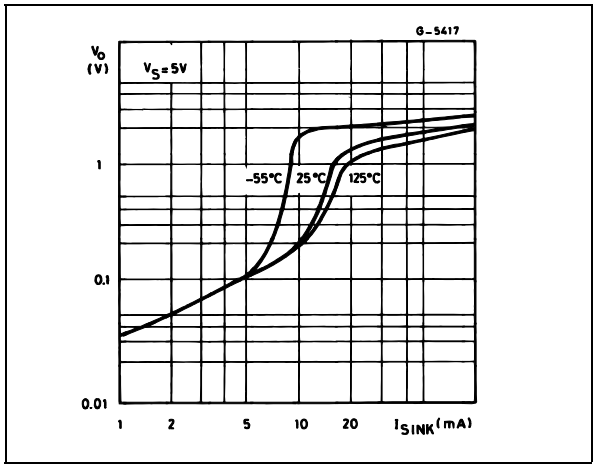


Figure 5 : Low Output Voltage versus Output Sink Current

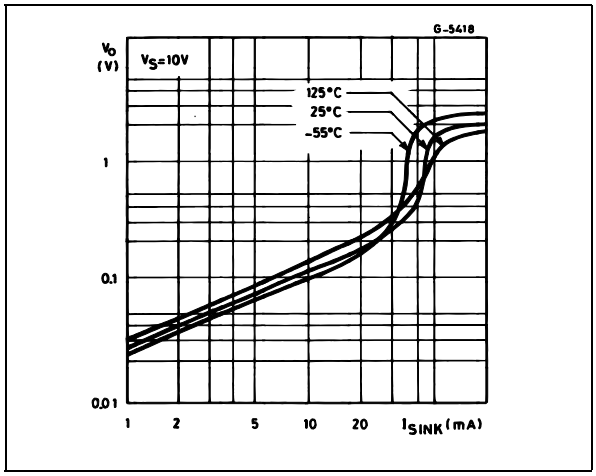


Figure 6 : Low Output Voltage versus Output Sink Current

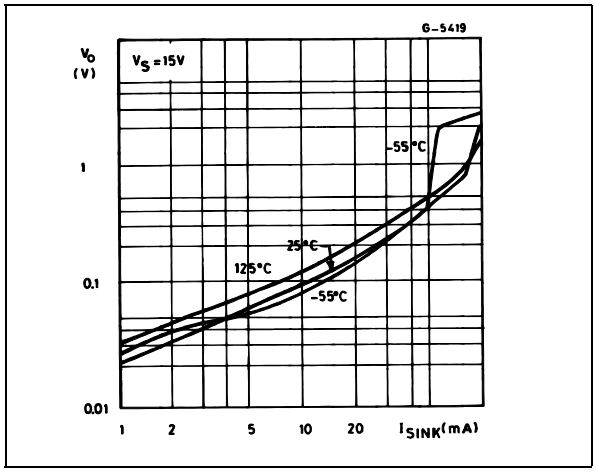


Figure 7 : High Output Voltage Drop versus Output

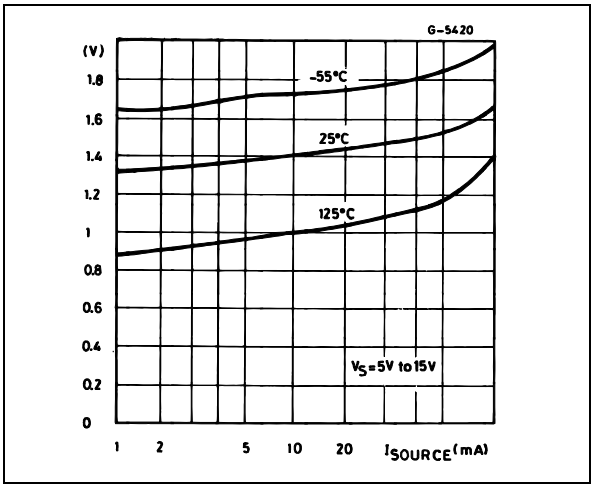


Figure 8 : Delay Time versus Supply Voltage

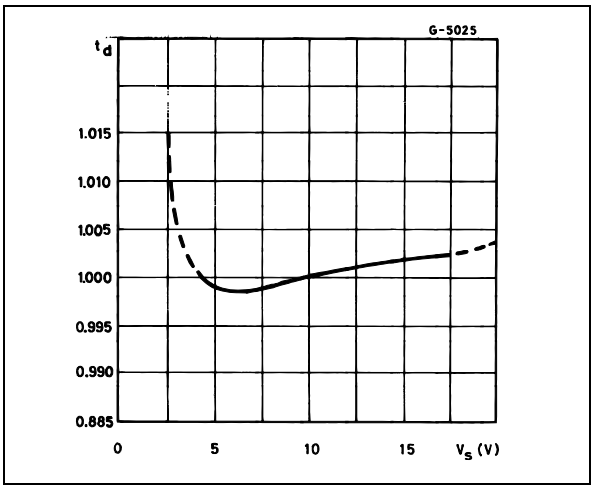
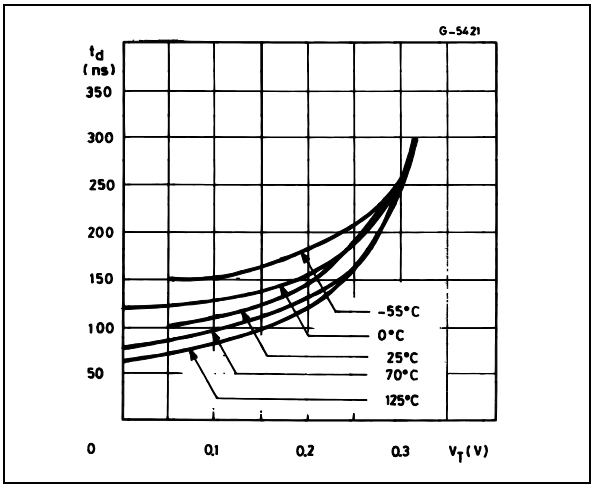
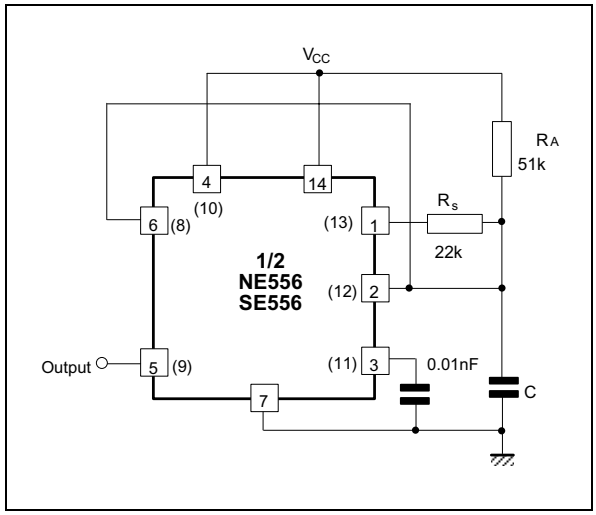


Figure 9 : Propagation Delay versus Voltage Level of Trigger Value



TYPICAL APPLICATION

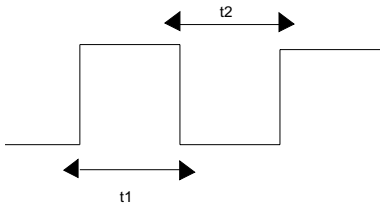
50% DUTY CYCLE OSCILLATOR



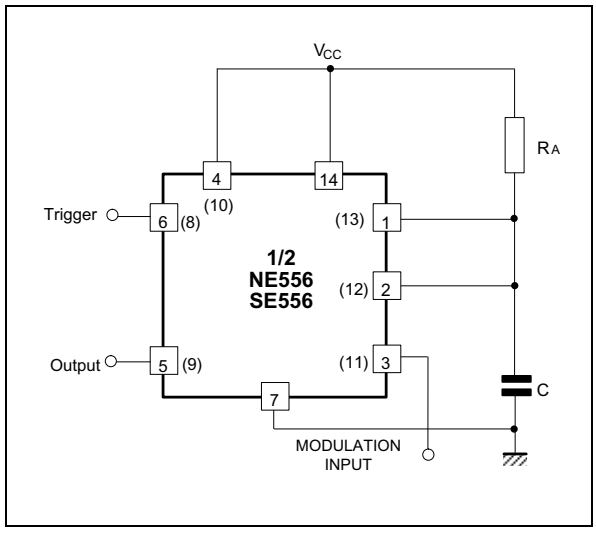
$t_1 = 0.693\ R_A.C$

$t2 = [(RARB)/(RA+RB)]CLn\left[\frac{RB-2RA}{2RB-RA}\right]$

$f = \frac{t1}{t1+t2}\ RB < \frac{1}{2}$ RA ti

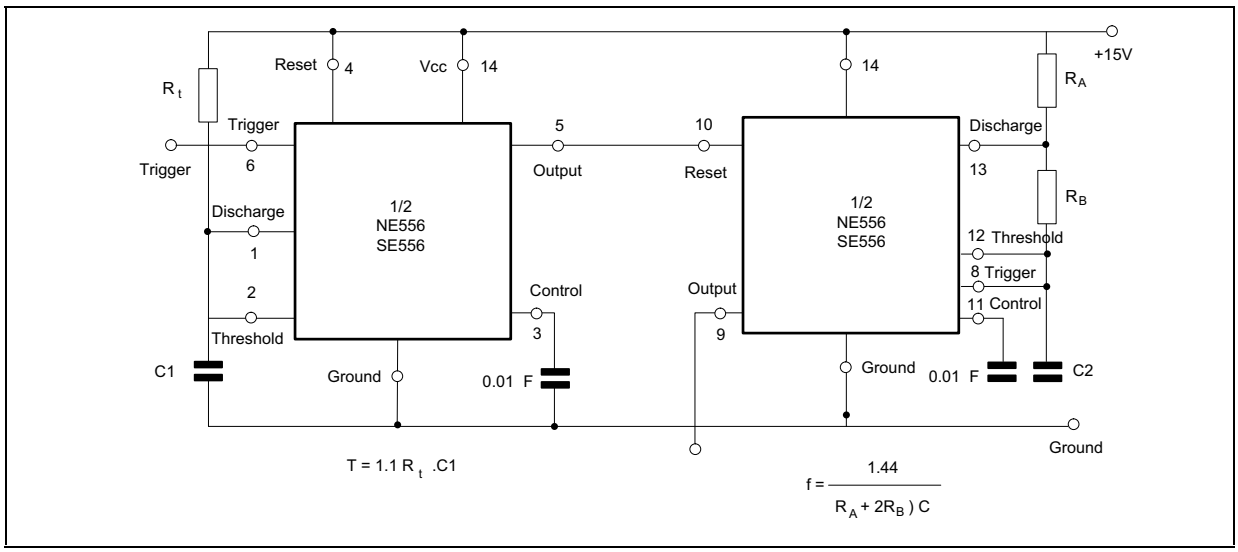


PULSE WIDTH MODULATOR

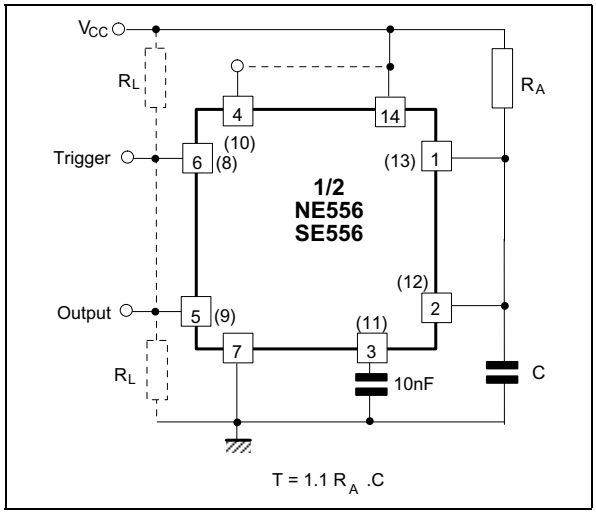


TONE BURST GENERATOR

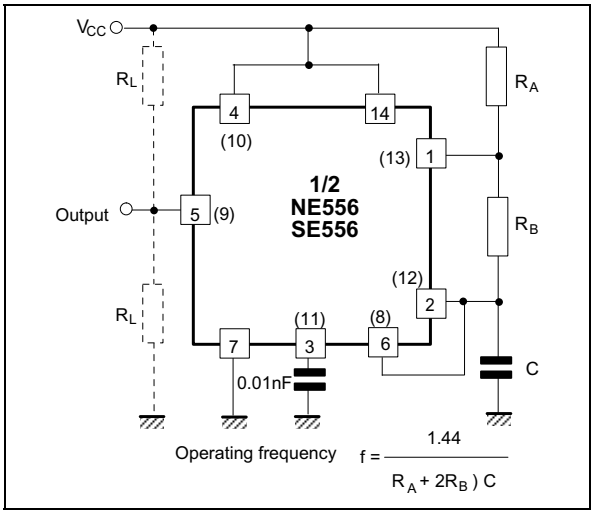
For a tone burst generator the first timer is used as a monostable and determines the tone duration when triggered by a positive pulse at pin 6. The second timer is enabled by the high output or the monostable. It is connected as an astable and determines the frequency of the tone.



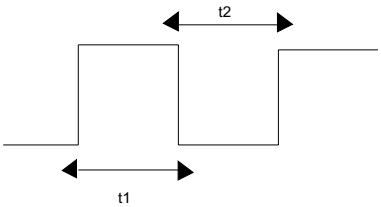
MONOSTABLE OPERATION



ASTABLE OPERATION



$t_1 = 0.693\ (R_A + R_B)\ C$ Output High
$t_2 = 0.693\ R_B C$ Output Low



National Semiconductor

January 1995

LM193/LM293/LM393/LM2903
Low Power Low Offset Voltage Dual Comparators

General Description

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

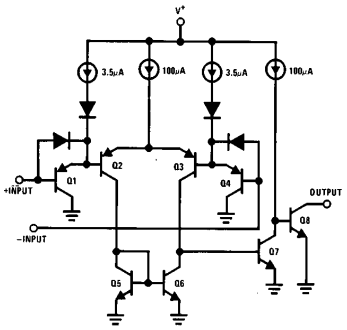
Advantages

- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near ground
- Compatible with all forms of logic
- Power drain suitable for battery operation

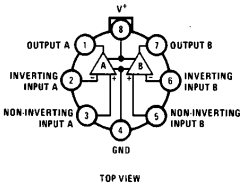
Features

- Wide supply
  - Voltage range 2.0V to 36V
  - single or dual supplies ±1.0V to ±18V
- Very low supply current drain (0.4 mA) — independent of supply voltage
- Low input biasing current 25 nA
- Low input offset current ±5 nA
  and maximum offset voltage ±3 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage, 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Schematic and Connection Diagrams

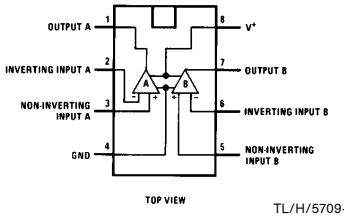


Metal Can Package



Order Number LM193H, LH193H/883*, LM193AH, LM193AH/883, LM293H, LM293AH, LM393H or LM393AH
See NS Package Number H08C

Dual-In-Line Package



TL/H/5709–1

Order Number LM193J/883*, LM193AJ/883, LM393J, LM393AJ, LM393M, LM2903M, LM393N, LM2903J or LM2903N
See NS Package Number J08A, M08A or N08E

*Also available per JM38510/11202

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
(Note 10)

Supply Voltage, V^+	36V
Differential Input Voltage (Note 8)	36V
Input Voltage	−0.3V to +36V
Input Current ($V_{IN} < -0.3V$) (Note 3)	50 mA
Power Dissipation (Note 1)	
Molded DIP	780 mW
Metal Can	660 mW
Small Outline Package	510 mW
Output Short-Circuit to Ground (Note 2)	Continuous
Operating Temperature Range	
LM393/LM393A	0°C to +70°C
LM293/LM293A	−25°C to +85°C
LM193/LM193A	−55°C to +125°C
LM2903	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 ''Surface Mounting Methods and Their Effect on Product Reliability'' for other methods of soldering surface mount devices.

ESD rating (1.5 kΩ in series with 100 pF) 1300V

Electrical Characteristics ($V^+ = 5V$, $T_A = 25°C$, unless otherwise stated)

Parameter	Conditions		LM193A			LM293A, LM393A			LM193			LM293, LM393			LM2903			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)			1.0	2.0		1.0	2.0		1.0	5.0		1.0	5.0		2.0	7.0	mV
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with Output In Linear Range, $V_{CM} = 0V$ (Note 5)			25	100		25	250		25	100		25	250		25	250	nA
Input Offset Current	$I_{IN}(+) - I_{IN}(-)$ $V_{CM} = 0V$			3.0	25		5.0	50		3.0	25		5.0	50		5.0	50	nA
Input Common Mode Voltage Range	$V^+ = 30V$ (Note 6)		0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V
Supply Current	$R_L = \infty$	$V^+ = 5V$		0.4	1		0.4	1		0.4	1		0.4	1		0.4	1.0	mA
		$V^+ = 36V$		1	2.5		1	2.5		1	2.5		1	2.5		1	2.5	mA
Voltage Gain	$R_L \geq 15\ k\Omega$, $V^+ = 15V$, $V_O = 1V$ to 11V		50	200		50	200		50	200		50	200		25	100		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, $V_{REF} = 1.4V$, $V_{RL} = 5V$, $R_L = 5.1\ k\Omega$			300			300			300			300			300		ns
Response Time	$V_{RL} = 5V$, $R_L = 5.1\ k\Omega$ (Note 7)			1.3			1.3			1.3			1.3			1.5		μs
Output Sink Current	$V_{IN}(-) = 1V$, $V_{IN}(+) = 0$, $V_O \leq 1.5V$		6.0	16		6.0	16		6.0	16		6.0	16		6.0	16		mA
Saturation Voltage	$V_{IN}(-) = 1V$, $V_{IN}(+) = 0$, $I_{SINK} \leq 4$ mA			250	400		250	400		250	400		250	400		250	400	mV
Output Leakage Current	$V_{IN}(-) = 0$, $V_{IN}(+) = 1V$, $V_O = 5V$			0.1			0.1			0.1			0.1			0.1		nA

Electrical Characteristics ($V^+ = 5V$) (Note 4)

Parameter	Conditions	LM193A			LM293A, LM393A			LM193			LM293, LM393			LM2903			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)			4.0			4.0			9			9		9	15	mV
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$			100			150			100			150		50	200	nA
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with Output in Linear Range, $V_{CM} = 0V$ (Note 5)			300			400			300			400		200	500	nA
Input Common Mode Voltage Range	$V^+ = 30V$ (Note 6)	0		$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$	V
Saturation Voltage	$V_{IN}(-) = 1V$, $V_{IN}(+) = 0$, $I_{SINK} \leq 4$ mA			700			700			700			700		400	700	mV
Output Leakage Current	$V_{IN}(-) = 0$, $V_{IN(+)} = 1V$, $V_O = 30V$			1.0			1.0			1.0			1.0			1.0	μA
Differential Input Voltage	Keep All V_{IN}'s $\geq 0V$ (or V^-, if Used), (Note 8)			36			36			36			36			36	V

Note 1: For operating at high temperatures, the LM393/LM393A and LM2903 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 170°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM193/LM193A/LM293/LM293A must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3V$.

Note 4: These specifications are limited to $-55°C \leq T_A \leq +125°C$, for the LM193/LM193A, With the LM293/LM293A all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$ and the LM393/LM393A temperature specifications are limited to $0°C \leq T_A \leq +70°C$. The LM2903 is limited to $-40°C \leq T_A \leq +85°C$.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$ at 25°C, but either or both inputs can go to 36V without damage, independent of the magnitude of V^+.

Note 7: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

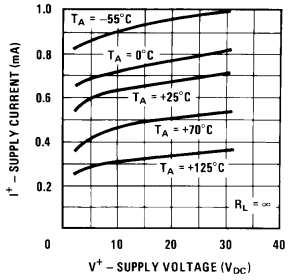
Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3V$ (or 0.3V below the magnitude of the negative power supply, if used).

Note 9: At output switch point, $V_O \cong 1.4V$, $R_S = 0\Omega$ with V^+ from 5V to 30V; and over the full input common-mode range (0V to $V^+ - 1.5V$), at 25°C.

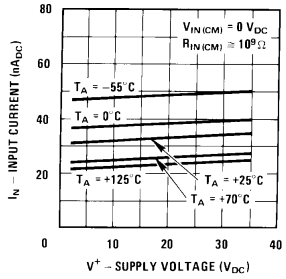
Note 10: Refer to RETS193AX for LM193AH military specifications and to RETS193X for LM193H military specifications.

Typical Performance Characteristics LM193/LM293/LM393, LM193A/LM293A/LM393A

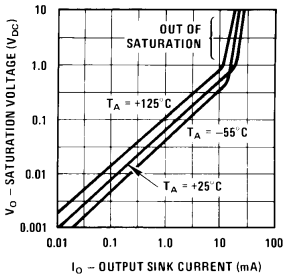
Supply Current



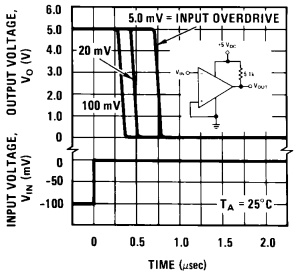
Input Current



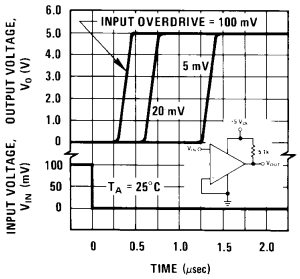
Output Saturation Voltage



Response Time for Various Input Overdrives—Negative Transition



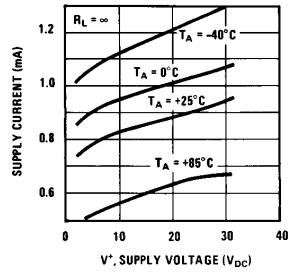
Response Time for Various Input Overdrives—Positive Transition



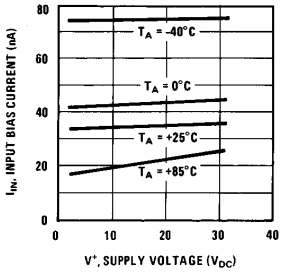
TL/H/5709–3

Typical Performance Characteristics LM2903

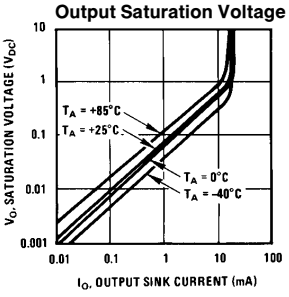
Supply Current



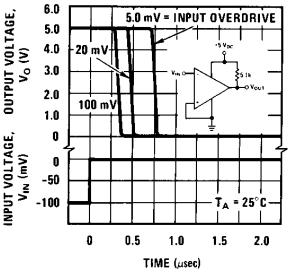
Input Current



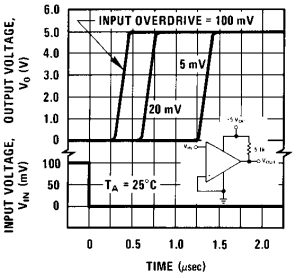
Output Saturation Voltage



Response Time for Various Input Overdrives—Negative Transition



Response Time for Various Input Overdrives—Positive Transition



TL/H/5709–4

National Semiconductor

January 1995

LM193/LM293/LM393/LM2903
Low Power Low Offset Voltage Dual Comparators

General Description

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

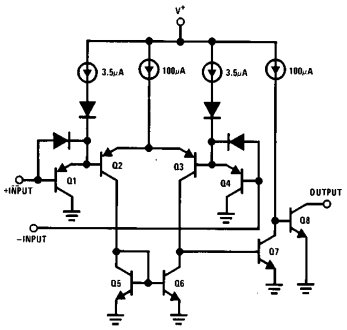
Advantages

- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near ground
- Compatible with all forms of logic
- Power drain suitable for battery operation

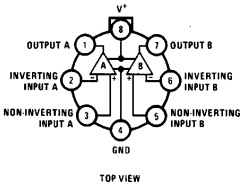
Features

- Wide supply
  - Voltage range 2.0V to 36V
  - single or dual supplies ±1.0V to ±18V
- Very low supply current drain (0.4 mA) — independent of supply voltage
- Low input biasing current 25 nA
- Low input offset current ±5 nA
  and maximum offset voltage ±3 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage, 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Schematic and Connection Diagrams

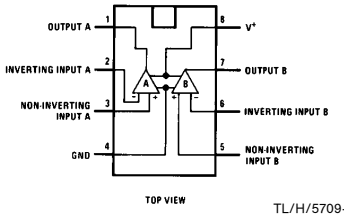


Metal Can Package



Order Number LM193H, LH193H/883*, LM193AH, LM193AH/883, LM293H, LM293AH, LM393H or LM393AH
See NS Package Number H08C

Dual-In-Line Package



TL/H/5709–1

Order Number LM193J/883*, LM193AJ/883, LM393J, LM393AJ, LM393M, LM2903M, LM393N, LM2903J or LM2903N
See NS Package Number J08A, M08A or N08E

*Also available per JM38510/11202

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
(Note 10)

Supply Voltage, V^+	36V
Differential Input Voltage (Note 8)	36V
Input Voltage	−0.3V to +36V
Input Current ($V_{IN} < -0.3V$) (Note 3)	50 mA
Power Dissipation (Note 1)	
Molded DIP	780 mW
Metal Can	660 mW
Small Outline Package	510 mW
Output Short-Circuit to Ground (Note 2)	Continuous
Operating Temperature Range	
LM393/LM393A	0°C to +70°C
LM293/LM293A	−25°C to +85°C
LM193/LM193A	−55°C to +125°C
LM2903	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 ''Surface Mounting Methods and Their Effect on Product Reliability'' for other methods of soldering surface mount devices.

ESD rating (1.5 kΩ in series with 100 pF) 1300V

Electrical Characteristics ($V^+ = 5V$, $T_A = 25°C$, unless otherwise stated)

Parameter	Conditions		LM193A			LM293A, LM393A			LM193			LM293, LM393			LM2903			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)			1.0	2.0		1.0	2.0		1.0	5.0		1.0	5.0		2.0	7.0	mV
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with Output In Linear Range, $V_{CM} = 0V$ (Note 5)			25	100		25	250		25	100		25	250		25	250	nA
Input Offset Current	$I_{IN}(+) - I_{IN}(-)$ $V_{CM} = 0V$			3.0	25		5.0	50		3.0	25		5.0	50		5.0	50	nA
Input Common Mode Voltage Range	$V^+ = 30V$ (Note 6)		0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V
Supply Current	$R_L = \infty$	$V^+ = 5V$		0.4	1		0.4	1		0.4	1		0.4	1		0.4	1.0	mA
		$V^+ = 36V$		1	2.5		1	2.5		1	2.5		1	2.5		1	2.5	mA
Voltage Gain	$R_L \geq 15\ k\Omega$, $V^+ = 15V$, $V_O = 1V$ to 11V		50	200		50	200		50	200		50	200		25	100		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, $V_{REF} = 1.4V$, $V_{RL} = 5V$, $R_L = 5.1\ k\Omega$			300			300			300			300			300		ns
Response Time	$V_{RL} = 5V$, $R_L = 5.1\ k\Omega$ (Note 7)			1.3			1.3			1.3			1.3			1.5		μs
Output Sink Current	$V_{IN}(-) = 1V$, $V_{IN}(+) = 0$, $V_O \leq 1.5V$		6.0	16		6.0	16		6.0	16		6.0	16		6.0	16		mA
Saturation Voltage	$V_{IN}(-) = 1V$, $V_{IN}(+) = 0$, $I_{SINK} \leq 4$ mA			250	400		250	400		250	400		250	400		250	400	mV
Output Leakage Current	$V_{IN}(-) = 0$, $V_{IN}(+) = 1V$, $V_O = 5V$			0.1			0.1			0.1			0.1			0.1		nA

Electrical Characteristics ($V^+ = 5V$) (Note 4)

Parameter	Conditions	LM193A			LM293A, LM393A			LM193			LM293, LM393			LM2903			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)			4.0			4.0			9			9		9	15	mV
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$			100			150			100			150		50	200	nA
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with Output in Linear Range, $V_{CM} = 0V$ (Note 5)			300			400			300			400		200	500	nA
Input Common Mode Voltage Range	$V^+ = 30V$ (Note 6)	0		$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$	V
Saturation Voltage	$V_{IN}(-) = 1V$, $V_{IN}(+) = 0$, $I_{SINK} \leq 4$ mA			700			700			700			700		400	700	mV
Output Leakage Current	$V_{IN}(-) = 0$, $V_{IN(+)} = 1V$, $V_O = 30V$			1.0			1.0			1.0			1.0			1.0	μA
Differential Input Voltage	Keep All V_{IN}'s $\geq 0V$ (or V^-, if Used), (Note 8)			36			36			36			36			36	V

Note 1: For operating at high temperatures, the LM393/LM393A and LM2903 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 170°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM193/LM193A/LM293/LM293A must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3V$.

Note 4: These specifications are limited to $-55°C \leq T_A \leq +125°C$, for the LM193/LM193A, With the LM293/LM293A all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$ and the LM393/LM393A temperature specifications are limited to $0°C \leq T_A \leq +70°C$. The LM2903 is limited to $-40°C \leq T_A \leq +85°C$.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$ at 25°C, but either or both inputs can go to 36V without damage, independent of the magnitude of V^+.

Note 7: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

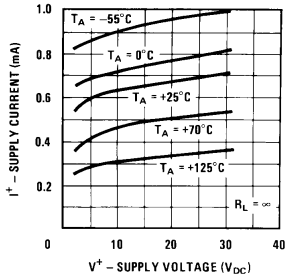
Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3V$ (or 0.3V below the magnitude of the negative power supply, if used).

Note 9: At output switch point, $V_O \cong 1.4V$, $R_S = 0\Omega$ with V^+ from 5V to 30V; and over the full input common-mode range (0V to $V^+ - 1.5V$), at 25°C.

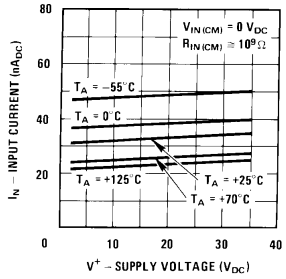
Note 10: Refer to RETS193AX for LM193AH military specifications and to RETS193X for LM193H military specifications.

Typical Performance Characteristics LM193/LM293/LM393, LM193A/LM293A/LM393A

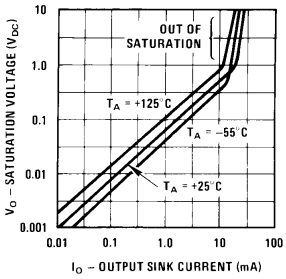
Supply Current



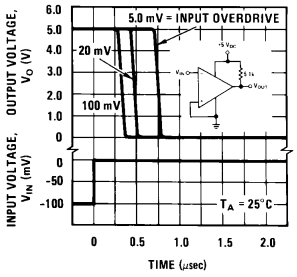
Input Current



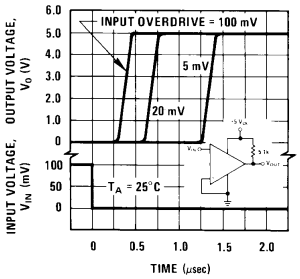
Output Saturation Voltage



Response Time for Various Input Overdrives—Negative Transition



Response Time for Various Input Overdrives—Positive Transition



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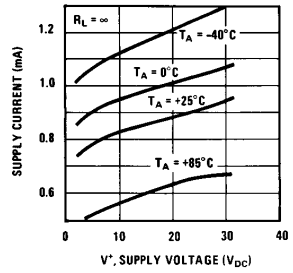
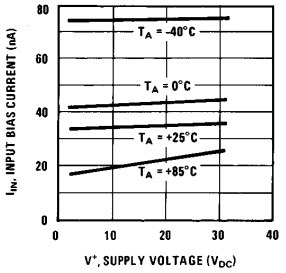
Typical Performance Characteristics LM2903

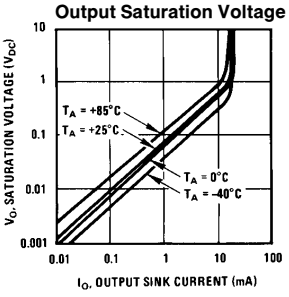
Supply Current



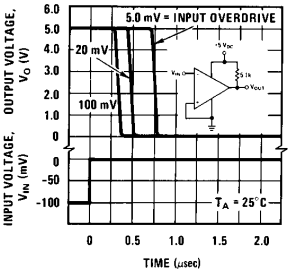
Input Current



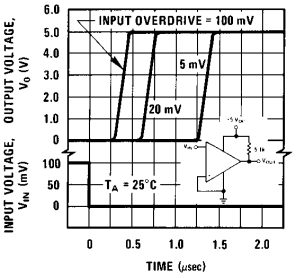
Output Saturation Voltage



Response Time for Various Input Overdrives—Negative Transition



Response Time for Various Input Overdrives—Positive Transition



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Application Hints

The LM193 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator change states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to $< 10\ k\Omega$ reduces the feedback signal levels and finally, adding even a small amount (1.0 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

The bias network of the LM193 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2.0 V_{DC} to 30 V_{DC}.

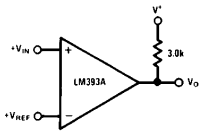
It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device (see Note 8). Protection should be provided to prevent the input voltages from going negative more than $-0.3\ V_{DC}$ (at 25°C). An input clamp diode can be used as shown in the applications section.

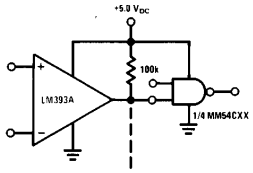
The output of the LM193 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM193 package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω r_{SAT} of the output transistor. The low offset voltage of the output transistor (1.0 mV) allows the output to clamp essentially to ground level for small load currents.

Typical Applications ($V^+ = 5.0\ V_{DC}$)

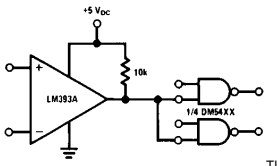
Basic Comparator



Driving CMOS



Driving TTL



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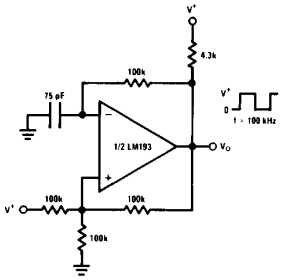
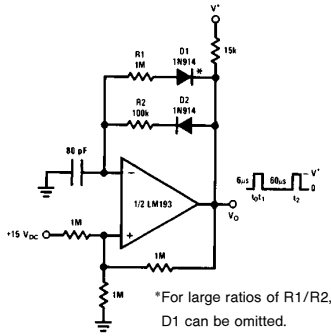
Typical Applications (Continued)

Squarewave Oscillator

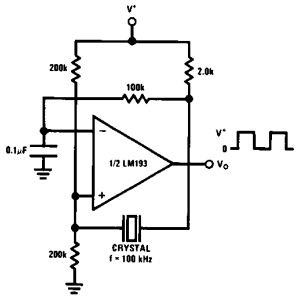


Pulse Generator

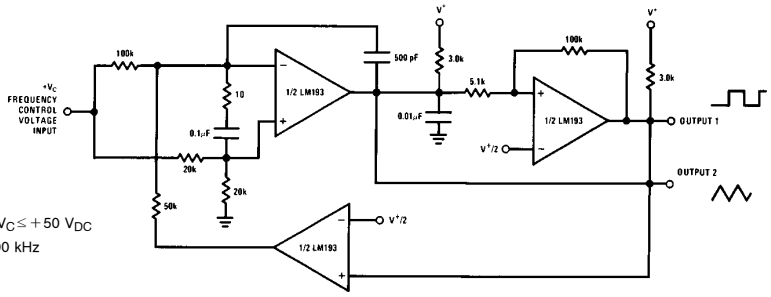


*For large ratios of R1/R2, D1 can be omitted.

Crystal Controlled Oscillator



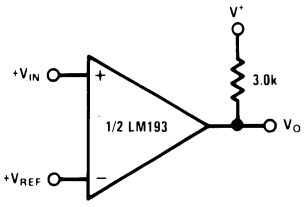
Two-Decade High-Frequency VCO



V* = +30 V_{DC}
+250 $mV_{DC} \leq V_C \leq +50\ V_{DC}$
700 Hz $\leq f_O \leq$ 100 kHz

TL/H/5709–5

Basic Comparator



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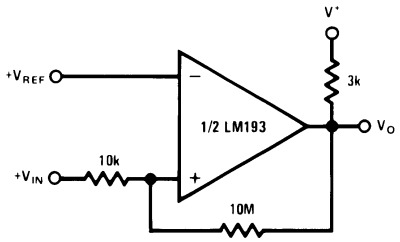
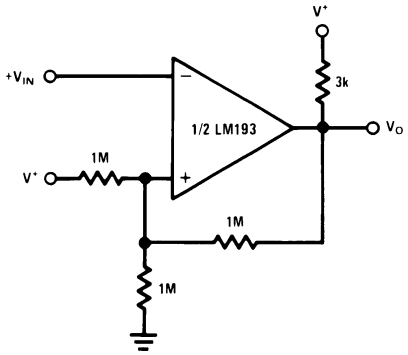
Non-Inverting Comparator with Hysteresis



TL/H/5709–9

Inverting Comparator with Hysteresis



TL/H/5709–10

SGS-THOMSON MICROELECTRONICS

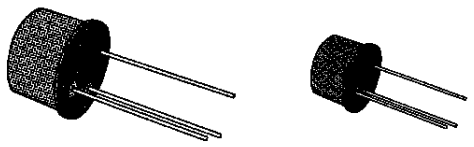
2N2218-2N2219
2N2221-2N2222

HIGH-SPEED SWITCHES

DESCRIPTION

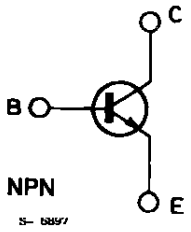
The 2N2218, 2N2219, 2N2221 and 2N2222 are silicon planar epitaxial NPN transistors in Jedec TO-39 (for 2N2218 and 2N2219) and in Jedec TO-18 (for 2N2221 and 2N2222) metal cases. They are designed for high-speed switching applications at collector currents up to 500 mA, and feature useful current gain over a wide range of collector current, low leakage currents and low saturation voltages.

2N2218/2N2219 approved to CECC 50002-100, 2N2221/2N2222 approved to CECC 50002-101 available on request.



TO-39 TO-18

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-base Voltage (I_E = 0)	60	V
V_{CEO}	Collector-emitter Voltage (I_B = 0)	30	V
V_{EBO}	Emitter-base Voltage (I_C = 0)	5	V
I_C	Collector Current	0.8	A
P_{tot}	Total Power Dissipation at $T_{amb} \leq 25$ °C		
	for **2N2218** and **2N2219**	0.8	W
	for **2N2221** and **2N2222**	0.5	W
	at $T_{case} \leq 25$ °C		
	for **2N2218** and **2N2219**	3	W
	for **2N2221** and **2N2222**	1.8	W
T_{stg}	Storage Temperature	– 65 to 200	°C
T_j	Junction Temperature	175	°C

THERMAL DATA

			2N2218 2N2219	2N2221 2N2222
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	50 °C/W	83.3 °C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	187.5 °C/W	300 °C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector Cutoff Current (I_E = 0)	V_{CB} = 50 V V_{CB} = 50 V T_{amb} = 150 °C			10 10	nA µA
I_{EBO}	Emitter Cutoff Current (I_C = 0)	V_{EB} = 3 V			10	nA
$V_{(BR)\ CBO}$	Colllector-base Breakdown Voltage (I_E = 0)	I_C = 10 µA	60			V
$V_{(BR)CEO}$*	Collector-emitter Breakdown Voltage (I_B = 0)	I_C = 10 mA	30			V
$V_{(BR)\ EBO}$	Emittter-base Breakdown Voltage (I_C = 0)	I_E = 10 µA	5			V
$V_{CE\ (sat)}$*	Collector-emitter Saturation Voltage	I_C = 150 mA I_B = 15 mA I_C = 500 mA I_B = 50 mA			0.4 1.6	V V
$V_{BE\ (sat)}$*	Base-emitter Saturation Voltage	I_C = 150 mA I_B = 15 mA I_C = 500 mA I_B = 50 mA			1.3 2.6	V V
h_{FE}*	DC Current Gain	for **2N2218** and **2N2221** I_C = 0.1 mA V_{CE} = 10 V I_C = 1 mA V_{CE} = 10 V I_C = 10 mA V_{CE} = 10 V I_C = 150 mA V_{CE} = 10 V I_C = 500 mA V_{CE} = 10 V I_C = 150 mA V_{CE} = 1 V for **2N2219** and **2N2222** I_C = 0.1 mA V_{CE} = 10 V I_C = 1 mA V_{CE} = 10 V I_C = 10 mA V_{CE} = 10 V I_C = 150 mA V_{CE} = 10 V I_C = 500 mA V_{CE} = 10 V I_C = 150 mA V_{CE} = 1 V	 20 25 35 40 20 20 35 50 75 100 30 50		 120 300 	
f_T	Transition Frequency	I_C = 20 mA V_{CE} = 20 V f = 100 MHz	250			MHz
C_{CBO}	Collector-base Capacitance	I_E = 0 V_{CB} = 10 V f = 100 kHz			8	pF
$R_{e(hie)}$	Real Part of Input Impedance	I_C = 20 mA V_{CE} = 20 V f = 300 MHz			60	Ω

* Pulsed : pulse duration = 300 µs, duty cycle = 1 %.

Table 3-2 Instruction Set (Sheet 1 of 6)

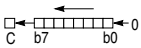
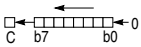
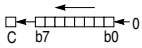
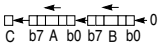
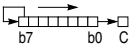
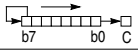
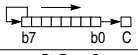
Mnemonic	Operation	Description	Addressing Mode	Instruction			Condition Codes							
				Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C
ABA	Add Accumulators	A + B ⇒ A	INH	1B	—	2	—	—	Δ	—	Δ	Δ	Δ	Δ
ABX	Add B to X	IX + (00 : B) ⇒ IX	INH	3A	—	3	—	—	—	—	—	—	—	—
ABY	Add B to Y	IY + (00 : B) ⇒ IY	INH	18 3A	—	4	—	—	—	—	—	—	—	—
ADCA (opr)	Add with Carry to A	A + M + C ⇒ A	A IMM	89	ii	2	—	—	Δ	—	Δ	Δ	Δ	Δ
			A DIR	99	dd	3								
			A EXT	B9	hh ll	4								
			A IND,X	A9	ff	4								
			A IND,Y	18 A9	ff	5								
ADCB (opr)	Add with Carry to B	B + M + C ⇒ B	B IMM	C9	ii	2	—	—	Δ	—	Δ	Δ	Δ	Δ
			B DIR	D9	dd	3								
			B EXT	F9	hh ll	4								
			B IND,X	E9	ff	4								
			B IND,Y	18 E9	ff	5								
ADDA (opr)	Add Memory to A	A + M ⇒ A	A IMM	8B	ii	2	—	—	Δ	—	Δ	Δ	Δ	Δ
			A DIR	9B	dd	3								
			A EXT	BB	hh ll	4								
			A IND,X	AB	ff	4								
			A IND,Y	18 AB	ff	5								
ADDB (opr)	Add Memory to B	B + M ⇒ B	B IMM	CB	ii	2	—	—	Δ	—	Δ	Δ	Δ	Δ
			B DIR	DB	dd	3								
			B EXT	FB	hh ll	4								
			B IND,X	EB	ff	4								
			B IND,Y	18 EB	ff	5								
ADDD (opr)	Add 16-Bit to D	D + (M : M + 1) ⇒ D	IMM	C3	jj kk	4	—	—	—	—	Δ	Δ	Δ	Δ
			DIR	D3	dd	5								
			EXT	F3	hh ll	6								
			IND,X	E3	ff	6								
			IND,Y	18 E3	ff	7								
ANDA (opr)	AND A with Memory	A • M ⇒ A	A IMM	84	ii	2	—	—	—	—	Δ	Δ	0	—
			A DIR	94	dd	3								
			A EXT	B4	hh ll	4								
			A IND,X	A4	ff	4								
			A IND,Y	18 A4	ff	5								
ANDB (opr)	AND B with Memory	B • M ⇒ B	B IMM	C4	ii	2	—	—	—	—	Δ	Δ	0	—
			B DIR	D4	dd	3								
			B EXT	F4	hh ll	4								
			B IND,X	E4	ff	4								
			B IND,Y	18 E4	ff	5								
ASL (opr)	Arithmetic Shift Left		EXT	78	hh ll	6	—	—	—	—	Δ	Δ	Δ	Δ
			IND,X	68	ff	6								
			IND,Y	18 68	ff	7								
ASLA	Arithmetic Shift Left A		A INH	48	—	2	—	—	—	—	Δ	Δ	Δ	Δ
ASLB	Arithmetic Shift Left B		B INH	58	—	2	—	—	—	—	Δ	Δ	Δ	Δ
ASLD	Arithmetic Shift Left D		INH	05	—	3	—	—	—	—	Δ	Δ	Δ	Δ
ASR	Arithmetic Shift Right		EXT	77	hh ll	6	—	—	—	—	Δ	Δ	Δ	Δ
			IND,X	67	ff	6								
			IND,Y	18 67	ff	7								
ASRA	Arithmetic Shift Right A		A INH	47	—	2	—	—	—	—	Δ	Δ	Δ	Δ
ASRB	Arithmetic Shift Right B		B INH	57	—	2	—	—	—	—	Δ	Δ	Δ	Δ
BCC (rel)	Branch if Carry Clear	? C = 0	REL	24	rr	3	—	—	—	—	—	—	—	—
BCLR (opr) (msk)	Clear Bit(s)	M • (mm) ⇒ M	DIR	15	dd mm	6	—	—	—	—	Δ	Δ	0	—
			IND,X	1D	ff mm	7								
			IND,Y	18 1D	ff mm	8								
BCS (rel)	Branch if Carry Set	? C = 1	REL	25	rr	3	—	—	—	—	—	—	—	—
BEQ (rel)	Branch if = Zero	? Z = 1	REL	27	rr	3	—	—	—	—	—	—	—	—
BGE (rel)	Branch if Δ Zero	? N ⊕ V = 0	REL	2C	rr	3	—	—	—	—	—	—	—	—

Table 3-2 Instruction Set (Sheet 2 of 6)

Mnemonic	Operation	Description	Addressing Mode	Instruction			Condition Codes							
				Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C
BGT (rel)	Branch if > Zero	? Z + (N ⊕ V) = 0	REL	2E	rr	3	—	—	—	—	—	—	—	—
BHI (rel)	Branch if Higher	? C + Z = 0	REL	22	rr	3	—	—	—	—	—	—	—	—
BHS (rel)	Branch if Higher or Same	? C = 0	REL	24	rr	3	—	—	—	—	—	—	—	—
BITA (opr)	Bit(s) Test A with Memory	A • M	A IMM A DIR A EXT A IND,X A IND,Y	85 95 B5 A5 18 A5	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	0	—
BITB (opr)	Bit(s) Test B with Memory	B • M	B IMM B DIR B EXT B IND,X B IND,Y	C5 D5 F5 E5 18 E5	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	0	—
BLE (rel)	Branch if Δ Zero	? Z + (N ⊕ V) = 1	REL	2F	rr	3	—	—	—	—	—	—	—	—
BLO (rel)	Branch if Lower	? C = 1	REL	25	rr	3	—	—	—	—	—	—	—	—
BLS (rel)	Branch if Lower or Same	? C + Z = 1	REL	23	rr	3	—	—	—	—	—	—	—	—
BLT (rel)	Branch if < Zero	? N ⊕ V = 1	REL	2D	rr	3	—	—	—	—	—	—	—	—
BMI (rel)	Branch if Minus	? N = 1	REL	2B	rr	3	—	—	—	—	—	—	—	—
BNE (rel)	Branch if not = Zero	? Z = 0	REL	26	rr	3	—	—	—	—	—	—	—	—
BPL (rel)	Branch if Plus	? N = 0	REL	2A	rr	3	—	—	—	—	—	—	—	—
BRA (rel)	Branch Always	? 1 = 1	REL	20	rr	3	—	—	—	—	—	—	—	—
BRCLR(opr) (msk) (rel)	Branch if Bit(s) Clear	? M • mm = 0	DIR IND,X IND,Y	13 1F 18 1F	dd mm rr ff mm rr ff mm rr	6 7 8	—	—	—	—	—	—	—	—
BRN (rel)	Branch Never	? 1 = 0	REL	21	rr	3	—	—	—	—	—	—	—	—
BRSET(opr) (msk) (rel)	Branch if Bit(s) Set	? (M̄) • mm = 0	DIR IND,X IND,Y	12 1E 18 1E	dd mm rr ff mm rr ff mm rr	6 7 8	—	—	—	—	—	—	—	—
BSET (opr) (msk)	Set Bit(s)	M + mm ⇒ M	DIR IND,X IND,Y	14 1C 18 1C	dd mm ff mm ff mm	6 7 8	—	—	—	—	Δ	Δ	0	—
BSR (rel)	Branch to Subroutine	See Figure 3–2	REL	8D	rr	6	—	—	—	—	—	—	—	—
BVC (rel)	Branch if Overflow Clear	? V = 0	REL	28	rr	3	—	—	—	—	—	—	—	—
BVS (rel)	Branch if Overflow Set	? V = 1	REL	29	rr	3	—	—	—	—	—	—	—	—
CBA	Compare A to B	A – B	INH	11	—	2	—	—	—	—	Δ	Δ	Δ	Δ
CLC	Clear Carry Bit	0 ⇒ C	INH	0C	—	2	—	—	—	—	—	—	—	0
CLI	Clear Interrupt Mask	0 ⇒ I	INH	0E	—	2	—	—	—	0	—	—	—	—
CLR (opr)	Clear Memory Byte	0 ⇒ M	EXT IND,X IND,Y	7F 6F 18 6F	hh ll ff ff	6 6 7	—	—	—	—	0	1	0	0
CLRA	Clear Accumulator A	0 ⇒ A	A INH	4F	—	2	—	—	—	—	0	1	0	0
CLRB	Clear Accumulator B	0 ⇒ B	B INH	5F	—	2	—	—	—	—	0	1	0	0
CLV	Clear Overflow Flag	0 ⇒ V	INH	0A	—	2	—	—	—	—	—	—	0	—
CMPA (opr)	Compare A to Memory	A – M	A IMM A DIR A EXT A IND,X A IND,Y	81 91 B1 A1 18 A1	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	Δ	Δ
CMPB (opr)	Compare B to Memory	B – M	B IMM B DIR B EXT B IND,X B IND,Y	C1 D1 F1 E1 18 E1	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	Δ	Δ

Table 3-2 Instruction Set (Sheet 3 of 6)

Mnemonic	Operation	Description	Addressing Mode	Instruction			Condition Codes							
				Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C
COM (opr)	Ones Complement Memory Byte	$FF – M ⇒ M	EXT IND,X IND,Y	73 63 18 63	hh ll ff ff	6 6 7	—	—	—	—	Δ	Δ	0	1
COMA	Ones Complement A	$FF – A ⇒ A	A INH	43	—	2	—	—	—	—	Δ	Δ	0	1
COMB	Ones Complement B	$FF – B ⇒ B	B INH	53	—	2	—	—	—	—	Δ	Δ	0	1
CPD (opr)	Compare D to Memory 16-Bit	D – M : M + 1	IMM DIR EXT IND,X IND,Y	1A 83 1A 93 1A B3 1A A3 CD A3	jj kk dd hh ll ff ff	5 6 7 7 7	—	—	—	—	Δ	Δ	Δ	Δ
CPX (opr)	Compare X to Memory 16-Bit	IX – M : M + 1	IMM DIR EXT IND,X IND,Y	8C 9C BC AC CD AC	jj kk dd hh ll ff ff	4 5 6 6 7	—	—	—	—	Δ	Δ	Δ	Δ
CPY (opr)	Compare Y to Memory 16-Bit	IY – M : M + 1	IMM DIR EXT IND,X IND,Y	18 8C 18 9C 18 BC 1A AC 18 AC	jj kk dd hh ll ff ff	5 6 7 7 7	—	—	—	—	Δ	Δ	Δ	Δ
DAA	Decimal Adjust A	Adjust Sum to BCD	INH	19	—	2	—	—	—	—	Δ	Δ	Δ	Δ
DEC (opr)	Decrement Memory Byte	M – 1 ⇒ M	EXT IND,X IND,Y	7A 6A 18 6A	hh ll ff ff	6 6 7	—	—	—	—	Δ	Δ	Δ	—
DECA	Decrement Accumulator A	A – 1 ⇒ A	A INH	4A	—	2	—	—	—	—	Δ	Δ	Δ	—
DECB	Decrement Accumulator B	B – 1 ⇒ B	B INH	5A	—	2	—	—	—	—	Δ	Δ	Δ	—
DES	Decrement Stack Pointer	SP – 1 ⇒ SP	INH	34	—	3	—	—	—	—	—	—	—	—
DEX	Decrement Index Register X	IX – 1 ⇒ IX	INH	09	—	3	—	—	—	—	—	Δ	—	—
DEY	Decrement Index Register Y	IY – 1 ⇒ IY	INH	18 09	—	4	—	—	—	—	—	Δ	—	—
EORA (opr)	Exclusive OR A with Memory	A ⊕ M ⇒ A	A IMM A DIR A EXT A IND,X A IND,Y	88 98 B8 A8 18 A8	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	0	—
EORB (opr)	Exclusive OR B with Memory	B ⊕ M ⇒ B	B IMM B DIR B EXT B IND,X B IND,Y	C8 D8 F8 E8 18 E8	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	0	—
FDIV	Fractional Divide 16 by 16	D / IX ⇒ IX; r ⇒ D	INH	03	—	41	—	—	—	—	—	Δ	Δ	Δ
IDIV	Integer Divide 16 by 16	D / IX ⇒ IX; r ⇒ D	INH	02	—	41	—	—	—	—	—	Δ	0	Δ
INC (opr)	Increment Memory Byte	M + 1 ⇒ M	EXT IND,X IND,Y	7C 6C 18 6C	hh ll ff ff	6 6 7	—	—	—	—	Δ	Δ	Δ	—
INCA	Increment Accumulator A	A + 1 ⇒ A	A INH	4C	—	2	—	—	—	—	Δ	Δ	Δ	—
INCB	Increment Accumulator B	B + 1 ⇒ B	B INH	5C	—	2	—	—	—	—	Δ	Δ	Δ	—
INS	Increment Stack Pointer	SP + 1 ⇒ SP	INH	31	—	3	—	—	—	—	—	—	—	—
INX	Increment Index Register X	IX + 1 ⇒ IX	INH	08	—	3	—	—	—	—	—	Δ	—	—

Table 3-2 Instruction Set (Sheet 4 of 6)

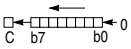
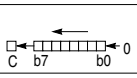
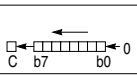
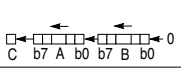
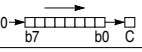
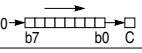
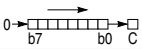
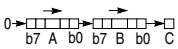
Mnemonic	Operation	Description	Addressing Mode	Instruction			Condition Codes							
				Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C
INY	Increment Index Register Y	IY + 1 ⇒ IY	INH	18 08	—	4	—	—	—	—	—	Δ	—	—
JMP (opr)	Jump	See Figure 3–2	EXT	7E	hh ll	3	—	—	—	—	—	—	—	—
			IND,X	6E	ff	3								
			IND,Y	18 6E	ff	4								
JSR (opr)	Jump to Subroutine	See Figure 3–2	DIR	9D	dd	5	—	—	—	—	—	—	—	—
			EXT	BD	hh ll	6								
			IND,X	AD	ff	6								
			IND,Y	18 AD	ff	7								
LDAA (opr)	Load Accumulator A	M ⇒ A	A IMM	86	ii	2	—	—	—	—	Δ	Δ	0	—
			A DIR	96	dd	3								
			A EXT	B6	hh ll	4								
			A IND,X	A6	ff	4								
			A IND,Y	18 A6	ff	5								
LDAB (opr)	Load Accumulator B	M ⇒ B	B IMM	C6	ii	2	—	—	—	—	Δ	Δ	0	—
			B DIR	D6	dd	3								
			B EXT	F6	hh ll	4								
			B IND,X	E6	ff	4								
			B IND,Y	18 E6	ff	5								
LDD (opr)	Load Double Accumulator D	M ⇒ A,M + 1 ⇒ B	IMM	CC	jj kk	3	—	—	—	—	Δ	Δ	0	—
			DIR	DC	dd	4								
			EXT	FC	hh ll	5								
			IND,X	EC	ff	5								
			IND,Y	18 EC	ff	6								
LDS (opr)	Load Stack Pointer	M : M + 1 ⇒ SP	IMM	8E	jj kk	3	—	—	—	—	Δ	Δ	0	—
			DIR	9E	dd	4								
			EXT	BE	hh ll	5								
			IND,X	AE	ff	5								
			IND,Y	18 AE	ff	6								
LDX (opr)	Load Index Register X	M : M + 1 ⇒ IX	IMM	CE	jj kk	3	—	—	—	—	Δ	Δ	0	—
			DIR	DE	dd	4								
			EXT	FE	hh ll	5								
			IND,X	EE	ff	5								
			IND,Y	CD EE	ff	6								
LDY (opr)	Load Index Register Y	M : M + 1 ⇒ IY	IMM	18 CE	jj kk	4	—	—	—	—	Δ	Δ	0	—
			DIR	18 DE	dd	5								
			EXT	18 FE	hh ll	6								
			IND,X	1A EE	ff	6								
			IND,Y	18 EE	ff	6								
LSL (opr)	Logical Shift Left		EXT	78	hh ll	6	—	—	—	—	Δ	Δ	Δ	Δ
			IND,X	68	ff	6								
			IND,Y	18 68	ff	7								
LSLA	Logical Shift Left A		A INH	48	—	2	—	—	—	—	Δ	Δ	Δ	Δ
LSLB	Logical Shift Left B		B INH	58	—	2	—	—	—	—	Δ	Δ	Δ	Δ
LSLD	Logical Shift Left Double		INH	05	—	3	—	—	—	—	Δ	Δ	Δ	Δ
LSR (opr)	Logical Shift Right		EXT	74	hh ll	6	—	—	—	—	0	Δ	Δ	Δ
			IND,X	64	ff	6								
			IND,Y	18 64	ff	7								
LSRA	Logical Shift Right A		A INH	44	—	2	—	—	—	—	0	Δ	Δ	Δ
LSRB	Logical Shift Right B		B INH	54	—	2	—	—	—	—	0	Δ	Δ	Δ
LSRD	Logical Shift Right Double		INH	04	—	3	—	—	—	—	0	Δ	Δ	Δ
MUL	Multiply 8 by 8	A * B ⇒ D	INH	3D	—	10	—	—	—	—	—	—	—	Δ
NEG (opr)	Two's Complement Memory Byte	0 – M ⇒ M	EXT	70	hh ll	6	—	—	—	—	Δ	Δ	Δ	Δ
			IND,X	60	ff	6								
			IND,Y	18 60	ff	7								
NEGA	Two's Complement A	0 – A ⇒ A	A INH	40	—	2	—	—	—	—	Δ	Δ	Δ	Δ
NEGB	Two's Complement B	0 – B ⇒ B	B INH	50	—	2	—	—	—	—	Δ	Δ	Δ	Δ

Table 3-2 Instruction Set (Sheet 5 of 6)

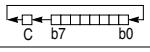
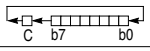
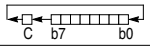
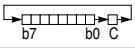
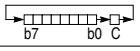
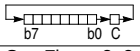
Mnemonic	Operation	Description	Addressing Mode	Instruction			Condition Codes							
				Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C
NOP	No operation	No Operation	INH	01	—	2	—	—	—	—	—	—	—	—
ORAA (opr)	OR Accumulator A (Inclusive)	A + M ⇒ A	A IMM	8A	ii	2	—	—	—	—	Δ	Δ	0	—
			A DIR	9A	dd	3								
			A EXT	BA	hh ll	4								
			A IND,X	AA	ff	4								
			A IND,Y	18 AA	ff	5								
ORAB (opr)	OR Accumulator B (Inclusive)	B + M ⇒ B	B IMM	CA	ii	2	—	—	—	—	Δ	Δ	0	—
			B DIR	DA	dd	3								
			B EXT	FA	hh ll	4								
			B IND,X	EA	ff	4								
			B IND,Y	18 EA	ff	5								
PSHA	Push A onto Stack	A ⇒ Stk,SP = SP – 1	A INH	36	—	3	—	—	—	—	—	—	—	—
PSHB	Push B onto Stack	B ⇒ Stk,SP = SP – 1	B INH	37	—	3	—	—	—	—	—	—	—	—
PSHX	Push X onto Stack (Lo First)	IX ⇒ Stk,SP = SP – 2	INH	3C	—	4	—	—	—	—	—	—	—	—
PSHY	Push Y onto Stack (Lo First)	IY ⇒ Stk,SP = SP – 2	INH	18 3C	—	5	—	—	—	—	—	—	—	—
PULA	Pull A from Stack	SP = SP + 1, A ⇐ Stk	A INH	32	—	4	—	—	—	—	—	—	—	—
PULB	Pull B from Stack	SP = SP + 1, B ⇐ Stk	B INH	33	—	4	—	—	—	—	—	—	—	—
PULX	Pull X From Stack (Hi First)	SP = SP + 2, IX ⇐ Stk	INH	38	—	5	—	—	—	—	—	—	—	—
PULY	Pull Y from Stack (Hi First)	SP = SP + 2, IY ⇐ Stk	INH	18 38	—	6	—	—	—	—	—	—	—	—
ROL (opr)	Rotate Left		EXT	79	hh ll	6	—	—	—	—	Δ	Δ	Δ	Δ
			IND,X	69	ff	6								
			IND,Y	18 69	ff	7								
ROLA	Rotate Left A		A INH	49	—	2	—	—	—	—	Δ	Δ	Δ	Δ
ROLB	Rotate Left B		B INH	59	—	2	—	—	—	—	Δ	Δ	Δ	Δ
ROR (opr)	Rotate Right		EXT	76	hh ll	6	—	—	—	—	Δ	Δ	Δ	Δ
			IND,X	66	ff	6								
			IND,Y	18 66	ff	7								
RORA	Rotate Right A		A INH	46	—	2	—	—	—	—	Δ	Δ	Δ	Δ
RORB	Rotate Right B		B INH	56	—	2	—	—	—	—	Δ	Δ	Δ	Δ
RTI	Return from Interrupt	See Figure 3–2	INH	3B	—	12	Δ	↓	Δ	Δ	Δ	Δ	Δ	Δ
RTS	Return from Subroutine	See Figure 3–2	INH	39	—	5	—	—	—	—	—	—	—	—
SBA	Subtract B from A	A – B ⇒ A	INH	10	—	2	—	—	—	—	Δ	Δ	Δ	Δ
SBCA (opr)	Subtract with Carry from A	A – M – C ⇒ A	A IMM	82	ii	2	—	—	—	—	Δ	Δ	Δ	Δ
			A DIR	92	dd	3								
			A EXT	B2	hh ll	4								
			A IND,X	A2	ff	4								
			A IND,Y	18 A2	ff	5								
SBCB (opr)	Subtract with Carry from B	B – M – C ⇒ B	B IMM	C2	ii	2	—	—	—	—	Δ	Δ	Δ	Δ
			B DIR	D2	dd	3								
			B EXT	F2	hh ll	4								
			B IND,X	E2	ff	4								
			B IND,Y	18 E2	ff	5								
SEC	Set Carry	1 ⇒ C	INH	0D	—	2	—	—	—	—	—	—	—	1
SEI	Set Interrupt Mask	1 ⇒ I	INH	0F	—	2	—	—	—	1	—	—	—	—
SEV	Set Overflow Flag	1 ⇒ V	INH	0B	—	2	—	—	—	—	—	—	1	—
STAA (opr)	Store Accumulator A	A ⇒ M	A DIR	97	dd	3	—	—	—	—	Δ	Δ	0	—
			A EXT	B7	hh ll	4								
			A IND,X	A7	ff	4								
			A IND,Y	18 A7	ff	5								

Table 3-2 Instruction Set (Sheet 6 of 6)

Mnemonic	Operation	Description	Addressing Mode	Instruction			Condition Codes							
				Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C
STAB (opr)	Store Accumulator B	B ⇒ M	B DIR	D7	dd	3	—	—	—	—	Δ	Δ	0	—
			B EXT	F7	hh ll	4								
			B IND,X	E7	ff	4								
			B IND,Y	18 E7	ff	5								
STD (opr)	Store Accumulator D	A ⇒ M, B ⇒ M + 1	DIR	DD	dd	4	—	—	—	—	Δ	Δ	0	—
			EXT	FD	hh ll	5								
			IND,X	ED	ff	5								
			IND,Y	18 ED	ff	6								
STOP	Stop Internal Clocks	—	INH	CF	—	2	—	—	—	—	—	—	—	—
STS (opr)	Store Stack Pointer	SP ⇒ M : M + 1	DIR	9F	dd	4	—	—	—	—	Δ	Δ	0	—
			EXT	BF	hh ll	5								
			IND,X	AF	ff	5								
			IND,Y	18 AF	ff	6								
STX (opr)	Store Index Register X	IX ⇒ M : M + 1	DIR	DF	dd	4	—	—	—	—	Δ	Δ	0	—
			EXT	FF	hh ll	5								
			IND,X	EF	ff	5								
			IND,Y	CD EF	ff	6								
STY (opr)	Store Index Register Y	IY ⇒ M : M + 1	DIR	18 DF	dd	5	—	—	—	—	Δ	Δ	0	—
			EXT	18 FF	hh ll	6								
			IND,X	1A EF	ff	6								
			IND,Y	18 EF	ff	6								
SUBA (opr)	Subtract Memory from A	A – M ⇒ A	A IMM	80	ii	2	—	—	—	—	Δ	Δ	Δ	Δ
			A DIR	90	dd	3								
			A EXT	B0	hh ll	4								
			A IND,X	A0	ff	4								
			A IND,Y	18 A0	ff	5								
SUBB (opr)	Subtract Memory from B	B – M ⇒ B	A IMM	C0	ii	2	—	—	—	—	Δ	Δ	Δ	Δ
			A DIR	D0	dd	3								
			A EXT	F0	hh ll	4								
			A IND,X	E0	ff	4								
			A IND,Y	18 E0	ff	5								
SUBD (opr)	Subtract Memory from D	D – M : M + 1 ⇒ D	IMM	83	jj kk	4	—	—	—	—	Δ	Δ	Δ	Δ
			DIR	93	dd	5								
			EXT	B3	hh ll	6								
			IND,X	A3	ff	6								
			IND,Y	18 A3	ff	7								
SWI	Software Interrupt	See Figure 3–2	INH	3F	—	14	—	—	—	1	—	—	—	—
TAB	Transfer A to B	A ⇒ B	INH	16	—	2	—	—	—	—	Δ	Δ	0	—
TAP	Transfer A to CC Register	A ⇒ CCR	INH	06	—	2	Δ	↓	Δ	Δ	Δ	Δ	Δ	Δ
TBA	Transfer B to A	B ⇒ A	INH	17	—	2	—	—	—	—	Δ	Δ	0	—
TEST	TEST (Only in Test Modes)	Address Bus Counts	INH	00	—	*	—	—	—	—	—	—	—	—
TPA	Transfer CC Register to A	CCR ⇒ A	INH	07	—	2	—	—	—	—	—	—	—	—
TST (opr)	Test for Zero or Minus	M – 0	EXT	7D	hh ll	6	—	—	—	—	Δ	Δ	0	0
			IND,X	6D	ff	6								
			IND,Y	18 6D	ff	7								
TSTA	Test A for Zero or Minus	A – 0	A INH	4D	—	2	—	—	—	—	Δ	Δ	0	0
TSTB	Test B for Zero or Minus	B – 0	B INH	5D	—	2	—	—	—	—	Δ	Δ	0	0
TSX	Transfer Stack Pointer to X	SP + 1 ⇒ IX	INH	30	—	3	—	—	—	—	—	—	—	—
TSY	Transfer Stack Pointer to Y	SP + 1 ⇒ IY	INH	18 30	—	4	—	—	—	—	—	—	—	—
TXS	Transfer X to Stack Pointer	IX – 1 ⇒ SP	INH	35	—	3	—	—	—	—	—	—	—	—
TYS	Transfer Y to Stack Pointer	IY – 1 ⇒ SP	INH	18 35	—	4	—	—	—	—	—	—	—	—
WAI	Wait for Interrupt	Stack Regs & WAIT	INH	3E	—	**	—	—	—	—	—	—	—	—
XGDX	Exchange D with X	IX ⇒ D, D ⇒ IX	INH	8F	—	3	—	—	—	—	—	—	—	—
XGDY	Exchange D with Y	IY ⇒ D, D ⇒ IY	INH	18 8F	—	4	—	—	—	—	—	—	—	—

Cycle

*	Infinity or until reset occurs
**	12 Cycles are used beginning with the opcode fetch. A wait state is entered which remains in effect for an integer number of MPU E-Clock cycles (n) until an interrupt is recognized. Finally, two additional cycles are used to fetch the appropriate interrupt vector (14 + n total).

Operands

dd	= 8-Bit Direct Address ($0000 –$00FF) (High Byte Assumed to be $00)
ff	= 8-Bit Positive Offset $00 (0) to $FF (255) (Is Added to Index)
hh	= High-Order Byte of 16-Bit Extended Address
ii	= One Byte of Immediate Data
jj	= High-Order Byte of 16-Bit Immediate Data
kk	= Low-Order Byte of 16-Bit Immediate Data
ll	= Low-Order Byte of 16-Bit Extended Address
mm	= 8-Bit Mask (Set Bits to be Affected)
rr	= Signed Relative Offset $80 (–128) to $7F (+127) (Offset Relative to Address Following Machine Code Offset Byte))

Operators

( )	Contents of register shown inside parentheses
⇐	Is transferred to
⇑	Is pulled from stack
⇓	Is pushed onto stack
•	Boolean AND
+	Arithmetic Addition Symbol except where used as Inclusive-OR symbol in Boolean Formula
⊕	Exclusive-OR
*	Multiply
:	Concatenation
–	Arithmetic subtraction symbol or Negation symbol (Two's Complement)

Condition Codes

—	Bit not changed
0	Bit always cleared
1	Bit always set
Δ	Bit cleared or set, depending on operation
↓	Bit can be cleared, cannot become set

APPENDIX A ELECTRICAL CHARACTERISTICS

Table A-1 Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.3 to + 7.0	V
Input Voltage	V_{in}	–0.3 to + 7.0	V
Operating Temperature Range MC68HC(7)11Ex MC68HC(7)11ExC MC68HC(7)11ExV MC68HC(7)11ExM MC68HC811E2 MC68HC811E2C MC68HC811E2V MC68HC811E2M MC68L11Ex	T_A	T_L to T_H 0 to + 70 –40 to + 85 –40 to + 105 –40 to + 125 0 to + 70 –40 to + 85 –40 to + 105 –40 to + 125 –20 to + 70	°C
Storage Temperature Range	T_{stg}	–55 to + 150	°C
Current Drain per Pin[1] Excluding V_{DD}, V_{SS}, AV_{DD}, V_{RH}, and V_{RL}	I_D	25	mA

NOTES:
1. One pin at a time, observing maximum power dissipation limits

Internal circuitry protects the inputs against damage caused by high static voltages or electric fields; however, normal precautions are necessary to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Extended operation at the maximum ratings can adversely affect device reliability. Tying unused inputs to an appropriate logic voltage level (either GND or V_{DD}) enhances reliability of operation.

Table A-2 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Average Junction Temperature	T_J	$T_A + (P_D \times \Theta_{JA})$	°C
Ambient Temperature	T_A	User-determined	°C
Package Thermal Resistance (Junction-to-Ambient) 48-Pin Plastic DIP (MC68HC811E2 only) 56-Pin Plastic SDIP 52-Pin Plastic Leaded Chip Carrier 52-Pin Plastic Thin Quad Flat Pack (TQFP) 64-Pin Quad Flat Pack	Θ_{JA}	 50 50 50 85 85	°C/W
Total Power Dissipation (Note 1)	P_D	$P_{INT} + P_{I/O}$ $K / (T_J + 273°C)$ (Note 1)	W
Device Internal Power Dissipation	P_{INT}	$I_{DD} \times V_{DD}$	W
I/O Pin Power Dissipation (Note 2)	$P_{I/O}$	User-determined	W
A Constant (Note 3)	K	$P_D \times (T_A + 273°C) + \Theta_{JA} \times P_D^2$	W·°C

NOTES:
1. This is an approximate value, neglecting $P_{I/O.}$
2. For most applications neglected.
3. K is a constant pertaining to the device. Solve for K with a known T_A and a measured P_D (at equilibrium). Use this value of K to solve for P_D and T_J iteratively for any value of T_A.

Table A-3 DC Electrical Characteristics

V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted

Characteristics		Symbol	Min	Max	Unit
Output Voltage (Note 1) All Outputs except XTAL All Outputs Except XTAL, $\overline{\text{RESET}}$, and MODA I_{Load} = ±10.0 µA		V_{OL} V_{OH}	— V_{DD} –0.1	0.1 —	V
Output High Voltage (Note 1) All Outputs Except XTAL, $\overline{\text{RESET}}$, and MODA I_{Load} = –0.8 mA, V_{DD} = 4.5 V		V_{OH}	V_{DD} –0.8	—	V
Output Low Voltage All Outputs Except XTAL I_{Load} = 1.6 mA		V_{OL}	—	0.4	V
Input High Voltage	All Inputs Except $\overline{\text{RESET}}$ $\overline{\text{RESET}}$	V_{IH}	$0.7 \times V_{DD}$ $0.8 \times VDD$	V_{DD} + 0.3 V_{DD} + 0.3	V
Input Low Voltage	All Inputs	V_{IL}	V_{SS} –0.3	$0.2 \times V_{DD}$	V
I/O Ports, Three-State Leakage $V_{in} = V_{IH}$ or V_{IL}	PA7, PA3, PC[7:0], PD[5:0], AS/STRA, MODA/$\overline{\text{LIR}}$, $\overline{\text{RESET}}$	I_{OZ}	—	±10	µA
Input Leakage Current (Note 2) $V_{in} = V_{DD}$ or V_{SS} $V_{in} = V_{DD}$ or V_{SS}	 PA[2:0], $\overline{\text{IRQ}}$, $\overline{\text{XIRQ}}$ MODB/V_{STBY} ($\overline{\text{XIRQ}}$ on EPROM-based devices)	I_{in}	 — —	 ±1 ±10	 µA µA
RAM Standby Voltagee	Power down	V_{SB}	4.0	V_{DD}	V
RAM Standby Current	Power down	I_{SB}	—	10	µA
Input Capacitance	PA[2:0], PE[7:0], $\overline{\text{IRQ}}$, $\overline{\text{XIRQ}}$, EXTAL PA7, PA3, PC[7:0], PD[5:0], AS/STRA, MODA/$\overline{\text{LIR}}$, $\overline{\text{RESET}}$	C_{in}	— —	8 12	pF pF
Output Load Capacitance	All Outputs Except PD[4:1] PD[4:1]	C_L	— —	90 100	pF pF
Maximum Total Supply Current (Note 3) **RUN:**		I_{DD}			
Single-Chip Mode	2 MHz		—	15	mA
	3 MHz		—	27	mA
Expanded Multiplexed Mode	2 MHz		—	27	mA
	3 MHz		—	35	mA
WAIT: (All Peripheral Functions Shut Down)		W_{IDD}			
Single-Chip Mode	2 MHz		—	6	mA
	3 MHz		—	15	mA
Expanded Multiplexed Mode	2 MHz		—	10	mA
	3 MHz		—	20	mA
STOP:		S_{IDD}			
Single-Chip Mode, No Clocks	–40 to + 85		—	25	µA
	> + 85 to + 105		—	50	
	> +105 to + 125		—	100	
Maximum Power Dissipation		P_D			
Single-Chip Mode	2 MHz		—	85	mW
	3 MHz		—	150	mW
Expanded Multiplexed Mode	2 MHz		—	150	mW
	3 MHz		—	195	mW

NOTES:

1. V_{OH} specification for $\overline{\text{RESET}}$ and MODA is not applicable because they are open-drain pins. V_{OH} specification not applicable to ports C and D in wired-OR mode.
2. Refer to A/D specification for leakage current for port E.
3. EXTAL is driven with a square wave, and
   t_{cyc} = 500 ns for 2 MHz rating;
   t_{cyc} = 333 ns for 3 MHz rating; $V_{IL} \leq 0.2$ V;
   $V_{IH} \geq V_{DD} – 0.2$ V; No dc loads

Table A-3a DC Electrical Characteristics (MC68L11E9)

V_{DD} = 3.0 Vdc to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted

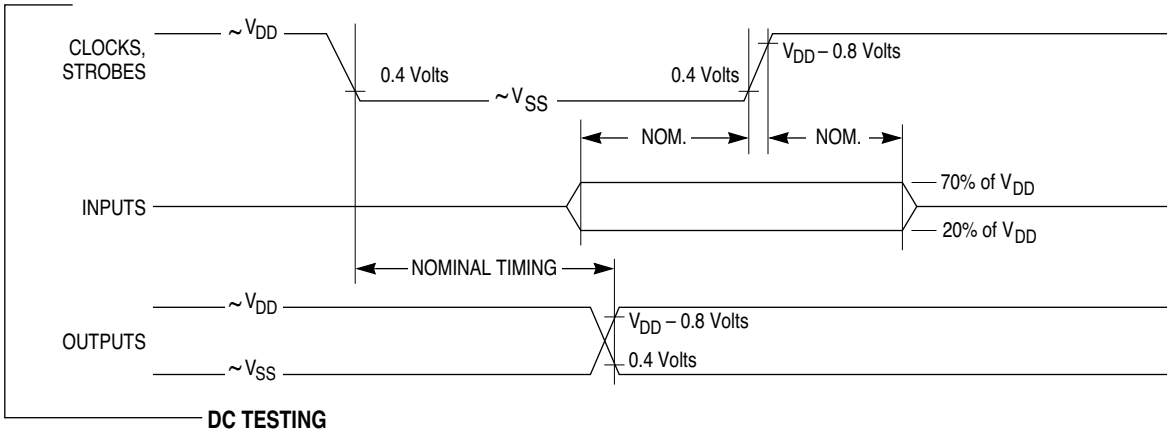
Characteristic	Symbol	Min	Max	Unit
Output Voltage (Note 1) All Outputs except XTAL	V_{OL}	—	0.1	V
All Outputs Except XTAL, $\overline{\text{RESET}}$, and MODA	V_{OH}	V_{DD} –0.1	—	V
I_{Load} = ±10.0 µA				
Output High Voltage (Note 1) All Outputs Except XTAL, $\overline{\text{RESET}}$, and MODA	V_{OH}	V_{DD} –0.8	—	V
I_{Load} = –0.5 mA, V_{DD} = 3.0 V				
I_{Load} = –0.8 mA, V_{DD} = 4.5 V				
Output Low Voltage All Outputs Except XTAL	V_{OL}	—	0.4	V
I_{Load} = 1.6 mA, V_{DD} = 5.0 V				
I_{Load} = 1.0 mA, V_{DD} = 3.0 V				
Input High Voltage All Inputs Except $\overline{\text{RESET}}$	V_{IH}	$0.7 \times V_{DD}$	V_{DD} + 0.3	V
$\overline{\text{RESET}}$		$0.8 \times V_{DD}$	V_{DD} + 0.3	V
Input Low Voltage All Inputs	V_{IL}	V_{SS} –0.3	$0.2 \times V_{DD}$	V
I/O Ports, Three-State Leakage PA7, PA3, PC[7:0], PD[5:0], AS/STRA,	I_{OZ}	—	±10	µA
$V_{in} = V_{IH}$ or V_{IL} MODA/$\overline{\text{LIR}}$, $\overline{\text{RESET}}$				
Input Leakage Current (Note 2)	I_{in}			
$V_{in} = V_{DD}$ or V_{SS} PA[2:0], $\overline{\text{IRQ}}$, $\overline{\text{XIRQ}}$		—	±1	µA
$V_{in} = V_{DD}$ or V_{SS} MODB/V_{STBY} ($\overline{\text{XIRQ}}$ on EPROM-based devices)		—	±10	µA
RAM Standby Voltage Power down	V_{SB}	2.0	V_{DD}	V
RAM Standby Current Power down	I_{SB}	—	10	µA
Input Capacitance PA[2:0], PE[7:0], $\overline{\text{IRQ}}$, $\overline{\text{XIRQ}}$, EXTAL	C_{in}	—	8	pF
PA7, PA3, PC[7:0], PD[5:0], AS/STRA, MODA/$\overline{\text{LIR}}$, $\overline{\text{RESET}}$		—	12	pF
Output Load Capacitance All Outputs Except PD[4:1]	C_L	—	90	pF
PD[4:1]		—	100	pF

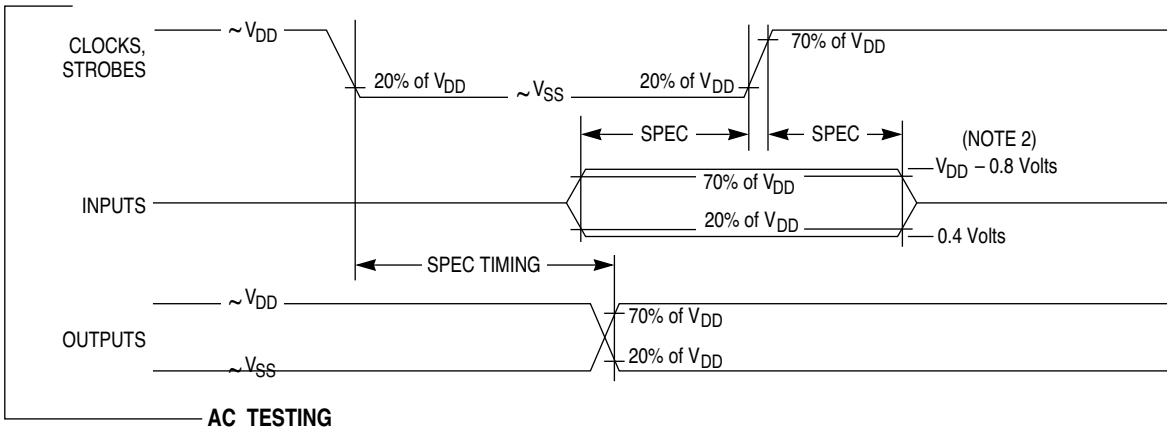
Characteristic		Symbol	1 MHz	2 MHz	Unit
Maximum Total Supply Current (Note 3)					
RUN:		I_{DD}			
Single-Chip Mode	V_{DD} = 5.5 V		8	15	mA
	V_{DD} = 3.0 V		4	8	mA
Expanded Multiplexed Mode	V_{DD} = 5.5 V		14	27	mA
	V_{DD} = 3.0 V		7	14	mA
WAIT:(All Peripheral Functions Shut Down)		W_{IDD}			
Single-Chip Mode	V_{DD} = 5.5 V		3	6	mA
	V_{DD} = 3.0 V		1.5	3	mA
Expanded Multiplexed Mode	V_{DD} = 5.5 V		5	10	mA
	V_{DD} = 3.0 V		2.5	5	mA
STOP:		S_{IDD}			
Single-Chip Mode, No Clocks	V_{DD} = 5.5 V		50	50	µA
	V_{DD} = 3.0 V		25	25	µA
Maximum Power Dissipation		P_D			
Single-Chip Mode	V_{DD} = 5.5 V		44	85	mW
	V_{DD} = 3.0 V		12	24	mW
Expanded Multiplexed Mode	V_{DD} = 5.5 V		77	150	mW
	V_{DD} = 3.0 V		21	42	mW

NOTES:

1. V_{OH} specification for $\overline{\text{RESET}}$ and MODA is not applicable because they are open-drain pins. V_{OH} specification not applicable to ports C and D in wired-OR mode.
2. Refer to A/D specification for leakage current for port E.
3. EXTAL is driven with a square wave, and
   t_{cyc} = 1000 ns for 1 MHz rating;
   t_{cyc} = 500 ns for 2 MHz rating; $V_{IL} \leq 0.2$ V;
   $V_{IH} \geq V_{DD}$ - 0.2 V; No dc loads.

A





NOTES:

1. Full test loads are applied during all DC electrical tests and AC timing measurements.
2. During AC timing measurements, inputs are driven to 0.4 volts and VDD – 0.8 volts while timing measurements are taken at the 20% and 70% of V_{DD} points.

TEST METHODS

Figure A-1 Test Methods

Table A-4 Control Timing

V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H

Characteristic	Symbol	1.0 MHz		2.0 MHz		3.0 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Frequency of Operation	f_o	dc	1.0	dc	2.0	dc	3.0	MHz
E-Clock Period	t_{cyc}	1000	—	500	—	333	—	ns
Crystal Frequency	f_{XTAL}	—	4.0	—	8.0	—	12.0	MHz
External Oscillator Frequency	4 f_o	dc	4.0	dc	8.0	dc	12.0	MHz
Processor Control Setup Time t_{PCSU} = 1/4 t_{cyc} + 50 ns	t_{PCSU}	300	—	175	—	133	—	ns
Reset Input Pulse Width To Guarantee External Reset Vector Minimum Input Time (Can Be Preempted by Internal Reset)	PW_{RSTL}	 8 1	 — —	 8 1	 — —	 8 1	 — —	t_{cyc}
Mode Programming Setup Time	t_{MPS}	2	—	2	—	2	—	t_{cyc}
Mode Programming Hold Time	t_{MPH}	10	—	10	—	10	—	ns
Interrupt Pulse Width, $\overline{IRQ}$ Edge-Sensitive Mode $PW_{IRQ} = t_{cyc} + 20$ ns	PW_{IRQ}	1020	—	520	—	353	—	ns
Wait Recovery Start-up Time	t_{WRS}	—	4	—	4	—	4	t_{cyc}
Timer Pulse Width Input Capture Pulse Accumulator Input $PW_{TIM} = t_{cyc} + 20$ ns	PW_{TIM}	1020	—	520	—	353	—	ns

NOTES:

1. $\overline{RESET}$ is recognized during the first clock cycle it is held low. Internal circuitry then drives the pin low for four clock cycles, releases the pin, and samples the pin level two cycles later to determine the source of the interrupt. Refer to **SECTION 5 RESETS AND INTERRUPTS** for further detail.
2. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.

A

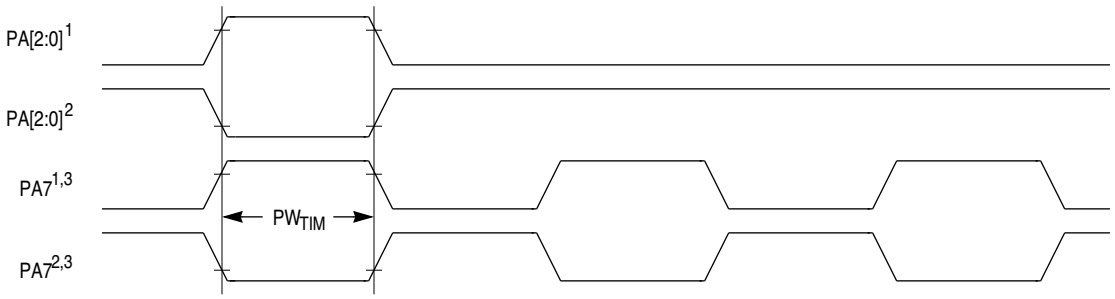
Table A-4a Control Timing (MC68L11E9)

V_{DD} = 3.0 Vdc to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H

Characteristic	Symbol	1.0 MHz		2.0 MHz		Unit
		Min	Max	Min	Max	
Frequency of Operation	f_o	dc	1.0	dc	2.0	MHz
E-Clock Period	t_{cyc}	1000	—	500	—	ns
Crystal Frequency	f_{XTAL}	—	4.0	—	8.0	MHz
External Oscillator Frequency	4 f_o	dc	4.0	dc	8.0	MHz
Processor Control Setup Time t_{PCSU} = 1/4 t_{cyc} + 75 ns	t_{PCSU}	325	—	200	—	ns
Reset Input Pulse Width To Guarantee External Reset Vector Minimum Input Time (Can Be Preempted by Internal Reset)	PW_{RSTL}	 8 1	 — —	 8 1	 — —	 t_{cyc} t_{cyc}
Mode Programming Setup Time	t_{MPS}	2	—	2	—	t_{cyc}
Mode Programming Hold Time	t_{MPH}	10	—	10	—	ns
Interrupt Pulse Width, $\overline{IRQ}$ Edge-Sensitive Mode $PW_{IRQ} = t_{cyc} + 20$ ns	PW_{IRQ}	1020	—	520	—	ns
Wait Recovery Start-up Time	t_{WRS}	—	4	—	4	t_{cyc}
Timer Pulse Width, Input Capture Pulse Accumulator Input $PW_{TIM} = t_{cyc} + 20$ ns	PW_{TIM}	1020	—	520	—	ns

NOTES:

1. $\overline{RESET}$ is recognized during the first clock cycle it is held low. Internal circuitry then drives the pin low for four clock cycles, releases the pin, and samples the pin level two cycles later to determine the source of the interrupt. Refer to **SECTION 5 RESETS AND INTERRUPTS** for further detail.
2. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.



NOTES:
1. Rising edge sensitive input
2. Falling edge sensitive input
3. Maximum pulse accumulator clocking rate is E-clock frequency divided by 2.

TIMER INPUTS TIM

Figure A-2 Timer Inputs

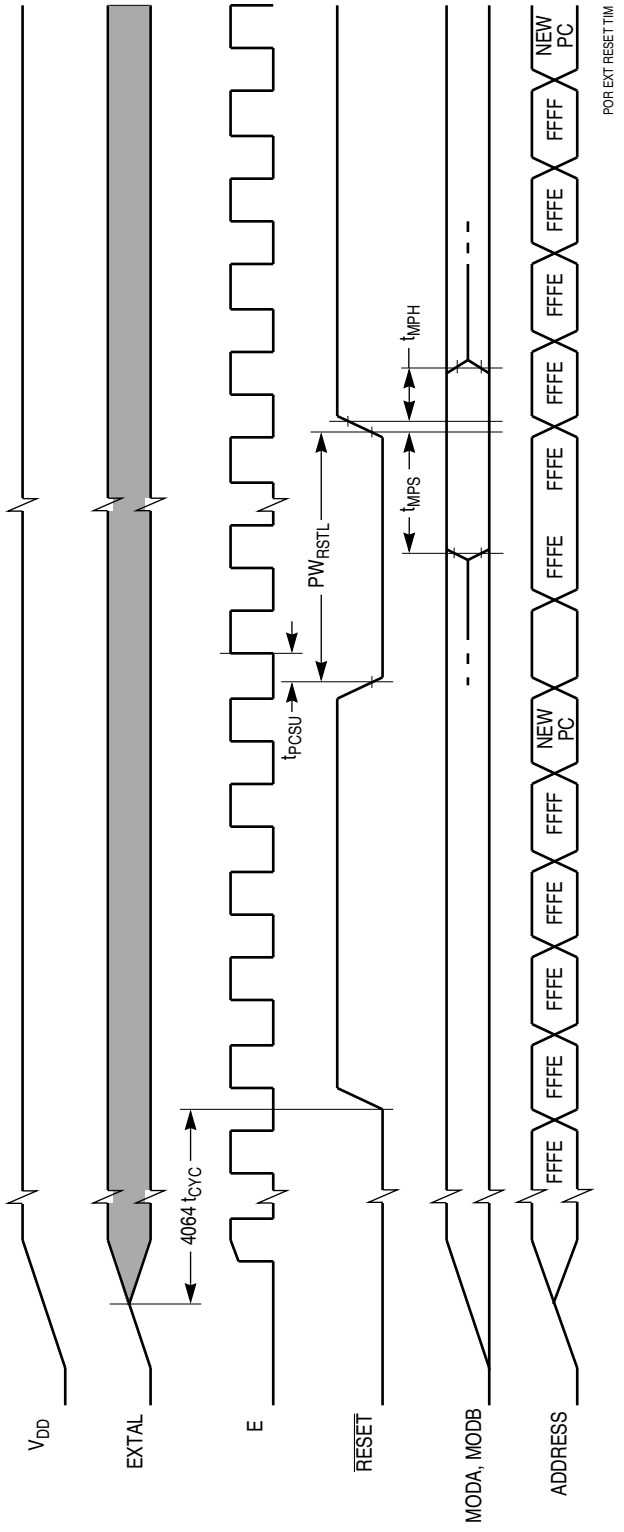


Figure A-3 POR External Reset Timing Diagram

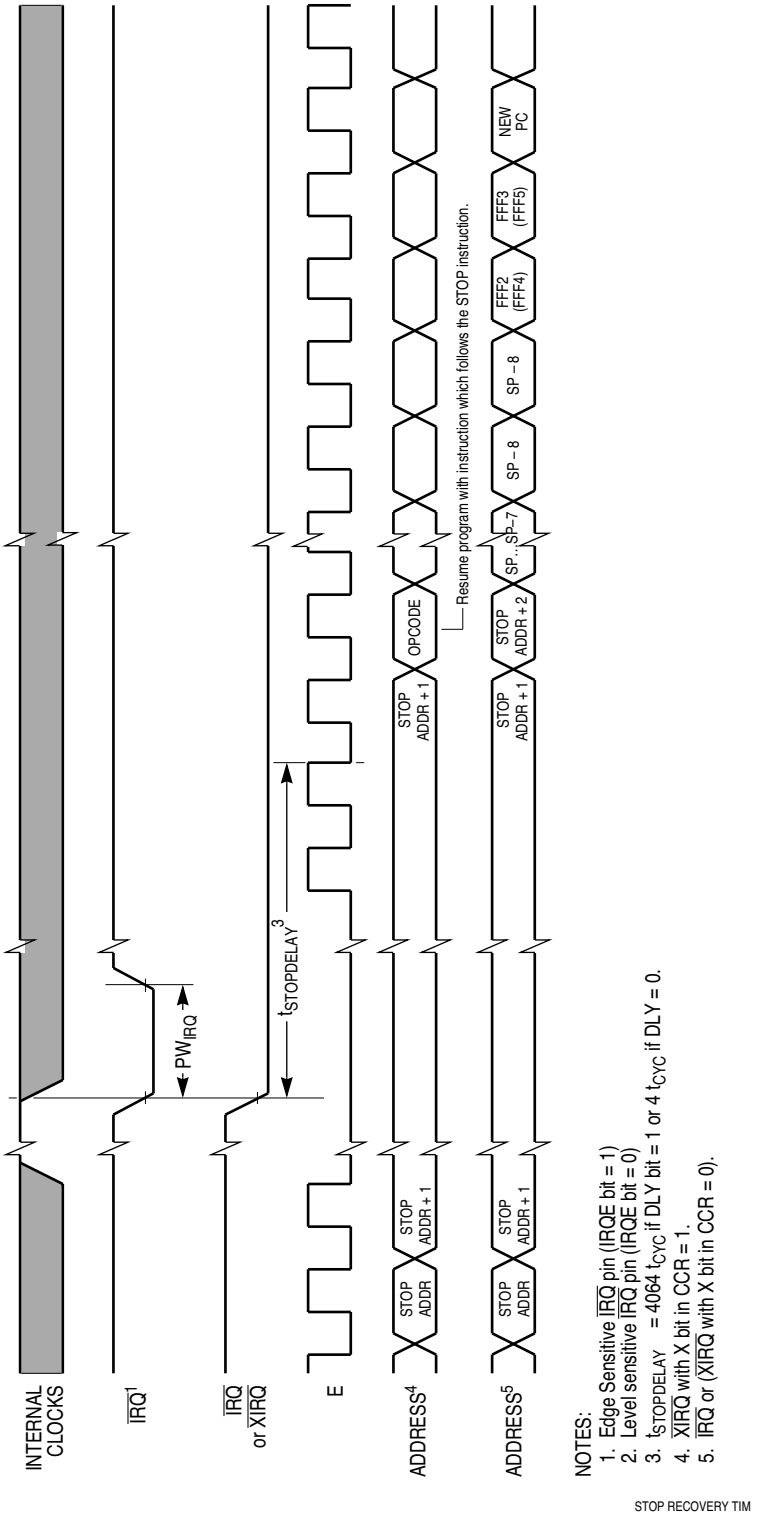


Figure A-4 STOP Recovery Timing Diagram

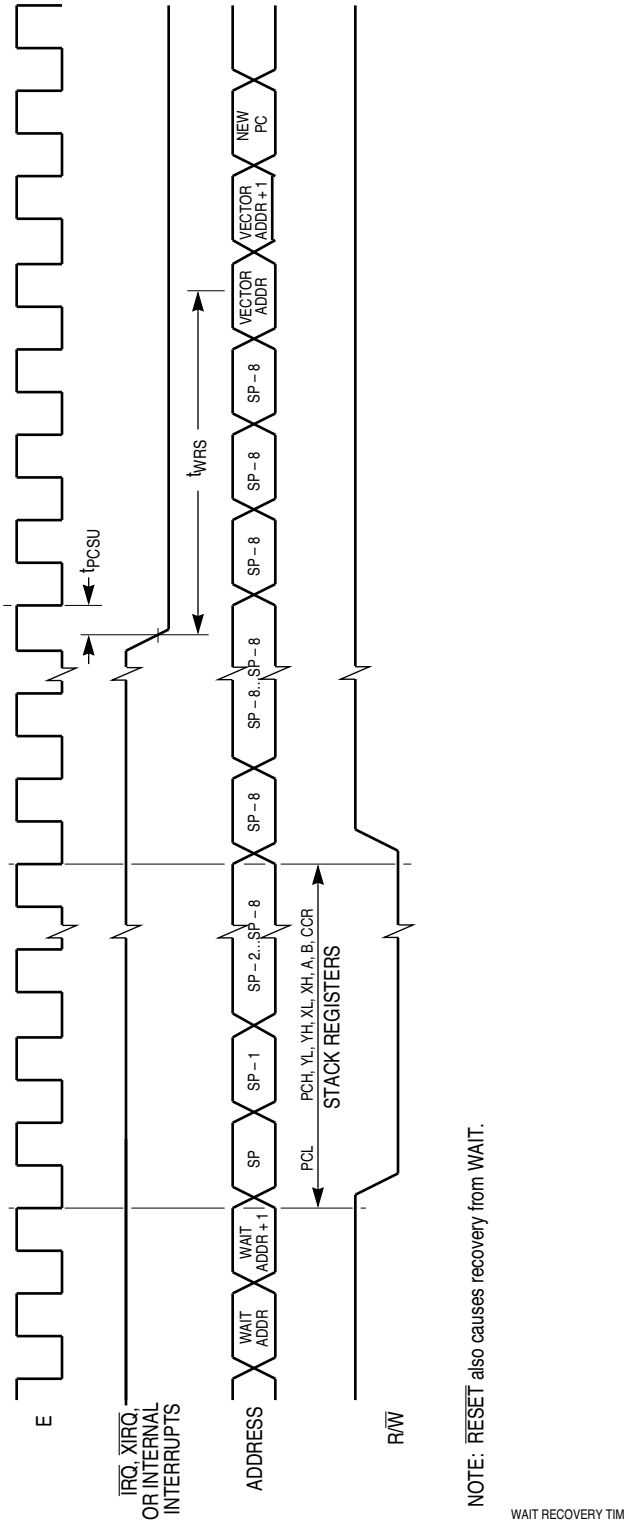


Figure A-5 WAIT Recovery from Interrupt Timing Diagram

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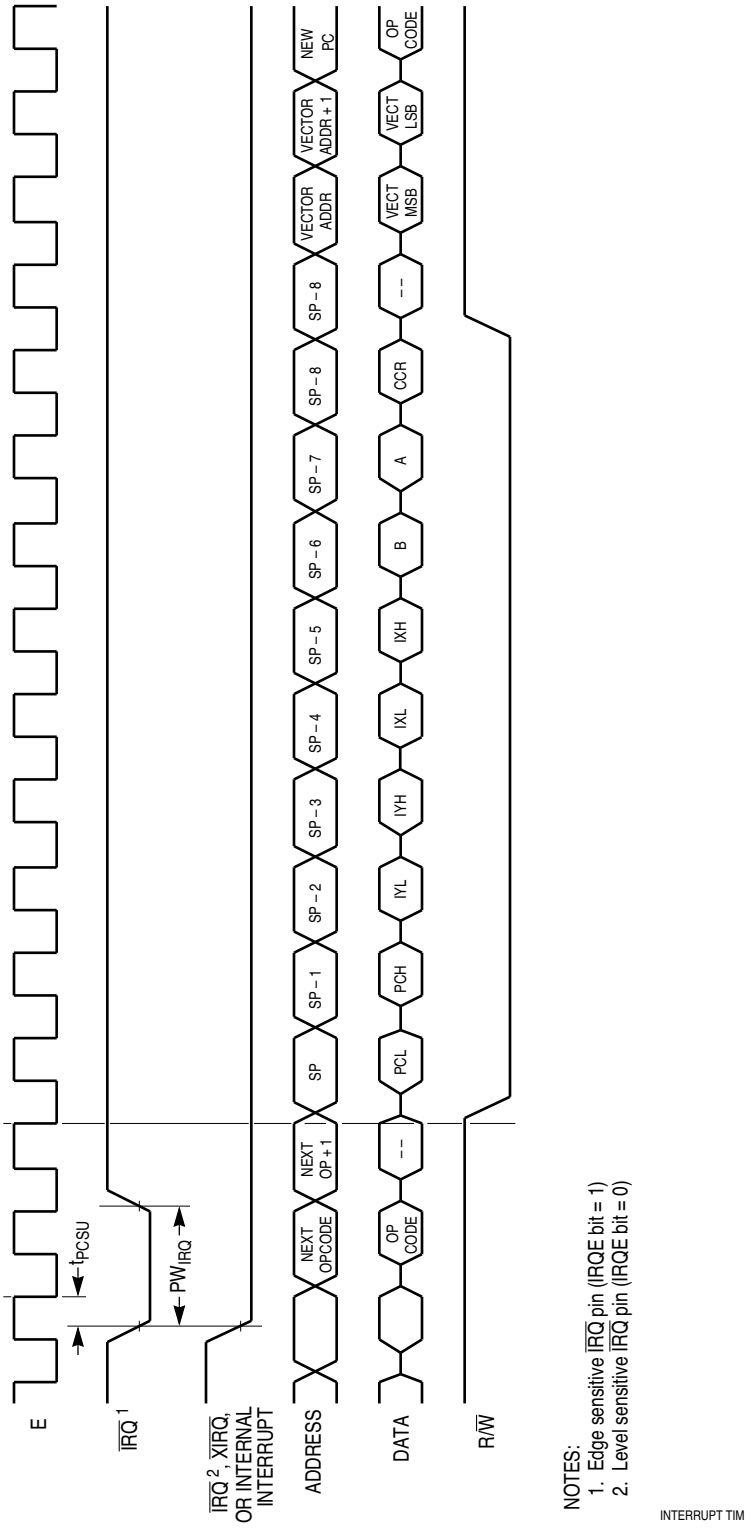

Figure A-6 Interrupt Timing Diagram

Table A-5 Peripheral Port Timing

V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H

Characteristic	Symbol	1.0 MHz		2.0 MHz		3.0 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Frequency of Operation (E-Clock Frequency)	f_o	dc	1.0	dc	2.0	dc	3.0	MHz
E-Clock Period	t_{cyc}	1000	—	500	—	333	—	ns
Peripheral Data Setup Time MCU Read of Ports A, C, D, and E	t_{PDSU}	100	—	100	—	100	—	ns
Peripheral Data Hold Time MCU Read of Ports A, C, D, and E	t_{PDH}	50	—	50	—	50	—	ns
Delay Time, Peripheral Data Write MCU Write to Port A MCU Writes to Ports B, C, and D t_{PWD} = 1/4 t_{cyc} + 100 ns	t_{PWD}	 — —	 200 350	 — —	 200 225	 — —	 200 183	 ns ns
Input Data Setup Time (Port C)	t_{IS}	60	—	60	—	60	—	ns
Input Data Hold Time (Port C)	t_{IH}	100	—	100	—	100	—	ns
Delay Time, E Fall to STRB t_{DEB} = 1/4 t_{cyc} + 100 ns	t_{DEB}	—	350	—	225	—	183	ns
Setup Time, STRA Asserted to E Fall (Note 1)	t_{AES}	0	—	0	—	0	—	ns
Delay Time, STRA Asserted to Port C Data Output Valid	t_{PCD}	—	100	—	100	—	100	ns
Hold Time, STRA Negated to Port C Data	t_{PCH}	10	—	10	—	10	—	ns
Three-State Hold Time	t_{PCZ}	—	150	—	150	—	150	ns

NOTES:

1. If this setup time is met, STRB acknowledges in the next cycle. If it is not met, the response may be delayed one more cycle.
2. Port C and D timing is valid for active drive (CWOM and DWOM bits not set in PIOC and SPCR registers respectively).
3. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.

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Table A-5a Peripheral Port Timing (MC68L11E9)

V_{DD} = 3.0 Vdc to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H

Characteristic	Symbol	1.0 MHz		2.0 MHz		Unit
		Min	Max	Min	Max	
Frequency of Operation (E-Clock Frequency)	f_o	dc	1.0	dc	2.0	MHz
E-Clock Period	t_{cyc}	1000	—	500	—	ns
Peripheral Data Setup Time MCU Read of Ports A, C, D, and E	t_{PDSU}	100	—	100	—	ns
Peripheral Data Hold Time MCU Read of Ports A, C, D, and E	t_{PDH}	50	—	50	—	ns
Delay Time, Peripheral Data Write MCU Write to Port A MCU Writes to Ports B, C, and D t_{PWD} = 1/4 t_{cyc} + 150 ns	t_{PWD}	— —	250 400	— —	250 275	ns ns
Input Data Setup Time (Port C)	t_{IS}	60	—	60	—	ns
Input Data Hold Time (Port C)	t_{IH}	100	—	100	—	ns
Delay Time, E Fall to STRB t_{DEB} = 1/4 t_{cyc} + 150 ns	t_{DEB}	—	400	—	275	ns
Setup Time, STRA Asserted to E Fall (Note 1)	t_{AES}	0	—	0	—	ns
Delay Time, STRA Asserted to Port C Data Output Valid	t_{PCD}	—	100	—	100	ns
Hold Time, STRA Negated to Port C Data	t_{PCH}	10	—	10	—	ns
Three-State Hold Time	t_{PCZ}	—	150	—	150	ns

NOTES:

1. If this setup time is met, STRB acknowledges in the next cycle. If it is not met, the response may be delayed one more cycle.
2. Port C and D timing is valid for active drive (CWOM and DWOM bits not set in PIOC and SPCR registers respectively).
3. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.

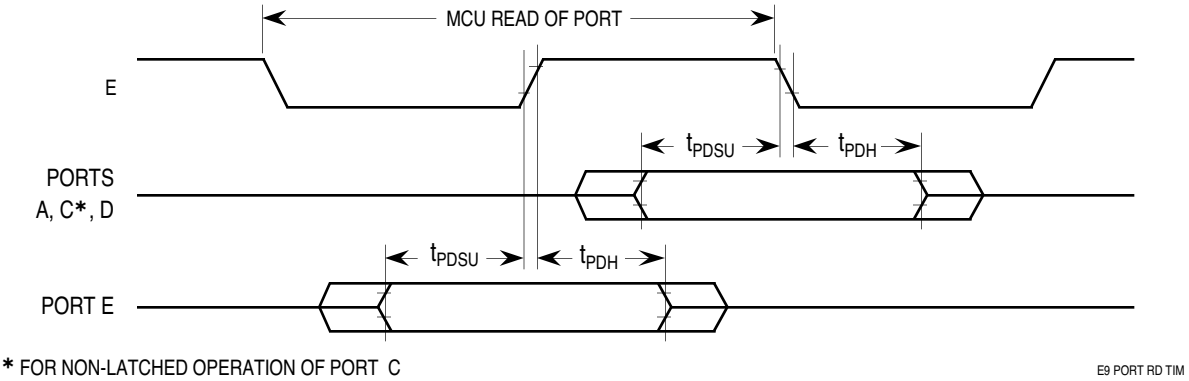


Figure A-7 Port Read Timing Diagram

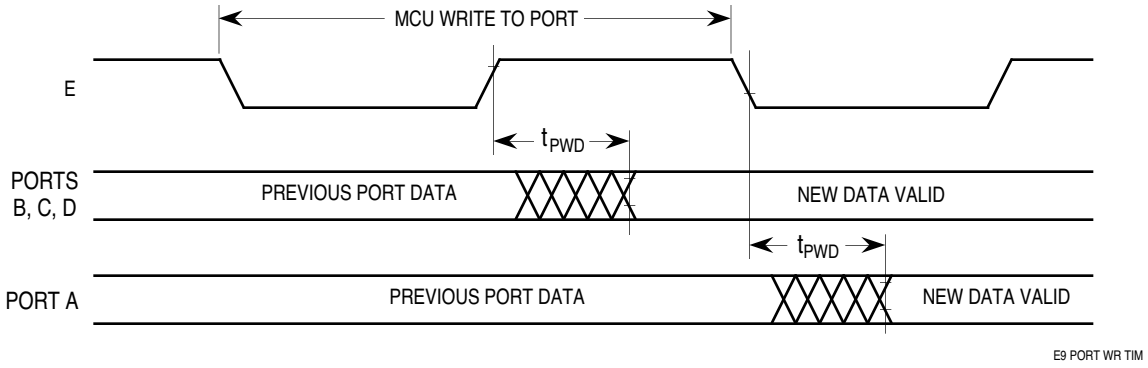


Figure A-8 Port Write Timing Diagram

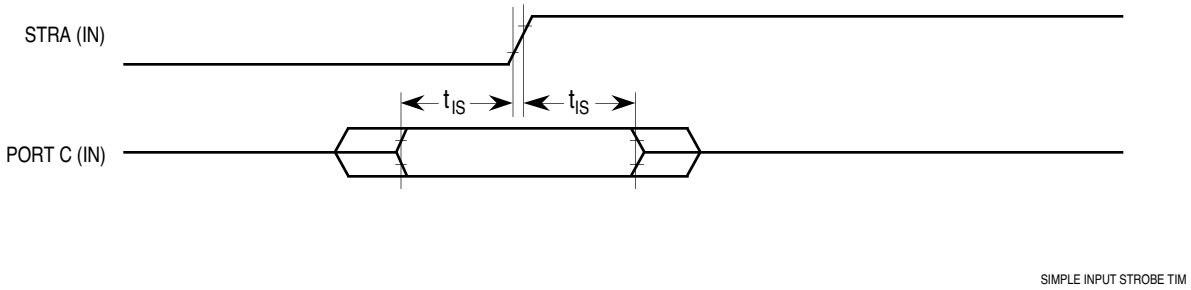


Figure A-9 Simple Input Strobe Timing Diagram

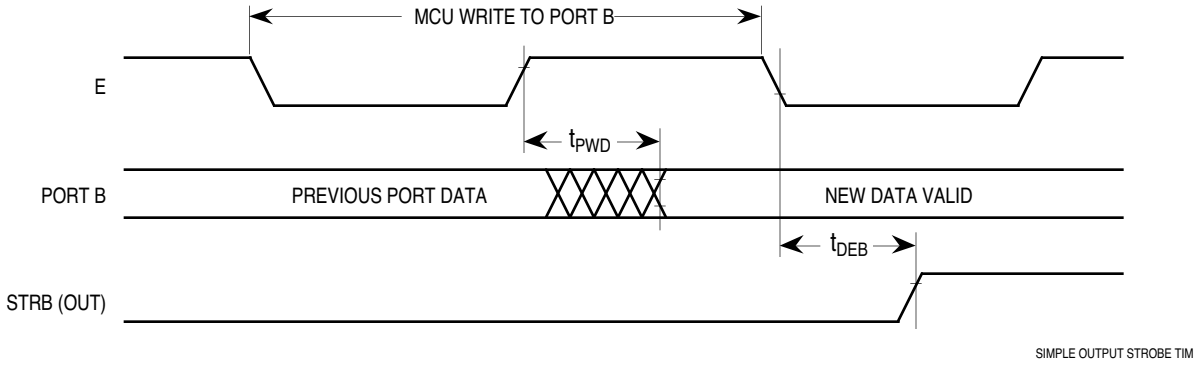
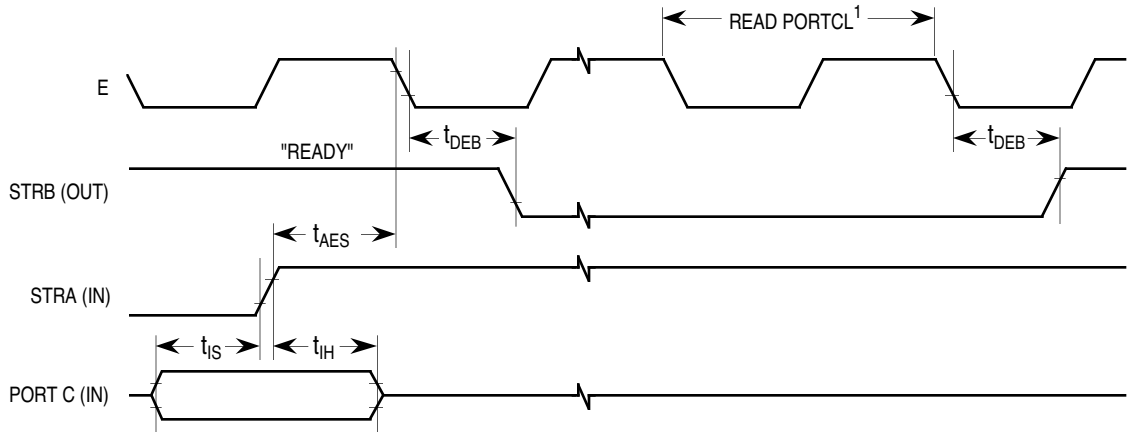


Figure A-10 Simple Output Strobe Timing Diagram



NOTES:
1. After reading PIOC with STAF set
2. Figure shows rising edge STRA (EGA = 1) and high true STRB (INVB = 1).

PORT C INPUT HNDSHK TIM

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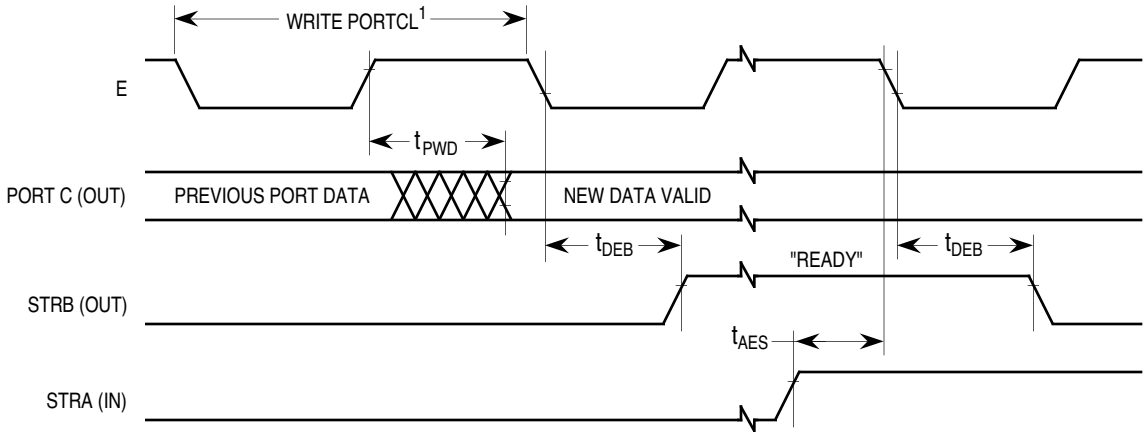
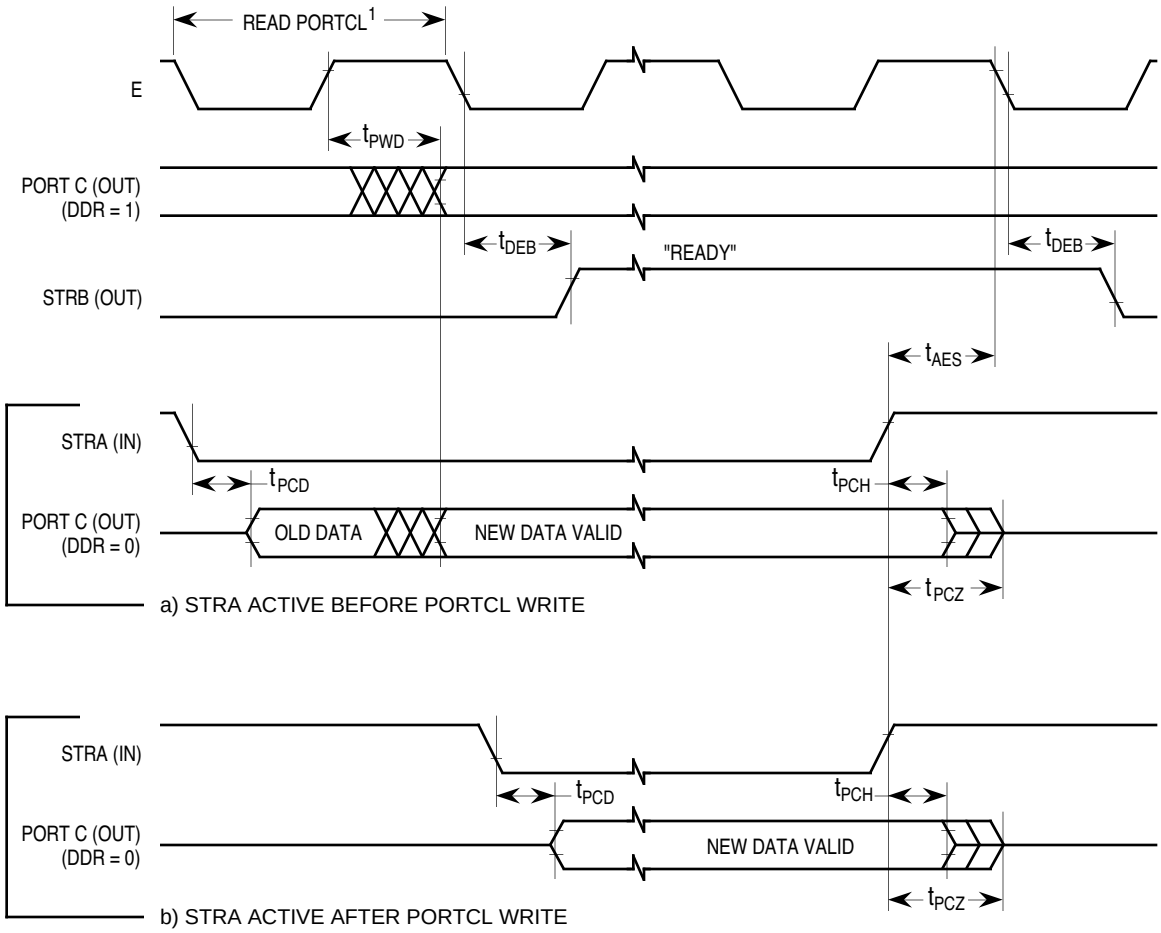
Figure A-11 Port C Input Handshake Timing Diagram



NOTES:
1. After reading PIOC with STAF set
2. Figure shows rising edge STRA (EGA = 1) and high true STRB (INVB = 1).

PORT C OUTPUT HNDSHK TIM

Figure A-12 Port C Output Handshake Timing Diagram



NOTES:
1. After reading PIOC with STAF set
2. Figure shows rising edge STRA (EGA = 1) and high true STRB (INVB = 1).

3-STATE VAR OUTPUT HNDSHK TIM

Figure A-13 Three-State Variation of Output Handshake Timing Diagram (STRA Enables Output Buffer)

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Table A-6 Analog-To-Digital Converter Characteristics

V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, 750 kHz ≤E ≤3.0 MHz, unless otherwise noted

Characteristic	Parameter	Min	Absolute	2.0 MHz	3.0 MHz	Unit
				Max	Max	
Resolution	Number of Bits Resolved by A/D Converter	—	8	—	—	Bits
Non-Linearity	Maximum Deviation from the Ideal A/D Transfer Characteristics	—	—	±1/2	±1	LSB
Zero Error	Difference Between the Output of an Ideal and an Actual for Zero Input Voltage	—	—	±1/2	±1	LSB
Full Scale Error	Difference Between the Output of an Ideal and an Actual A/D for Full-Scale Input Voltage	—	—	±1/2	±1	LSB
Total Unadjusted Error	Maximum Sum of Non-Linearity, Zero Error, and Full-Scale Error	—	—	±1/2	±1 1/2	LSB
Quantization Error	Uncertainty Because of Converter Resolution	—	—	±1/2	±1/2	LSB
Absolute Accuracy	Difference Between the Actual Input Voltage and the Full-Scale Weighted Equivalent of the Binary Output Code, All Error Sources Included	—	—	±1	±2	LSB
Conversion Range	Analog Input Voltage Range	V_{RL}	—	V_{RH}	V_{RH}	V
V_{RH}	Maximum Analog Reference Voltage (Note 2)	V_{RL}	—	V_{DD} + 0.1	V_{DD} + 0.1	V
V_{RL}	Minimum Analog Reference Voltage (Note 2)	V_{SS} -0.1	—	V_{RH}	V_{RH}	V
ΔV_R	Minimum Difference between V_{RH} and V_{RL} (Note 2)	3	—	—	—	V
Conversion Time	Total Time to Perform a Single Analog-to-Digital Conversion:					
	E Clock	—	32	—	—	t_{cyc}
	Internal RC Oscillator	—	—	t_{cyc} + 32	t_{cyc} + 32	µs
Monotonicity	Conversion Result Never Decreases with an Increase in Input Voltage and has no Missing Codes	—	Guaranteed	—	—	—
Zero Input Reading	Conversion Result when $V_{in} = V_{RL}$	00	—	—	—	Hex
Full Scale Reading	Conversion Result when $V_{in} = V_{RH}$	—	—	FF	FF	Hex
Sample Acquisition Time	Analog Input Acquisition Sampling Time:					
	E Clock	—	12	—	—	t_{cyc}
	Internal RC Oscillator	—	—	12	12	µs
Sample/Hold Capacitance	Input Capacitance During Sample PE[7:0]	—	20 (Typ)	—	—	pF
Input Leakage	Input Leakage on A/D Pins PE[7:0]	—	—	400	400	nA
	V_{RL}, V_{RH}	—	—	1.0	1.0	µA

NOTES:

1. Source impedances greater than 10 kΩ affect accuracy adversely because of input leakage.
2. Performance verified down to 2.5 V ΔV_R, but accuracy is tested and guaranteed at ΔV_R = 5 V ±10%.

Table A-6a Analog-To-Digital Converter Characteristics (MC68L11E9)

V_{DD} = 3.0 Vdc to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, 750 kHz ≤E ≤2.0 MHz, unless otherwise noted

Characteristic	Parameter	Min	Absolute	Max	Unit
Resolution	Number of Bits Resolved by A/D Converter	—	8	—	Bits
Non-Linearity	Maximum Deviation from the Ideal A/D Transfer Characteristics	—	—	±1	LSB
Zero Error	Difference Between the Output of an Ideal and an Actual for Zero Input Voltage	—	—	±1	LSB
Full Scale Error	Difference Between the Output of an Ideal and an Actual A/D for Full-Scale Input Voltage	—	—	±1	LSB
Total Unadjusted Error	Maximum Sum of Non-Linearity, Zero Error, and Full-Scale Error	—	—	±1 1/2	LSB
Quantization Error	Uncertainty Because of Converter Resolution	—	—	±1/2	LSB
Absolute Accuracy	Difference Between the Actual Input Voltage and the Full-Scale Weighted Equivalent of the Binary Output Code, All Error Sources Included	—	—	±2	LSB
Conversion Range	Analog Input Voltage Range	V_{RL}	—	V_{RH}	V
V_{RH}	Maximum Analog Reference Voltage	V_{RL}	—	V_{DD} + 0.1	V
V_{RL}	Minimum Analog Reference Voltage	V_{SS} –0.1	—	V_{RH}	V
ΔV_R	Minimum Difference between V_{RH} and V_{RL}	3.0	—	—	V
Conversion Time	Total Time to Perform a Single Analog-to-Digital Conversion:				
	E Clock	—	32	—	t_{cyc}
	Internal RC Oscillator	—	—	t_{cyc} + 32	µs
Monotonicity	Conversion Result Never Decreases with an Increase in Input Voltage and has no Missing Codes	—	Guaranteed	—	—
Zero Input Reading	Conversion Result when $V_{in} = V_{RL}$	00	—	—	Hex
Full Scale Reading	Conversion Result when $V_{in} = V_{RH}$	—	—	FF	Hex
Sample Acquisition Time	Analog Input Acquisition Sampling Time:				
	E Clock	—	12	—	t_{cyc}
	Internal RC Oscillator	—	—	12	µs
Sample/Hold Capacitance	Input Capacitance During Sample PE[7:0]	—	20 (Typ)	—	pF
Input Leakage	Input Leakage on A/D Pins PE[7:0]	—	—	400	nA
	V_{RL}, V_{RH}	—	—	1.0	µA

NOTES:

1. Source impedances greater than 10 kΩ affect accuracy adversely because of input leakage.

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Table A-7 Expansion Bus Timing

V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H

Num	Characteristic	Symbol	1.0 MHz		2.0 MHz		3.0 MHz		Unit
			Min	Max	Min	Max	Min	Max	
	Frequency of Operation (E-Clock Frequency)	f_o	dc	1.0	dc	2.0	dc	3.0	MHz
1	Cycle Time	t_{cyc}	1000	—	500	—	333	—	ns
2	Pulse Width, E Low PW_{EL} = 1/2 t_{cyc} –23 ns (Note 1)	PW_{EL}	477	—	227	—	146	—	ns
3	Pulse Width, E High PW_{EH} = 1/2 t_{cyc} –28 ns (Note 1)	PW_{EH}	472	—	222	—	141	—	ns
4a 4b	E and AS Rise Time E and AS Fall Time	t_r t_f	— —	20 20	— —	20 20	— —	20 15	ns
9	Address Hold Time t_{AH} = 1/8 t_{cyc} –29.5 ns (Note 1, 2a)	t_{AH}	95.5	—	33	—	26	—	ns
12	Nonmultiplexed Address Valid Time to E Rise $t_{AV} = PW_{EL} – (t_{ASD} + 80$ ns) (Note 1, 2a)	t_{AV}	281.5	—	94	—	54	—	ns
17	Read Data Setup Time	t_{DSR}	30	—	30	—	30	—	ns
18	Read Data Hold Time (Max = t_{MAD})	t_{DHR}	0	145.5	0	83	0	51	ns
19	Write Data Delay Time t_{DDW} = 1/8 t_{cyc} + 65.5 ns (Note 1, 2a)	t_{DDW}	—	190.5	—	128		71	ns
21	Write Data Hold Time t_{DHW} = 1/8 t_{cyc} –29.5 ns (Note 1, 2a)	t_{DHW}	95.5	—	33	—	26	—	ns
22	Multiplexed Address Valid Time to E Rise $t_{AVM} = PW_{EL} – (t_{ASD} + 90$ ns) (Note 1, 2a)	t_{AVM}	271.5	—	84	—	54	—	ns
24	Multiplexed Address Valid Time to AS Fall $t_{ASL} = PW_{ASH}$ –70 ns (Note 1)	t_{ASL}	151	—	26	—	13	—	ns
25	Multiplexed Address Hold Time t_{AHL} = 1/8 t_{cyc} –29.5 ns (Note 1, 2b)	t_{AHL}	95.5	—	33	—	31	—	ns
26	Delay Time, E to AS Rise t_{ASD} = 1/8 t_{cyc} –9.5 ns (Note 1, 2a)	t_{ASD}	115.5	—	53	—	31	—	ns
27	Pulse Width, AS High PW_{ASH} = 1/4 t_{cyc} –29 ns (Note 1)	PW_{ASH}	221	—	96	—	63	—	ns
28	Delay Time, AS to E Rise t_{ASED} = 1/8 t_{cyc} –9.5 ns (Note 1, 2b)	t_{ASED}	115.5	—	53	—	31	—	ns
29	MPU Address Access Time (Note 2a) $t_{ACCA} = t_{cyc} – (PW_{EL} – t_{AVM}) – t_{DSR} – t_f$	t_{ACCA}	744.5	—	307	—	196	—	ns
35	MPU Access Time $t_{ACCE} = PW_{EH} – t_{DSR}$	t_{ACCE}	—	442	—	192		111	ns
36	Multiplexed Address Delay (Previous Cycle MPU Read) $t_{MAD} = t_{ASD}$ + 30 ns (Note 1, 2a)	t_{MAD}	145.5	—	83	—	51	—	ns

1. Formula only for dc to 2 MHz.
2. Input clocks with duty cycles other than 50% affect bus performance. Timing parameters affected by input clock duty cycle are identified by (a) and (b). To recalculate the approximate bus timing values, substitute the following expressions in place of 1/8 t_{cyc} in the above formulas, where applicable:
   (a) (1–DC) × 1/4 t_{cyc}
   (b) DC × 1/4 t_{cyc}
   Where:
   DC is the decimal value of duty cycle percentage (high time).
3. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.

Table A-7a Expansion Bus Timing (MC68L11E9)

V_{DD} = 3.0 Vdc to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H

Num	Characteristic	Symbol	1.0 MHz		2.0 MHz		Unit
			Min	Max	Min	Max	
	Frequency of Operation (E-Clock Frequency)	f_o	dc	1.0	dc	2.0	MHz
1	Cycle Time	t_{cyc}	1000	—	500	—	ns
2	Pulse Width, E Low $PW_{EL} = 1/2\ t_{cyc} - 25$ ns	PW_{EL}	475	—	225	—	ns
3	Pulse Width, E High $PW_{EH} = 1/2\ t_{cyc} - 30$ ns	PW_{EH}	470	—	220	—	ns
4A 4B	E and AS Rise Time E and AS Fall Time	t_r t_f	— —	25 25	— —	25 25	ns ns
9	Address Hold Time $t_{AH} = 1/8\ t_{cyc} - 30$ ns (Note 1a)	t_{AH}	95	—	33	—	ns
12	Nonmultiplexed Address Valid Time to E Rise $t_{AV} = PW_{EL} - (t_{ASD} + 80$ ns) (Note 1a)	t_{AV}	275	—	88	—	ns
17	Read Data Setup Time	t_{DSR}	30	—	30	—	ns
18	Read Data Hold Time (Max = t_{MAD})	t_{DHR}	0	150	0	88	ns
19	Write Data Delay Time $t_{DDW} = 1/8\ t_{cyc} + 70$ ns (Note 1a)	t_{DDW}	—	195	—	133	ns
21	Write Data Hold Time $t_{DHW} = 1/8\ t_{cyc} - 30$ ns (Note 1a)	t_{DHW}	95	—	33	—	ns
22	Multiplexed Address Valid Time to E Rise $t_{AVM} = PW_{EL} - (t_{ASD} + 90$ ns) (Note 1a)	t_{AVM}	265	—	78	—	ns
24	Multiplexed Address Valid Time to AS Fall $t_{ASL} = PW_{ASH} - 70$ ns	t_{ASL}	150	—	25	—	ns
25	Multiplexed Address Hold Time $t_{AHL} = 1/8\ t_{cyc} - 30$ ns (Note 1b)	t_{AHL}	95	—	33	—	ns
26	Delay Time, E to AS Rise $t_{ASD} = 1/8\ t_{cyc} - 5$ ns (Note 1a)	t_{ASD}	120	—	58	—	ns
27	Pulse Width, AS High $PW_{ASH} = 1/4\ t_{cyc} - 30$ ns	PW_{ASH}	220	—	95	—	ns
28	Delay Time, AS to E Rise $t_{ASED} = 1/8\ t_{cyc} - 5$ ns (Note 1b)	t_{ASED}	120	—	58	—	ns
29	MPU Address Access Time (Note 1a) $t_{ACCA} = t_{cyc} - (PW_{EL} - t_{AVM}) - t_{DSR} - t_f$	t_{ACCA}	735	—	298	—	ns
35	MPU Access Time $t_{ACCE} = PW_{EH} - t_{DSR}$	t_{ACCE}	—	440	—	190	ns
36	Multiplexed Address Delay (Previous Cycle MPU Read) $t_{MAD} = t_{ASD} + 30$ ns (Note 1a)	t_{MAD}	150	—	88	—	ns

NOTES:

1. Input clocks with duty cycles other than 50% affect bus performance. Timing parameters affected by input clock duty cycle are identified by (a) and (b). To recalculate the approximate bus timing values, substitute the following expressions in place of $1/8\ t_{cyc}$ in the above formulas, where applicable:
   (a) $(1–DC) \times 1/4\ t_{cyc}$
   (b) $DC \times 1/4\ t_{cyc}$
   Where:
   DC is the decimal value of duty cycle percentage (high time).
2. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.

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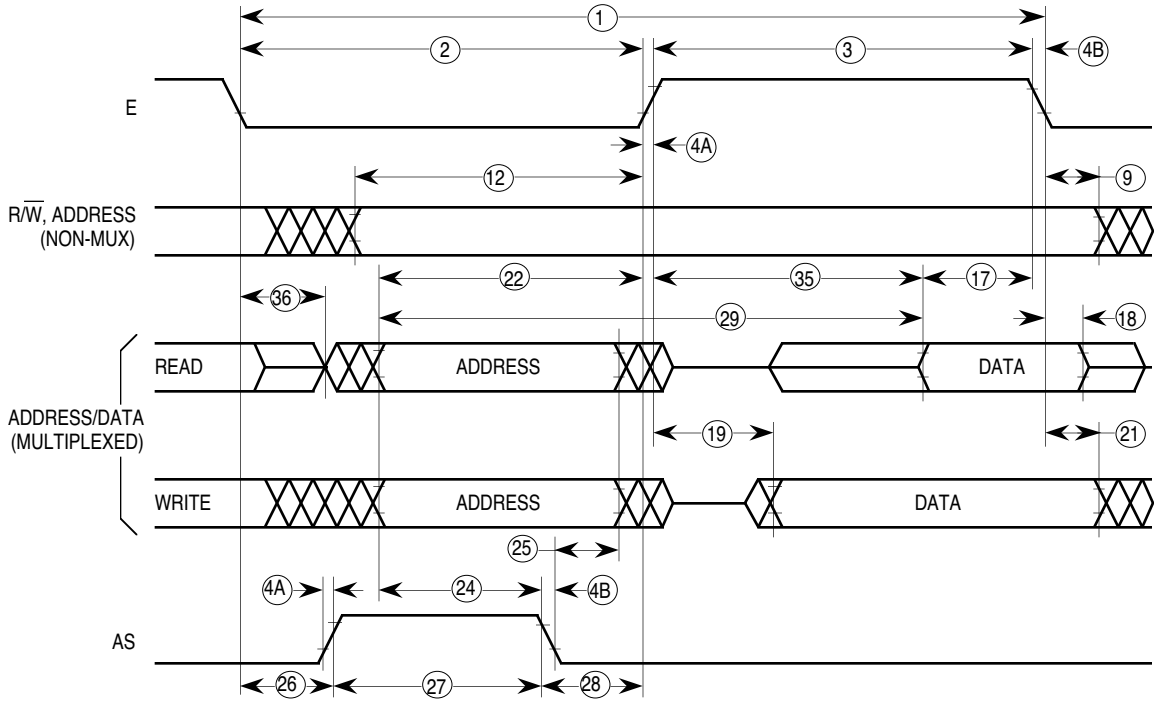

NOTE: Measurement points shown are 20% and 70% of V_{DD}.

MUX BUS TIM

Figure A-14 Multiplexed Expansion Bus Timing Diagram

Table A-8 Serial Peripheral Interface Timing

V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H

Num	Characteristic	Symbol	2.0 MHz		3.0 MHz		Unit
			Min	Max	Min	Max	
	Operating Frequency Master Slave	 $f_{op(m)}$ $f_{op(s)}$	 dc dc	 0.5 2.0	 dc dc	 0.5 3.0	f_{op} MHz
1	Cycle Time Master Slave	 $t_{cyc(m)}$ $t_{cyc(s)}$	 2.0 500	 — —	 2.0 333	 — —	t_{cyc} ns
2	Enable Lead Time Master (Note 2) Slave	 $t_{lead(m)}$ $t_{lead(s)}$	 — 250	 — —	 — 240	 — —	 ns ns
3	Enable Lag Time Master (Note 2) Slave	 $t_{lag(m)}$ $t_{lag(s)}$	 — 250	 — —	 — 240	 — —	 ns ns
4	Clock (SCK) High Time Master Slave	 $t_{w(SCKH)m}$ $t_{w(SCKH)s}$	 340 190	 — —	 227 127	 — —	 ns ns
5	Clock (SCK) Low Time Master Slave	 $t_{w(SCKL)m}$ $t_{w(SCKL)s}$	 340 190	 — —	 227 127	 — —	 ns ns
6	Data Setup Time (Inputs) Master Slave	 $t_{su(m)}$ $t_{su(s)}$	 100 100	 — —	 100 100	 — —	 ns ns
7	Data Hold Time (Inputs) Master Slave	 $t_{h(m)}$ $t_{h(s)}$	 100 100	 — —	 100 100	 — —	 ns ns
8	Access Time (Time to Data Active from High-Impedance State) Slave	 t_a	 0	 120	 0	 120	 ns
9	Disable Time (Hold Time to High-Impedance State) Slave	 t_{dis}	 —	 240	 —	 167	 ns
10	Data Valid (After Enable Edge) (Note 3)	$t_{v(s)}$	—	240	—	167	ns
11	Data Hold Time (Outputs) (After Enable Edge)	t_{ho}	0	—	0	—	ns
12	Rise Time (20% V_{DD} to 70% V_{DD}, C_L = 200 pF) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and $\overline{SS}$)	 t_{rm} t_{rs}	 — —	 100 2.0	 — —	 100 2.0	 ns µs
13	Fall Time (70% V_{DD} to 20% V_{DD}, C_L = 200 pF) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and $\overline{SS}$)	 t_{fm} t_{fs}	 — —	 100 2.0	 — —	 100 2.0	 ns µs

1. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.
2. Signal production depends on software.
3. Assumes 200 pF load on SCK, MOSI, and MISO pins.

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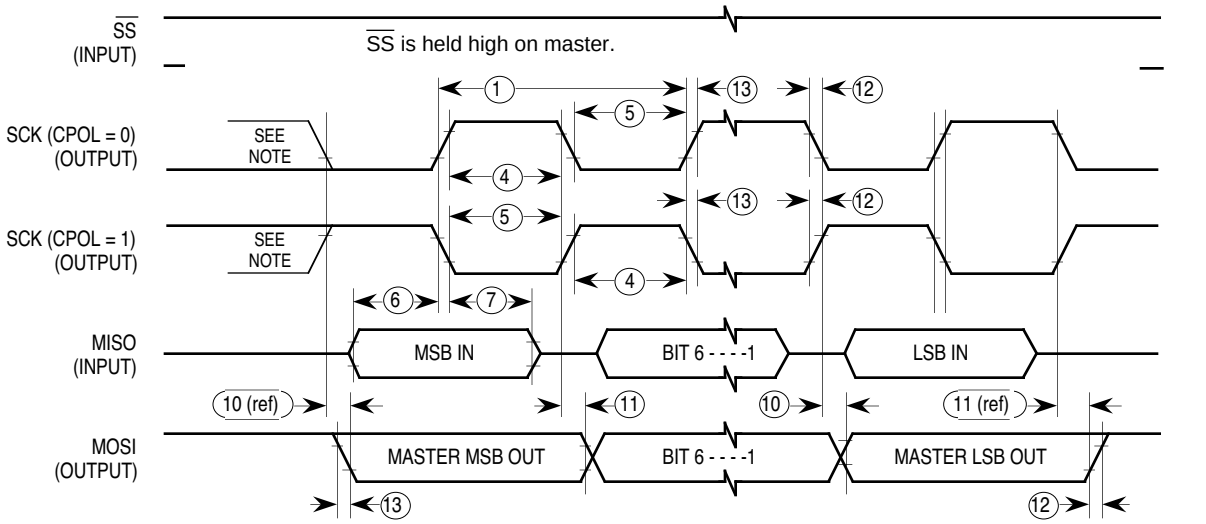
Table A-8a Serial Peripheral Interface Timing (MC68L11E9)

Num	Characteristic	Symbol	1.0 MHz		2.0 MHz		Unit
			Min	Max	Min	Max	
	Operating Frequency Master Slave	 $f_{op(m)}$ $f_{op(s)}$	 dc dc	 0.5 1.0	 dc dc	 0.5 2.0	 f_{op} MHz
1	Cycle Time Master Slave	 $t_{cyc(m)}$ $t_{cyc(s)}$	 2.0 1000	 — —	 2.0 500	 — —	 t_{cyc} ns
2	Enable Lead Time Master (Note 2) Slave	 $t_{lead(m)}$ $t_{lead(s)}$	 — 500	 — —	 — 250	 — —	 ns ns
3	Enable Lag Time Master (Note 2) Slave	 $t_{lag(m)}$ $t_{lag(s)}$	 — 500	 — —	 — 250	 — —	 ns ns
4	Clock (SCK) High Time Master Slave	 $t_{w(SCKH)m}$ $t_{w(SCKH)s}$	 680 380	 — —	 340 190	 — —	 ns ns
5	Clock (SCK) Low Time Master Slave	 $t_{w(SCKL)m}$ $t_{w(SCKL)s}$	 680 380	 — —	 340 190	 — —	 ns ns
6	Data Setup Time (Inputs) Master Slave	 $t_{su(m)}$ $t_{su(s)}$	 100 100	 — —	 100 100	 — —	 ns ns
7	Data Hold Time (Inputs) Master Slave	 $t_{h(m)}$ $t_{h(s)}$	 100 100	 — —	 100 100	 — —	 ns ns
8	Access Time (Time to Data Active from High-Impedance State) Slave	t_a	0	120	0	120	ns
9	Disable Time (Hold Time to High-Impedance State) Slave	t_{dis}	—	240	—	240	ns
10	Data Valid (After Enable Edge) (Note 3)	$t_{v(s)}$	—	240	—	240	ns
11	Data Hold Time (Outputs) (After Enable Edge)	t_{ho}	0	—	0	—	ns
12	Rise Time (20% V_{DD} to 70% V_{DD}, C_L = 200 pF) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and $\overline{SS}$)	 t_{rm} t_{rs}	 — —	 100 2.0	 — —	 100 2.0	 ns µs
13	Fall Time (70% V_{DD} to 20% V_{DD}, C_L = 200 pF) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and $\overline{SS}$)	 t_{fm} t_{fs}	 — —	 100 2.0	 — —	 100 2.0	 ns µs

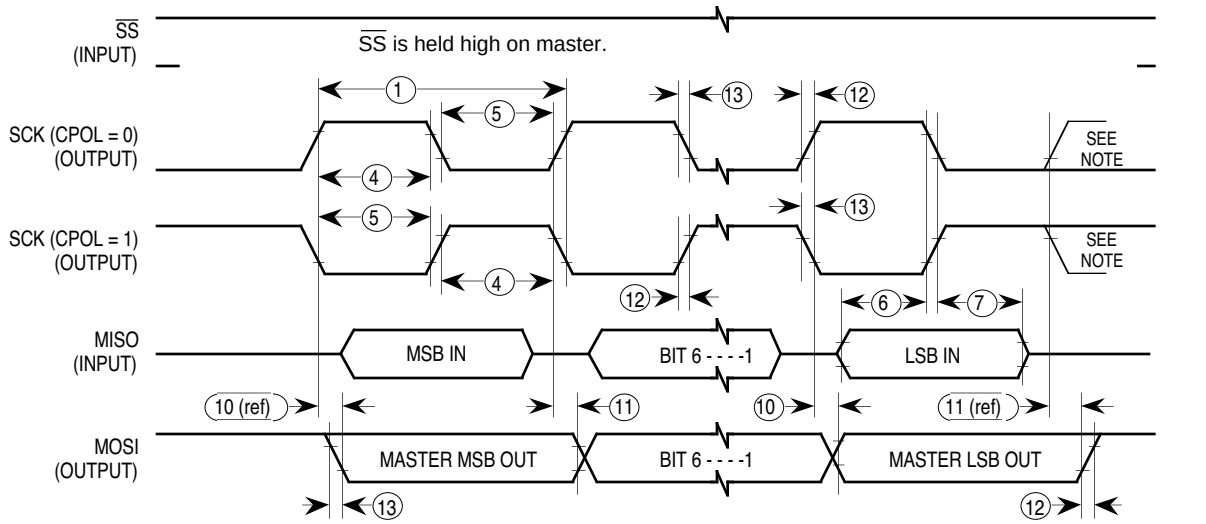
NOTES:

1. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.
2. Signal production depends on software.
3. Assumes 100 pF load on all SPI pins.



NOTE: This first clock edge is generated internally but is not seen at the SCK pin.

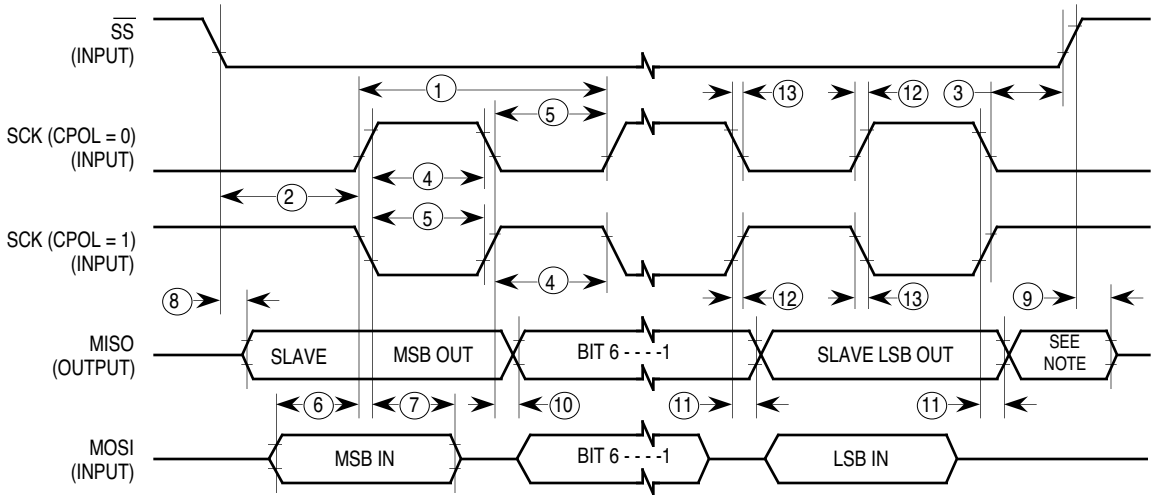
a) SPI Master Timing (CPHA = 0)



NOTE: This last clock edge is generated internally but is not seen at the SCK pin.

b) SPI Master Timing (CPHA = 1)

Figure A-15 SPI Timing Diagram (1 of 2)

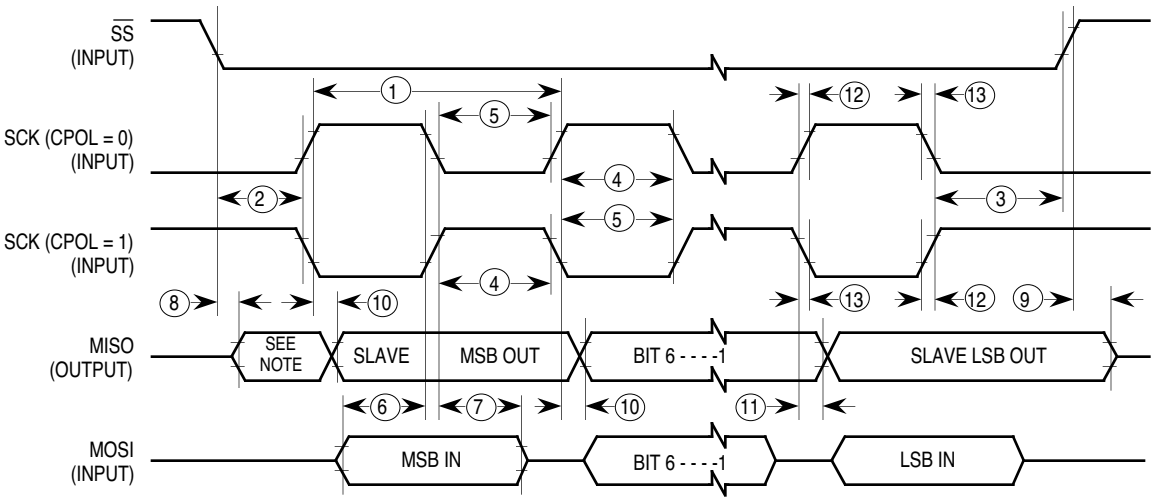


NOTE: Not defined but normally MSB of character just received.

SPI SLAVE CPHA0 TIM

A

a) SPI Slave Timing (CPHA = 0)



NOTE: Not defined but normally LSB of character previously transmitted.

SPI SLAVE CPHA1 TIM

b) SPI Slave Timing (CPHA = 1)

Figure A-15 SPI Timing Diagram (2 of 2)

Table A-9 EEPROM Characteristics

V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H

Characteristic		Temperature Range			Unit
		–40 to 85°C	**–40 to 105°C**	**–40 to 125°C**	
Programming Time (Note 1)	<1.0 MHz, RCO Enabled 1.0 to 2.0 MHz, RCO Disabled ≥2.0 MHz (or Anytime RCO Enabled)	10 20 10	15 Must use RCO 15	20 Must use RCO 20	ms
Erase Time (Note 1)	Byte, Row and Bulk	10	10	10	ms
Write/Erase Endurance (Note 2)		10,000	10,000	10,000	Cycles
Data Retention (Note 2)		10	10	10	Years

NOTES:

1. The RC oscillator (RCO) must be enabled (by setting the CSEL bit in the OPTION register) for EEPROM programming and erasure when the E-clock frequency is below 1.0 MHz.
2. Refer to Reliability Monitor Report (current quarterly issue) for current failure rate information.

Table A-9a EEPROM Characteristics (MC68L11E9)

V_{DD} = 3.0 Vdc to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H

Characteristic		Temperature Range **–20 to 70°C**	Unit
Programming Time (Note 1)	3 V, E ≤ 2.0 MHz, RCO Enabled 5 V, E ≤ 2.0 MHz, RCO Enabled	25 10	ms ms
Erase Time (Byte, Row and Bulk) (Note 1)	3 V, E ≤ 2.0 MHz, RCO Enabled 5 V, E ≤ 2.0 MHz, RCO Enabled	25 10	ms ms
Write/Erase Endurance (Note 2)		10,000	Cycles
Data Retention (Note 2)		10	Years

NOTES:

1. The RC oscillator (RCO) must be enabled (by setting the CSEL bit in the OPTION register) for EEPROM programming and erasure.
2. Refer to Reliability Monitor Report (current quarterly issue) for current failure rate information.

A

A