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THÈME :

Commande numérique pour réseau ferroviaire de modélisme

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Lons-le-Saunier

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Dossier élève

Table des matières

LE SYSTÈME TECHNIQUE

1 Mise en situation du système technique

1-1 Introduction

Il est assez remarquable de constater l'importance que prend aujourd'hui l'électronique dans les jouets. Et s'il est un domaine dans lequel cette importance s'est profondément accrue depuis une quinzaine d'années, c'est bien le modélisme et en particulier le modélisme ferroviaire.

Pour satisfaire les exigences des passionnés de modélisme ferroviaire, les fabricants ont exploité le domaine des réseaux industriels à courant porteur. Les deux rails sont utilisés pour transporter l'énergie et communiquer toutes les informations utiles, aux locomotives et aux accessoires. C'est ainsi que de nombreux fabricants proposent des « coffrets avec commande digitale ». Grâce à cette nouvelle commande, le train miniature se fait toujours plus ludique et sophistiqué ! Aujourd'hui, un train ne se contente pas de rouler avec des feux qui éclairent, il siffle, il fume, il fait « tchou-tchou », il attelle et dételle et suit l'itinéraire qu'on lui commande de prendre, tout cela le plus simplement du monde... ou presque !

1-2 Éléments constitutifs du système réel

Le système digital minimal est formé d'une unité centrale associée à un amplificateur (booster), qui génère le courant codé appliqué à la voie, et de décodeurs embarqués dans les locomotives. L'unité centrale comprend, dans certains cas, les organes de commande qui permettent à l'utilisateur de contrôler les trains, dans d'autres cas, il est fait appel à un ou plusieurs boîtiers de commande séparés.

L'alimentation :

La souris :

Elle permet de commander 99 systèmes différents (locomotives ou accessoires).

Le booster :

Permet d'envoyer sur les voies l'énergie et l'information.

Une locomotive :

1-3 Approche des milieux

Milieu humain :

L'opérateur agit aux commandes d'un régleur manuel pour modifier les trajectoires des trains, la vitesse des trains, la signalisation ….

Il doit aussi effectuer la mise en oeuvre et les opérations de maintenance. L'opérateur peut être aussi bien un enfant qu'un adulte.

Milieu Physique :

Le système est utilisé dans une habitation classique avec des conditions de température et d'hygrométrie classique.

Milieu technique :

On dispose de l'alimentation secteur 230 Veff – 50 Hz. Les différents éléments constituant le système sont remplaçables facilement par l'utilisateur : les décodeurs, les locomotives, les rails, l'unité de commande, le booster…

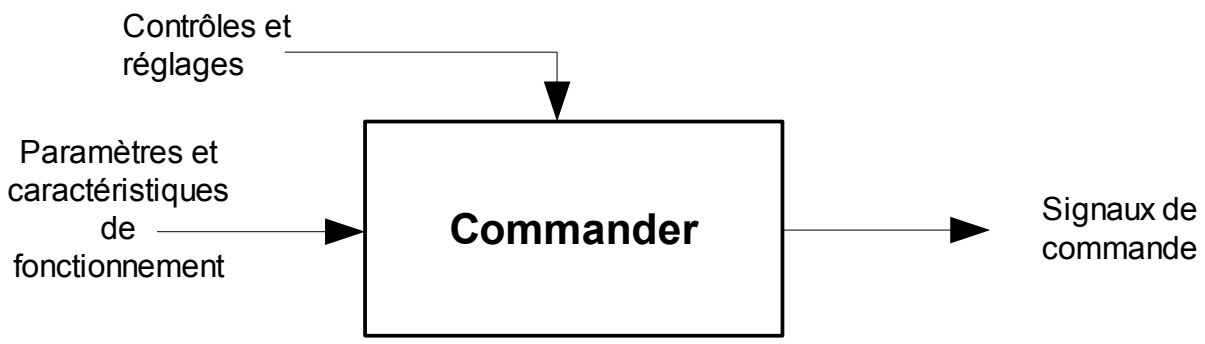
Milieu économique :

Ce système fait partie de l'industrie du jouet. On trouve un grand nombre de fabricants de décodeurs, d'unités de commande, de boosters, de logiciels, de rails, de trains, etc.

Les plus connus sont : MARKLIN, LENZ, ROCO, SELECTRIX, VIESSMANN…

Le prix de revient de l'équipement de base dépasse rapidement les 300 €. Les concurrents étant de plus en plus nombreux, le prix du matériel diminue fortement.

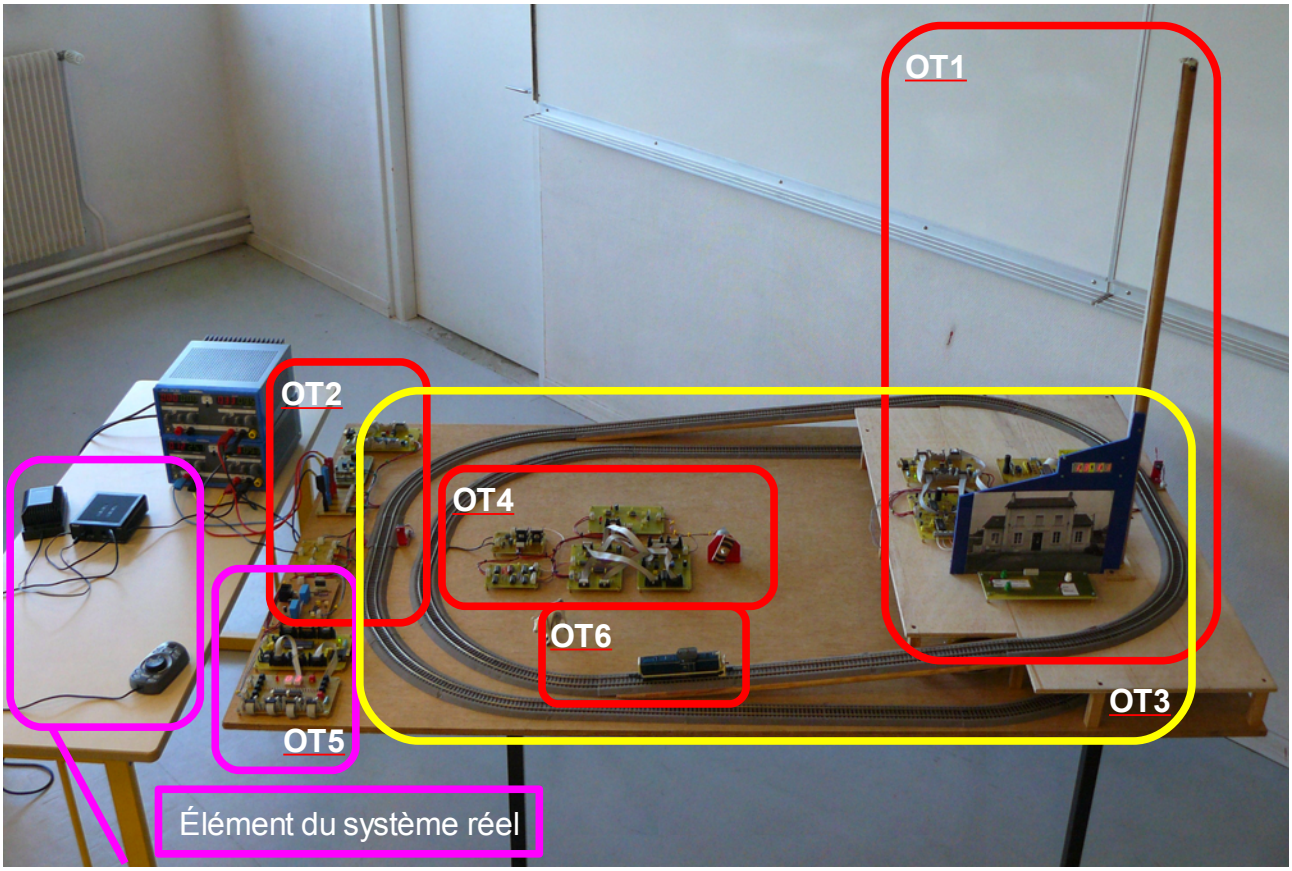
1-4 Schéma fonctionnel de niveau I



2 Le système technique étudié

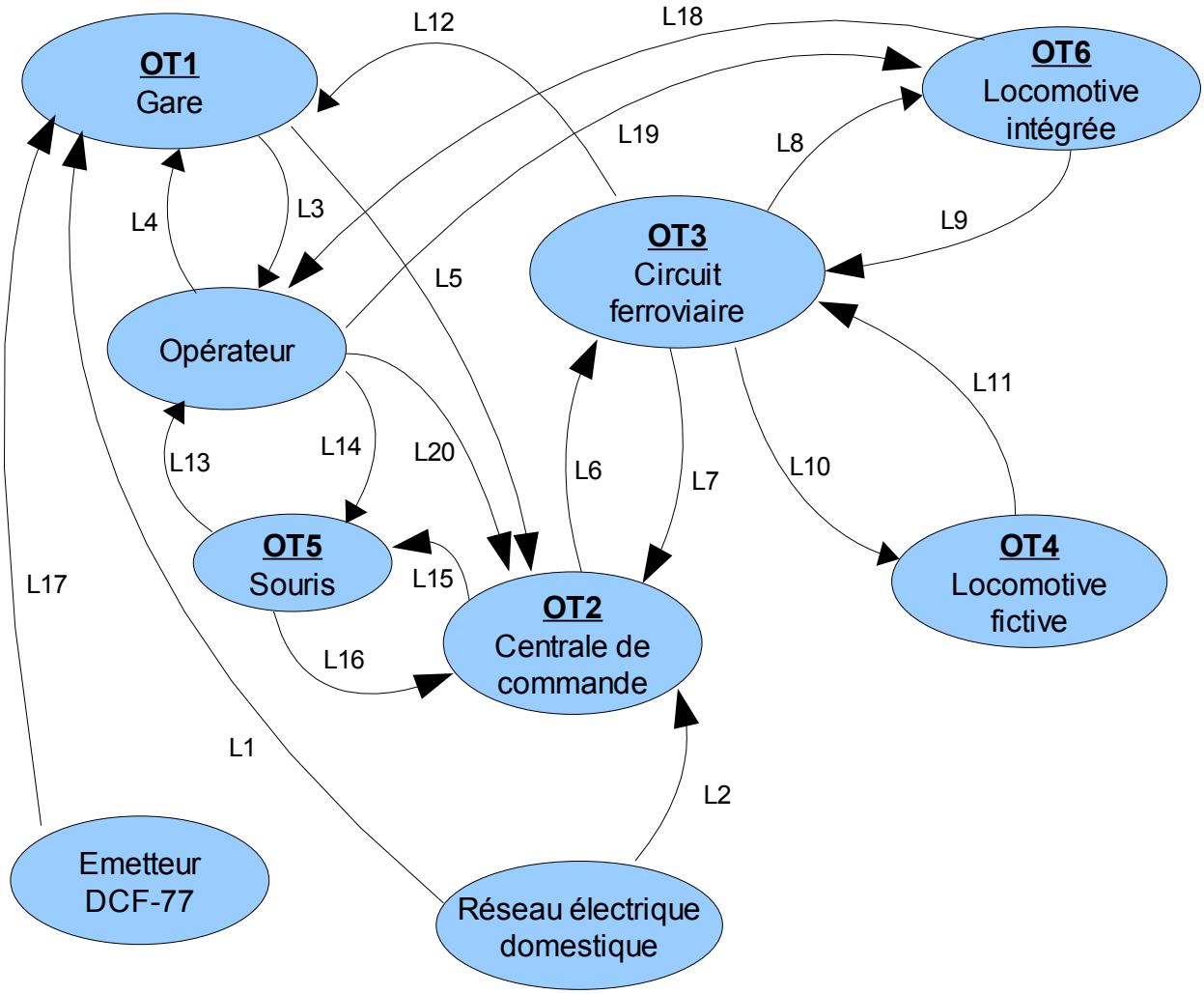
2-1 Présentation

Le système technique étudié est composé de 6 objets techniques différents, auxquels s'ajoutent le système technique réel.



Les objets techniques OT3 (le circuit ferroviaire) et OT6 (la locomotive intégré) ne seront pas étudiés.

2-2 Diagramme sagittal du système



L1 : Énergie issue du réseau EDF (ou similaire).

L2 : Énergie issue du réseau EDF (ou similaire).

L3 : Information visuelle.

L4 : Action manuelle.

L5 : Signal informationnel radio sur l'état de présence du train.

L6 : Signal informationnel et énergétique au format DCC NMRA.

L7 : Information sur une anomalie électrique (protection des personnes et des biens).

L8 : Signal informationnel et énergétique au format DCC NMRA dédié aux motrices.

L9 : Déplacement.

L10 : Signal informationnel et énergétique au format DCC NMRA dédié aux accessoires.

L11 : Déplacement.

L12 : Signal informationnel sur le passage du train

L13 : Information visuelle.

L14 : Action manuelle.

L15 : Signal informationnel sur l'état de fonctionnement.

L16 : Informations de commande.

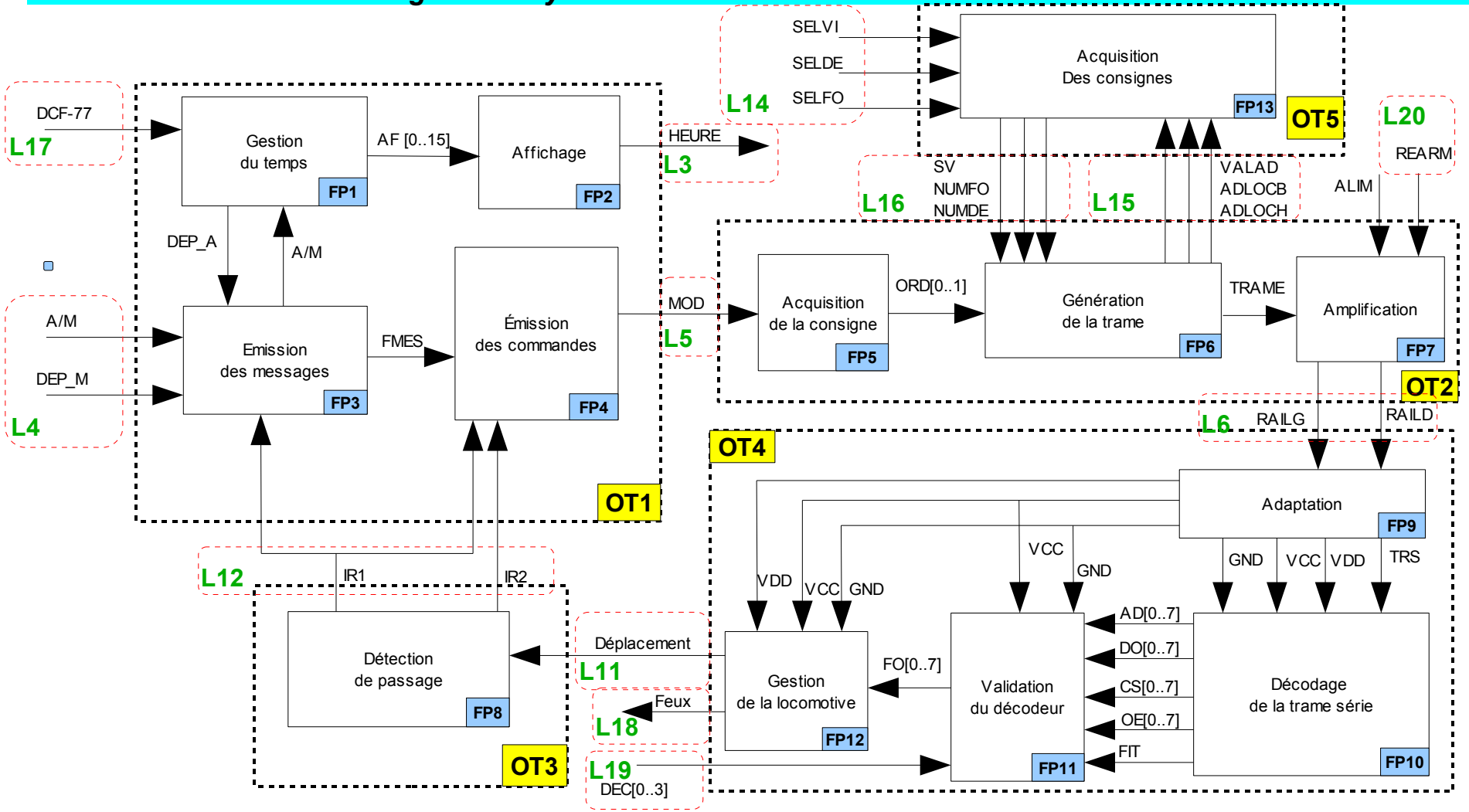
L17 : Signal informationnel radio au format DCF-77 dédié à l'heure (60 impulsions).

L18 : Information visuelle.

L19 : Information de réglage.

L20 : Information de réglage.

3 Schéma fonctionnel de degré 1 du système étudié



4 Fonctionnement du système étudié

4-1 Fonctionnement de la gare

- Fonctionnement manuel : A l'appui sur le poussoir de départ, un message sonore avertit l'usager du départ imminent du train. Celui-ci part en vitesse rapide.

  Au passage du détecteur situé peu avant la gare, un message sonore avertit de l'arrivée imminente du train.

  Celui-ci ralentit avant d'entrer en gare.

  A l'arrivée en gare le train stoppe, il attend un nouveau départ par l'appui sur le poussoir de départ.

- Fonctionnement automatique : Même fonctionnement que précédemment, mais le départ du train s'effectue toutes les minutes.

4-2 Utilisation de la souris OT5

Il est possible de commander des trains par l'intermédiaire de la "souris" réalisée. On commande :

- Choix de la locomotive à commander.
- Sens de déplacement de la locomotive.
- Vitesse de déplacement de la locomotive.

4-3 Fonctionnement de la locomotive fictive OT4

Une locomotive fictive est réalisée, afin de décoder à l'aide de composants discrets la trame DCC NMRA reçue. Celle-ci se commande soit par l'intermédiaire de la souris réalisée, soit par la souris ROCO©.

OT1 Gare

1 Mise en situation du système technique

1-1 Introduction

La gare réalisée doit permettre :

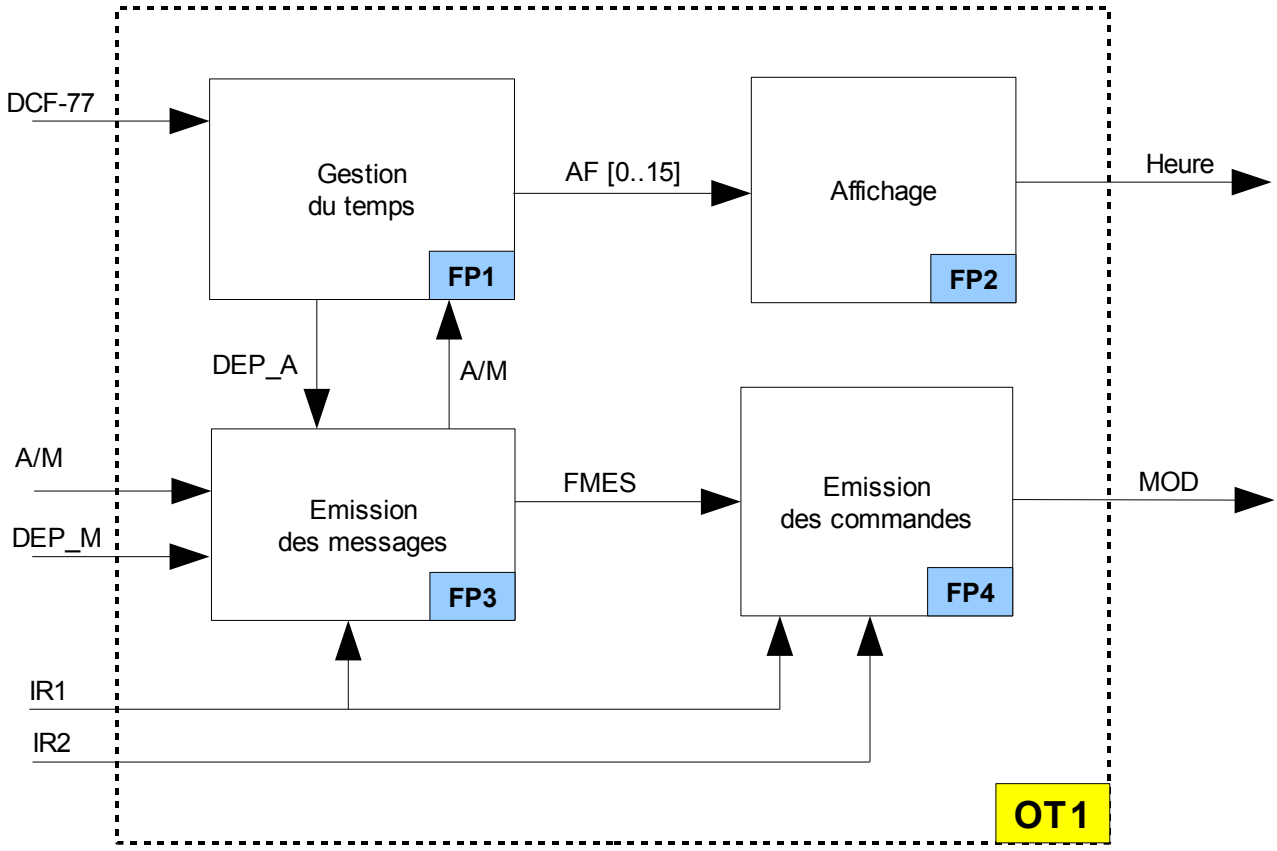
- De donner l'heure
- De disposer d'un mode manuel ou automatique :
  - Mode manuel
    Départ du train de la gare à l'appui sur un poussoir.
  - Mode automatique
    Départ du train de la gare toutes les minutes.

1-2 Fonction d'usage

Afficher l'heure légale et prévenir de l'arrivée imminente d'un train et du départ de celui-ci.

2 Étude fonctionnelle

2-1 Schéma fonctionnel de degré 1



2-2 Définition des fonctions principales

FP1 (Gestion du temps)

- Elle acquiert l'heure atomique absolue.
- Elle gère l'heure.
- Elle commande en automatique les départs du train (toutes les minutes).

FP2 (Affichage)

- Elle affiche l'heure légale.

FP3 (Émission des messages)

- Elle émet le message d'arrivée du train en gare.
- Elle émet le message du départ du train de la gare.
- Elle commande en manuel les départs du train.

FP4 (Émission des commandes)

- Elle émet les différents ordres, pour pouvoir les transmettre à la locomotive.
  - Départ de la locomotive en vitesse rapide.
  - Ralentissement de la locomotive.
  - Arrêt de la locomotive.

2-3 Étude fonctionnelle de degré 2

2-3-1 Étude fonctionnelle de FP1

rôle : Gérer l'heure légale et les départs automatiques du train.

entrée(s) :
DCF-77 : Information horaire codée (voir annexe).
A/M : Information binaire donnant le mode de départ du train
A/M = 1 : Départ automatique toutes les minutes.
A/M = 0 : Départ manuel, à l'appui sur DEP_M.
sortie(s) :
AF [0..15] : Heure légale codée en BCD.
DEP_A : Information binaire ordonnant l'émission du message vocal du départ imminent du train (actif à l'état bas).

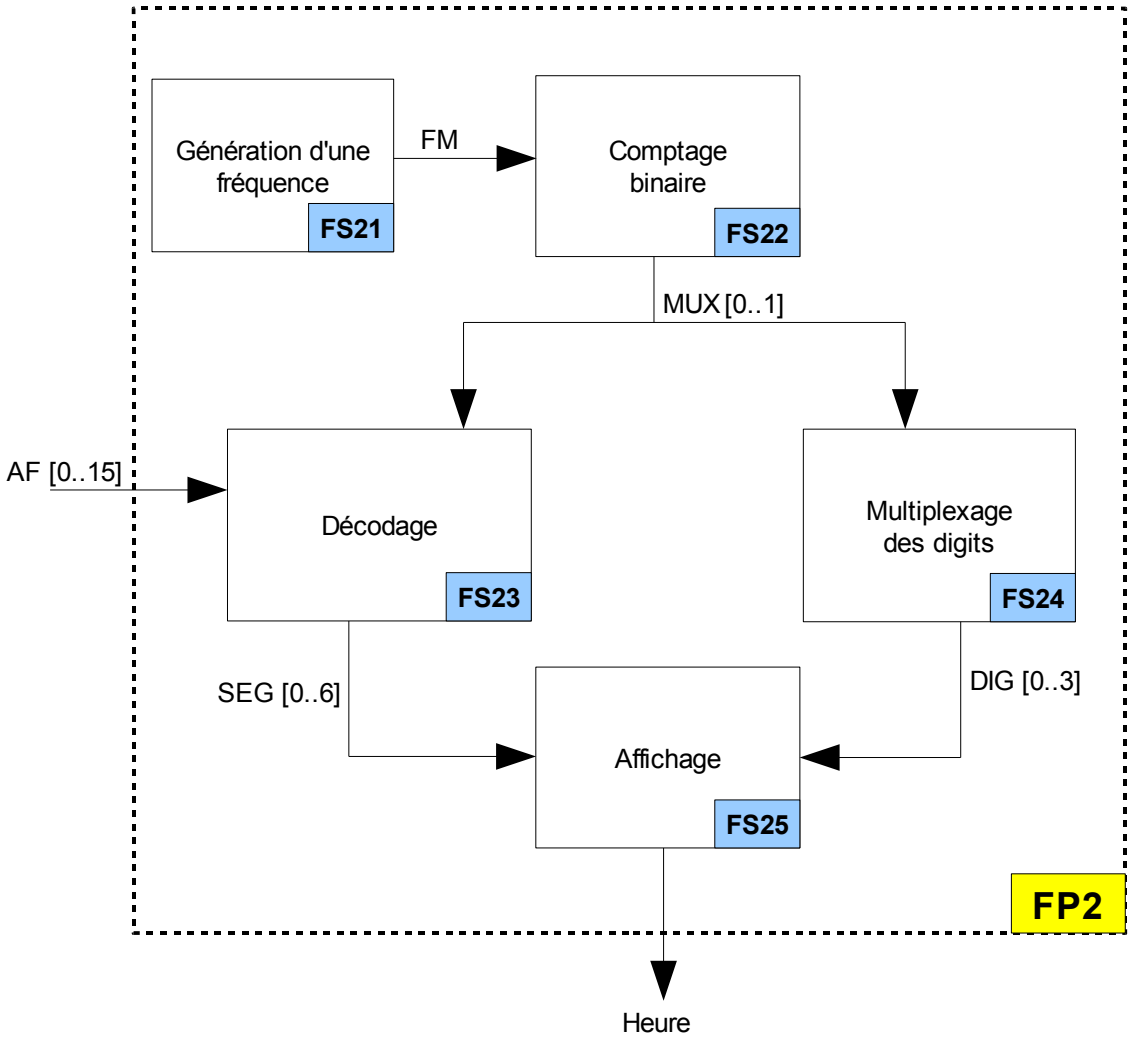
Pas d'étude fonctionnelle de degré 2 pour la fonction FP1, utilisation de la carte ATMEL.

2-3-2 Étude fonctionnelle de FP2

rôle : Afficher l'heure légale.

entrée(s) :
AF [0..15] : Heure légale codée en BCD.
sortie(s) :
Heure : Visualisation de l'heure légale

Schéma fonctionnel



Etude de FS21

rôle : Générer une fréquence variable

entrée(s) :
Aucune
sortie(s) :
FM : Signal périodique de fréquence variable.

Etude de FS22

rôle : Générer les signaux de commande de multiplexage.

entrée(s) :
FM : Signal périodique de fréquence variable.
sortie(s) :
MUX [0..1] : Signaux de comptage sur 2 bits.

Etude de FS23

rôle : Sélectionner et décoder un digit parmi 4.

entrée(s) :
MUX [0..1] : Signaux de comptage sur 2 bits.
AF [0..15] : Heure légale codée en BCD.
sortie(s) :
SEG [0..6] : Valeur du digit sélectionné et décodé pour un affichage 7 segments.

Etude de FS24

rôle : Sélectionner un afficheur parmi 4.

entrée(s) :
MUX [0..1] : Signaux de comptage sur 2 bits.
sortie(s) :
DIG [0..3] : Signaux de validation des afficheurs.
(actif par un niveau bas).

Etude de FS25

rôle : Visualiser l'heure légale.

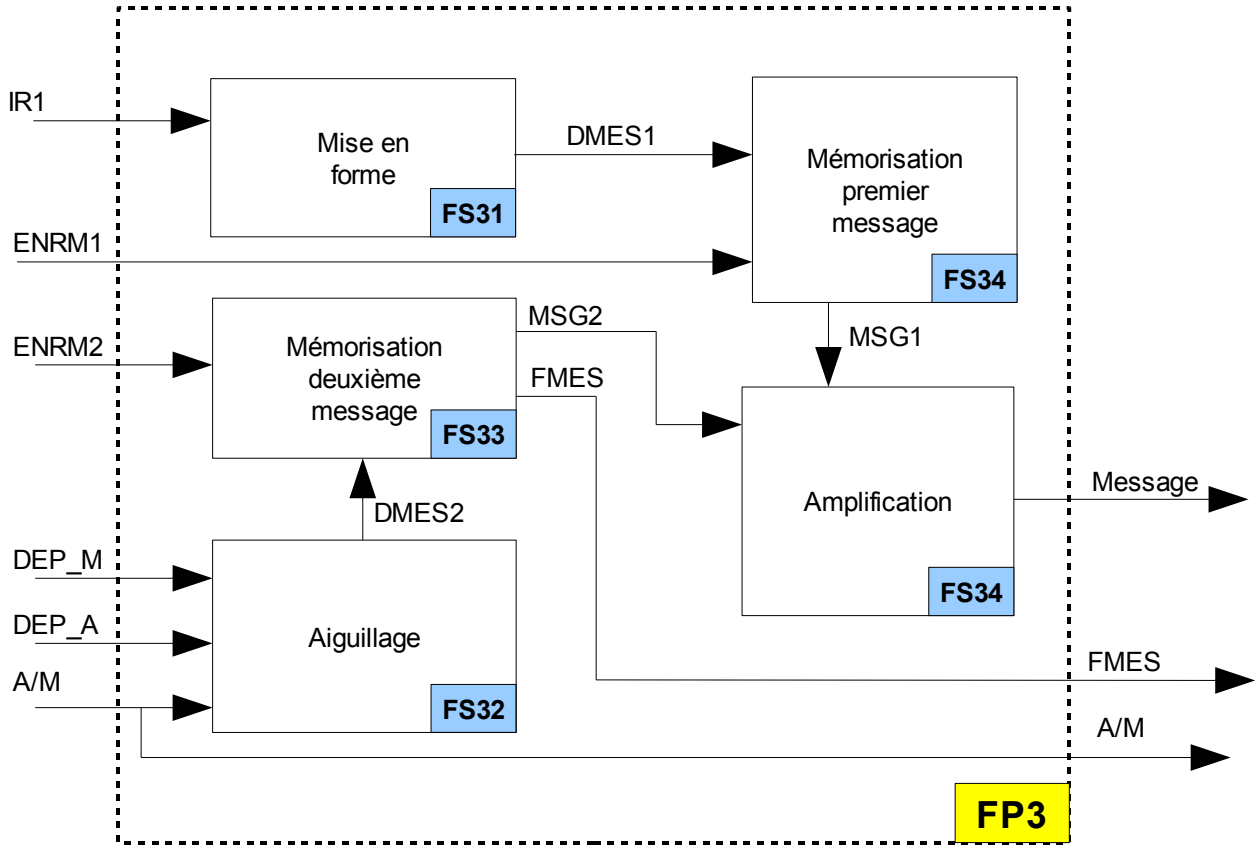
entrée(s) :
SEG [0..6] : Valeur du digit sélectionné et décodé pour un affichage 7 segments.
DIG [0..3] : Signaux de validation des afficheurs.
(actif par un niveau bas).
sortie(s) :
Heure : Visualisation de l'heure légale

2-3-3 Étude fonctionnelle de FP3

rôle : Emettre deux messages vocaux (arrivée et départ imminent du train), et donner l'ordre de départ du train.

entrée(s) :
A/M : Information binaire donnant le mode de départ du train
A/M = 1 : Départ automatique toutes les minutes.
A/M = 0 : Départ manuel, à l'appui sur DEP_M.
DEP_A : Information binaire ordonnant l'émission du message vocal du départ imminent du train
(actif à l'état bas).
DEP_M : Information binaire ordonnant l'émission du message vocal du départ imminent du train
(actif à l'état bas).
sortie(s) :
FMES : Signal binaire indiquant la fin du message vocal, et que le train peut partir.
(actif à l'état bas).
A/M : Information binaire donnant le mode de départ du train
A/M = 1 : Départ automatique toutes les minutes.
A/M = 0 : Départ manuel, à l'appui sur DEP_M.

Schéma fonctionnel



Étude de FS31

rôle : Générer une impulsion calibrée.

entrée(s) :
IR1 : Signal binaire informant que le train va arriver en gare.
(actif à l'état bas).
sortie(s) :
DMES1 : Signal binaire autorisant l'émission d'un message vocal.
(actif à l'état bas).

Étude de FS32

rôle : Générer l'émission du message soit en fonctionnement manuel, soit en fonctionnement automatique.

entrée(s) :
A/M : Information binaire donnant le mode de départ du train
A/M = 1 : Départ automatique toutes les minutes.
A/M = 0 : Départ manuel, à l'appui sur DEP_A.
DEP_A : Information binaire ordonnant l'émission du message vocal du départ imminent du train
(actif à l'état bas).
DEP_M : Information binaire ordonnant l'émission du message vocal du départ imminent du train
(actif à l'état bas).
sortie(s) :
DMES2 : Signal binaire autorisant l'émission d'un message vocal.
(actif à l'état bas).

Étude de FS33

rôle : Mémoriser et émettre un premier message vocal.

entrée(s) :
- DMES2 : Signal binaire autorisant l'émission d'un message vocal. (actif à l'état bas).
- ENMR2 : Signal binaire actif à l'état bas pendant l'enregistrement du premier message vocal.

sortie(s) :
- MSG2 : Signal analogique image du premier message vocal.

Étude de FS34

rôle : Mémoriser et émettre un deuxième message vocal.

entrée(s) :
- DMES1 : Signal binaire autorisant l'émission d'un message vocal. (actif à l'état bas).
- ENMR1 : Signal binaire actif à l'état bas pendant l'enregistrement du premier message vocal.

sortie(s) :
- MSG1 : Signal analogique image du premier message vocal.

Étude de FS34

rôle : Amplifier et restituer un message vocal.

entrée(s) :
- MSG1 : Signal analogique image du premier message vocal.
- MSG2 : Signal analogique image du deuxième message vocal.

sortie(s) :
- Message : Écoute du message émis.

2-3-4 Étude fonctionnelle de FP4

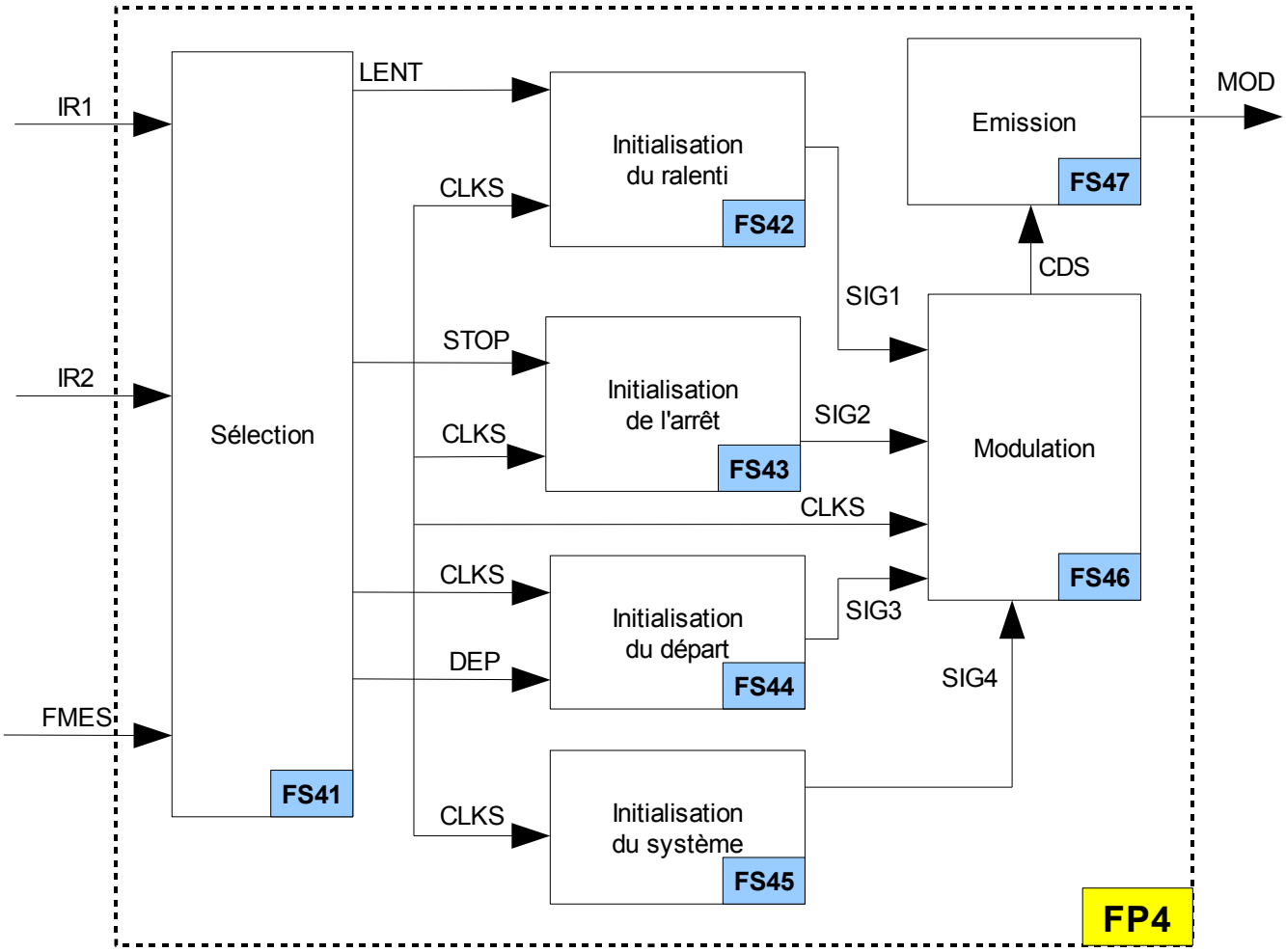
rôle : Sélectionner et émettre une des quatre commandes suivantes :

Émettre une fréquence de 3000Hz à l'initialisation du système.
Émettre une fréquence de 500Hz pour faire ralentir le train.
Émettre une fréquence de 1000Hz pour faire arrêter le train.
Émettre une fréquence de 1500Hz pour faire partir le train.

entrée(s) :
- FMES : Signal binaire indiquant la fin du message vocal, et que le train peut partir. (actif à l'état bas).
- IR1 : Signal binaire informant que le train va arriver en gare. (actif à l'état bas).
- IR2 : Signal binaire informant que le train arrive en gare. (actif à l'état bas).

sortie(s) :
- MOD : Signal HF codé.

Schéma fonctionnel



Étude de FS41
rôle : Générer un signal d'horloge actif au front montant
entrée(s) :

FMES	: Signal binaire indiquant la fin du message vocal, et que le train peut partir. (actif à l'état bas).
IR1	: Signal binaire informant que le train va arriver en gare. (actif à l'état bas).
IR2	: Signal binaire informant que le train arrive en gare. (actif à l'état bas).

sortie(s) :

CLKS	: Signal d'horloge actif sur front montant.
DEP	: Signal binaire autorisant le départ du train. (actif à l'état haut).
LENT	: Signal binaire informant que le train va arriver en gare. (actif à l'état haut).
STOP	: Signal binaire informant que le train arrive en gare. (actif à l'état haut).

Étude de FS42
rôle : Sélectionner la commande : Faire ralentir le train.
entrée(s) :
LENT : Signal binaire informant que le train va arriver en gare. (actif à l'état haut).
CLKS : Signal d'horloge actif sur front montant.
sortie(s) :
SIG1 : Signal binaire validant la première commande. (actif à l'état haut).

Étude de FS43
rôle : Sélectionner la commande : Faire arrêter le train.
entrée(s) :
STOP : Signal binaire informant que le train arrive en gare. (actif à l'état haut).
CLKS : Signal d'horloge actif sur front montant.
sortie(s) :
SIG2 : Signal binaire validant la deuxième commande. (actif à l'état haut).

Étude de FS44
rôle : Sélectionner la commande : Faire partir le train.
entrée(s) :
DEP : Signal binaire autorisant le départ du train. (actif à l'état haut).
CLKS : Signal d'horloge actif sur front montant.
sortie(s) :
SIG3 : Signal binaire validant la troisième commande. (actif à l'état haut).

Étude de FS45
rôle : Initialiser le système.
entrée(s) :
CLKS : Signal d'horloge actif sur front montant.
sortie(s) :
SIG4 : Signal binaire validant la quatrième commande. (actif à l'état haut).

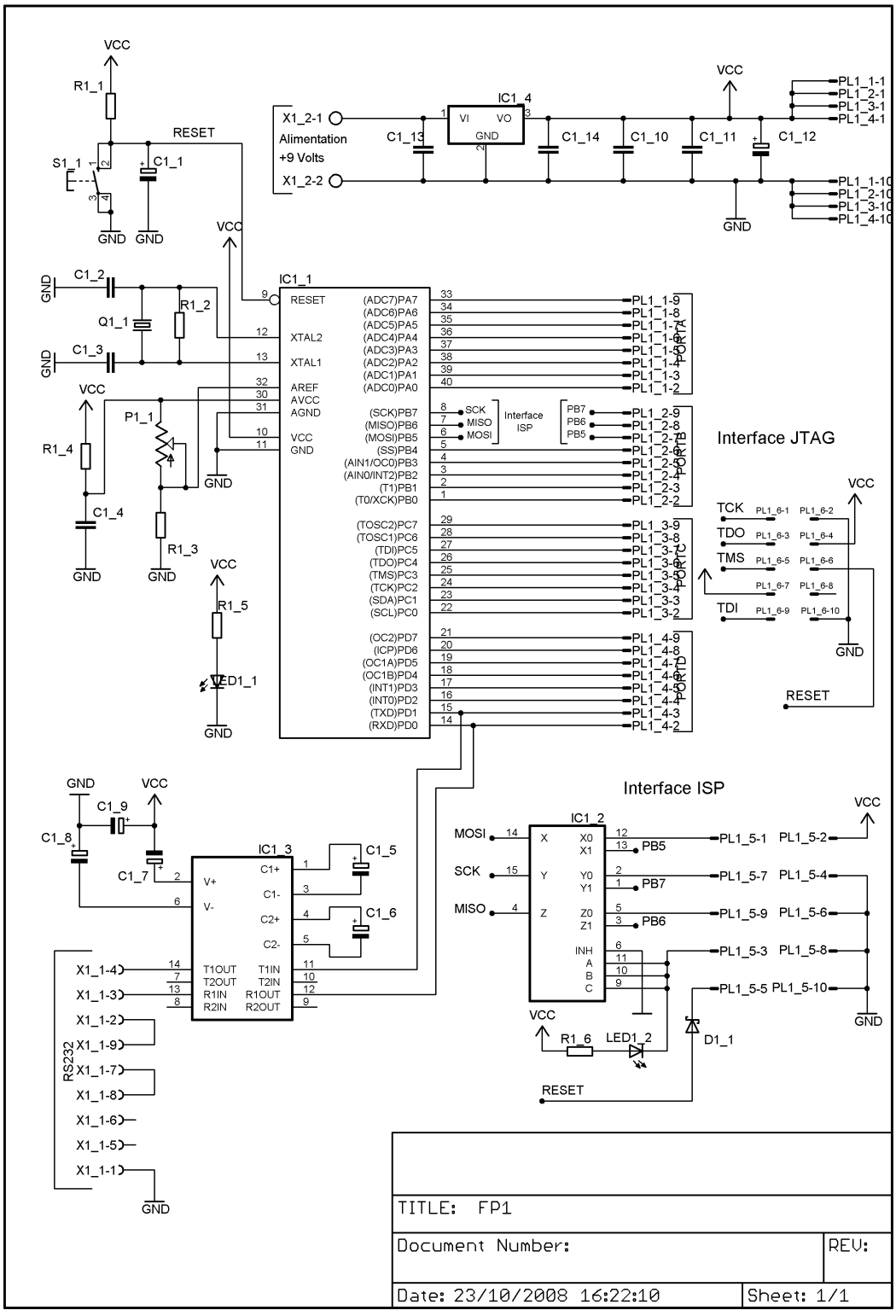
Étude de FS46
rôle : Préparer le signal de commande à émettre.
entrée(s) :
SIG1 : Signal binaire validant la première commande. (actif à l'état haut).
SIG2 : Signal binaire validant la deuxième commande. (actif à l'état haut).
SIG3 : Signal binaire validant la troisième commande. (actif à l'état haut).
SIG4 : Signal binaire validant la quatrième commande. (actif à l'état haut).
sortie(s) :
CDS : Fréquence à émettre.

Étude de FS47
rôle : Émettre la commande.
entrée(s) :
CDS : Fréquence à émettre.
sortie(s) :
MOD : Signal HF.

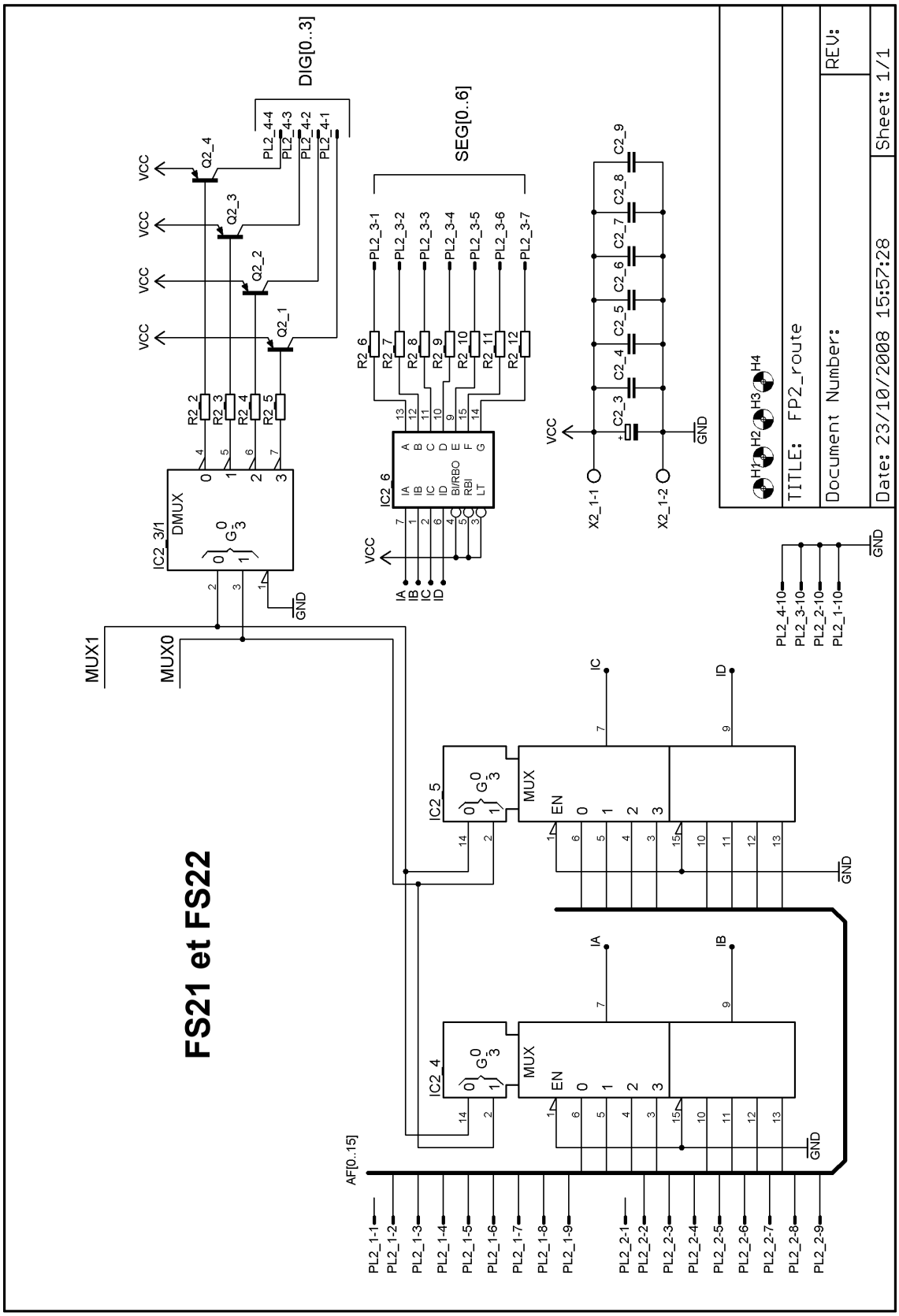
3 Étude structurelle

3-1 Schémas structurels

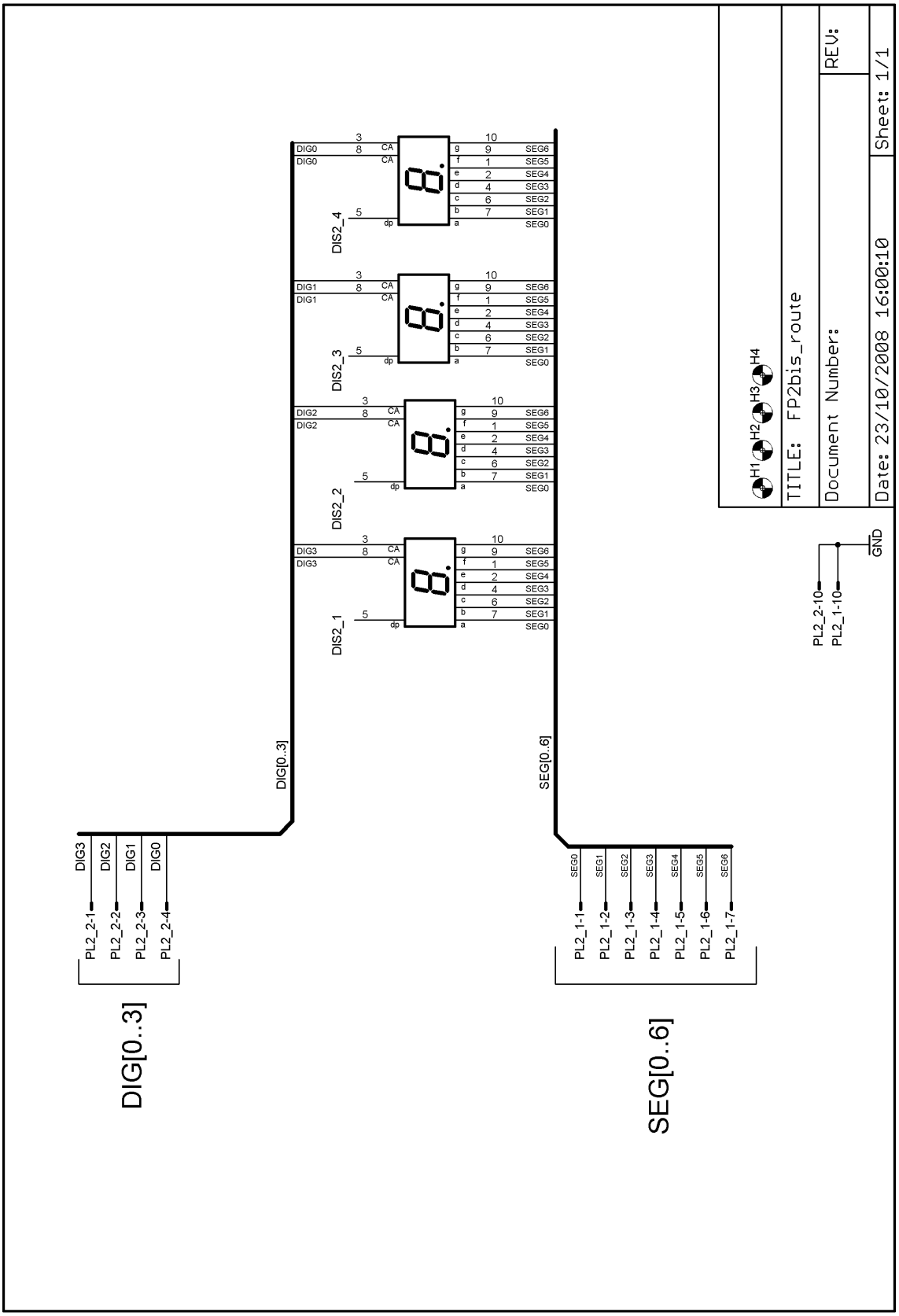
Structure de FP1



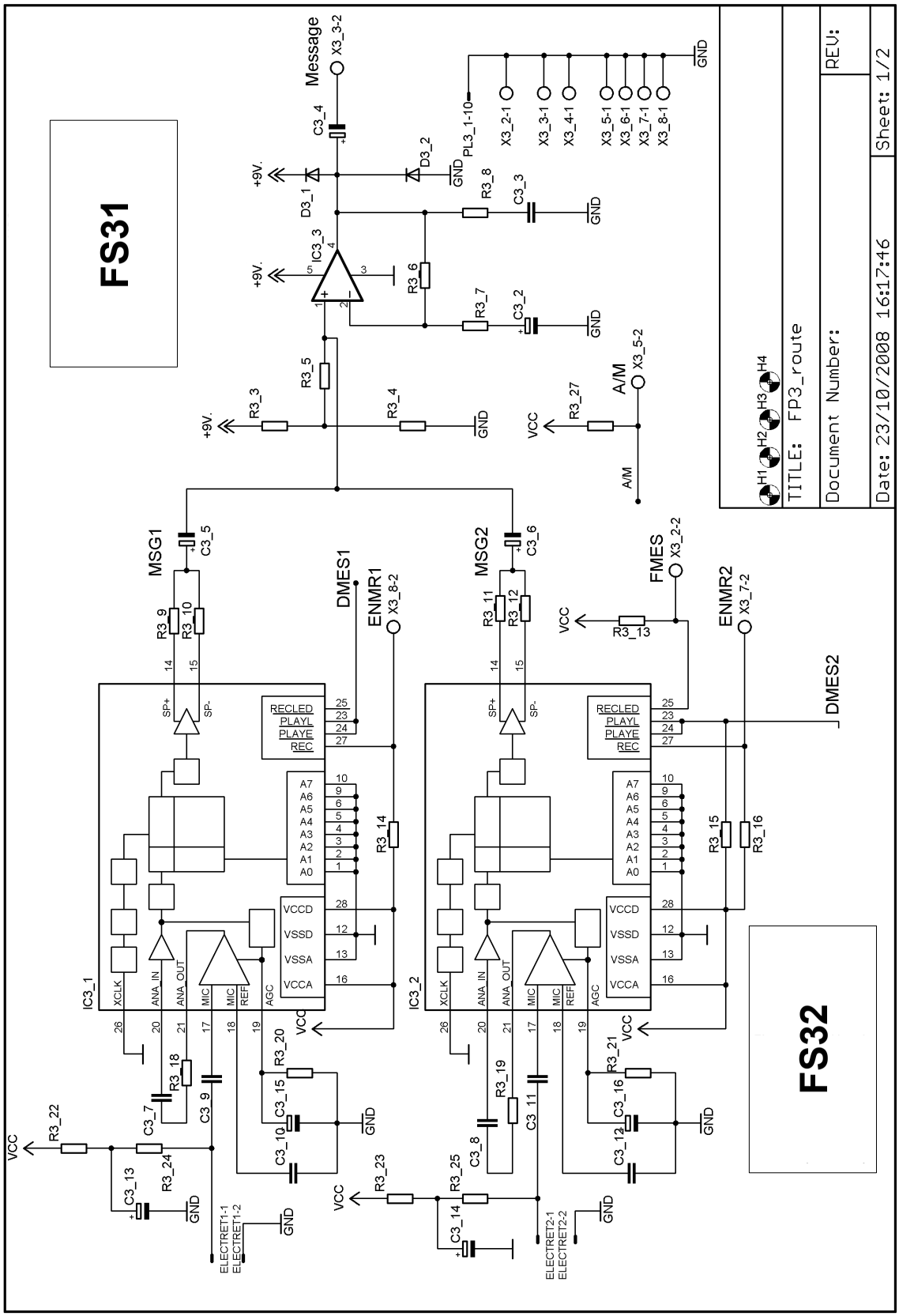
Structure de FP2



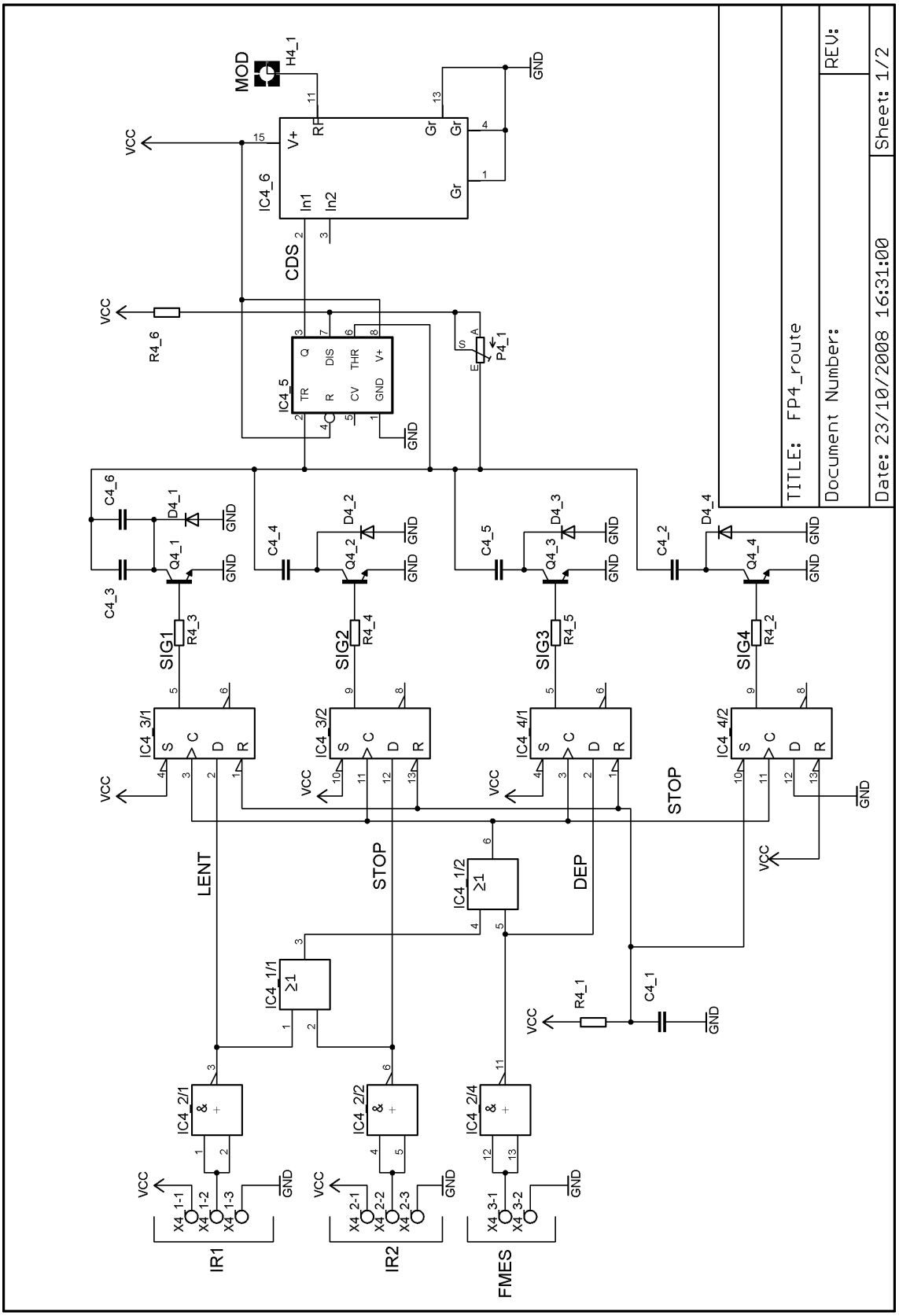
Structure de FP2bis



Structure de FP3



Structure de FP4



3-2 Nomenclature

Réf.	Désignation	Valeur	Qte	Réf.	Désignation	Valeur	Qte
IC1_1	Microcontroleur	ATMEGA32	1	IC3_1 et IC3_2	Mémoire	ISD1400	2
IC1_2	Monostable	4053	1	IC3_3	Amplificateur	TDA2040	1
IC1_3	Driver	MAX232	1	R3_3 à R3_5	Résistance	100K	3
IC1_4	Régulateur	7805	1	R3_6	Résistance	150K	1
R1_1	Résistance	10K	1	R3_7	Résistance	4,7K	1
R1_2	Résistance	1,5M	1	R3_8	Résistance	1	1
R1_3	Résistance	68K	1	R3_9	Résistance	5,6	1
R1_4	Résistance	100	1	R3_10	Résistance	10	1
R1_5 et R1_6	Résistance	180	2	R3_11	Résistance	5,6	1
P1_1	Trimmer 64W	100K	1	R3_12	Résistance	10	1
C1_1	Condensateur	22uF	1	R3_13	Résistance	33K	1
C1_2 et C1_3	Condensateur	22pF	2	R3_14 à R3_16	Résistance	100K	3
C1_4	Condensateur	47nF	1	R3_18 et R3_19	Résistance	0	2
C1_5 à C1_9	Condensateur	1uF	5	R3_20 et R3_21	Résistance	470K	2
C1_10 à C1_11	Condensateur	100nF	2	R3_22 et R3_23	Résistance	220	2
C1_12	Condensateur	100uF	1	R3_24 et R3_25	Résistance	2,2K	2
C1_13	Condensateur	470nF	1	R3_27	Résistance	10K	1
C1_14	Condensateur	330nF	1				
D1_1	Diode	BAT42	1	C3_2	Condensateur	2u	1
LED1_1 et LED1_2	Led 5mm		2	C3_3	Condensateur	220n	1
S1_1	Poussoir	DT6	1	C3_4	Condensateur	2200uF	1
PL1_1 à PL1_6	Connecteur	HE10	6	C3_5 etC3_6	Condensateur	22uF	2
X1_1	Connecteur	SUBD9	1	C3_7 et C3_8	Condensateur	1uF	2
X1_2	Bornier	2 plots	1	C3_9 àC3_12	Condensateur	470n	4
				C3_13 et C3_14	Condensateur	2.2u	2
				C3_15 et C3_16	Condensateur	4.7u	2
			1	C3_17 et C3_18	Condensateur	100u	2
			1	C3_19 à C3_24	Condensateur	100n	6
IC2_3		74139	1	D3_1 et D3_2	Diode	1N4148	2
IC2_4 et IC2_5		74153	2	PL3_1	Connecteur	HE10	1
IC2_6	Décodeur	74LS47	1	X3_1	Bornier	3 plots	1
				X3_2 à X3_8	Bornier	2 plots	7
R2_2 à R2_5	Résistance		4				
R1_6 à R2_12	Résistance		7				
C2_2	Condensateur	10nF	1				
C2_3	Condensateur	220uF	1				
C2_4 à C2_9	Condensateur	100nF	6				
Q2_1 à Q2_4	Transistor	BC327	4				
PL2_1 à PL2_6	Connecteur	HE10	6				
X2_1	Bornier	2 plots	1				
DIS2_1 à DIS2_4	Afficheur						

Réf.	Désignation	Valeur	Qte	Réf.	Désignation	Valeur	Qte
IC4_1	Portes logiques	7432	1	C4_1	Condensateur	1uF	1
IC4_2	Portes logiques	7400	1	C4_2	Condensateur		
IC4_3 et IC4_4	Bascules	7474	2	C4_3	Condensateur		
IC4_5	Astable	NE555	1	C4_4	Condensateur		
IC4_6	Module AUREL	TX-SAW	1	C4_5	Condensateur		
				C4_6	Condensateur		
R4_1	Résistance	22K	1	C4_7 à C4_10	Condensateur	100nF	4
R4_2	Résistance			C4_11	Condensateur	220uF	1
R4_3	Résistance			X4_1 à X4_2	Bornier	3 plots	2
R4_4	Résistance						
R4_5	Résistance						
R4_6	Résistance						
P4_1	Trimmer 64W			X4_3 à X4_4	Bornier	2 plots	2
				H4_1	Antenne		1
Q4_1 à Q4_4	Transistor	2N2222A	4				
D4_1 à D4_4	Diode	1N4148	4				

OT2 Centrale de commande

1 Mise en situation du système technique

1-1 Introduction

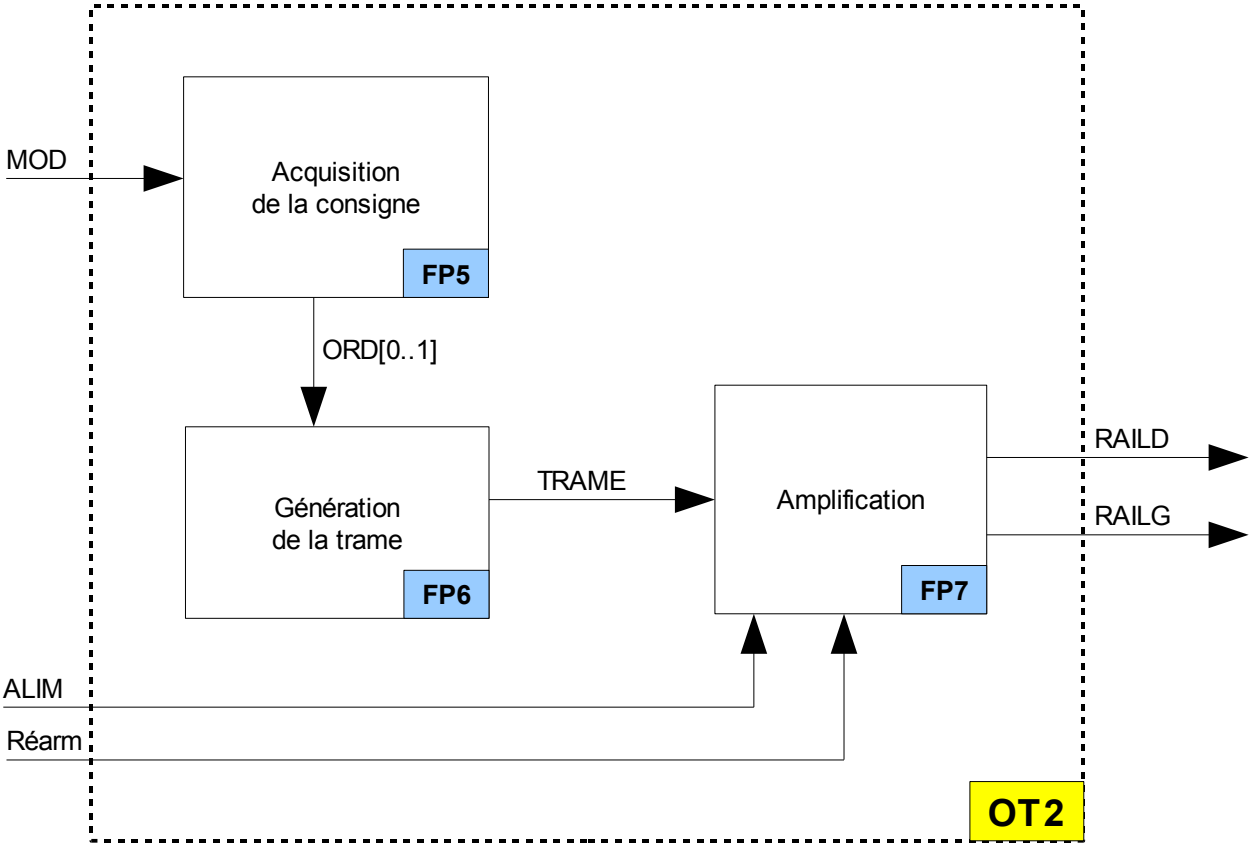
La centrale de commande réalise l'envoi de la trame au format NMEA, afin de pouvoir piloter une ou plusieurs locomotives.

1-2 Fonction d'usage

Commande la vitesse du train

2 Étude fonctionnelle

2-1 Schéma fonctionnel de degré 1



2-2 Définition des fonctions principales

FP5 (Acquisition de la consigne)

- Elle reçoit et met en forme la consigne venant de la gare.

FP6 (Génération de la trame)

- Elle génère la trame au protocole DCC NMRA en fonction des consignes reçues.

FP7 (Amplification)

- Elle amplifie la trame au protocole DCC NMRA avant de la transmettre sur les rails.
- Elle surveille les court-circuits sur les rails.

2-3 Étude fonctionnelle de degré 2

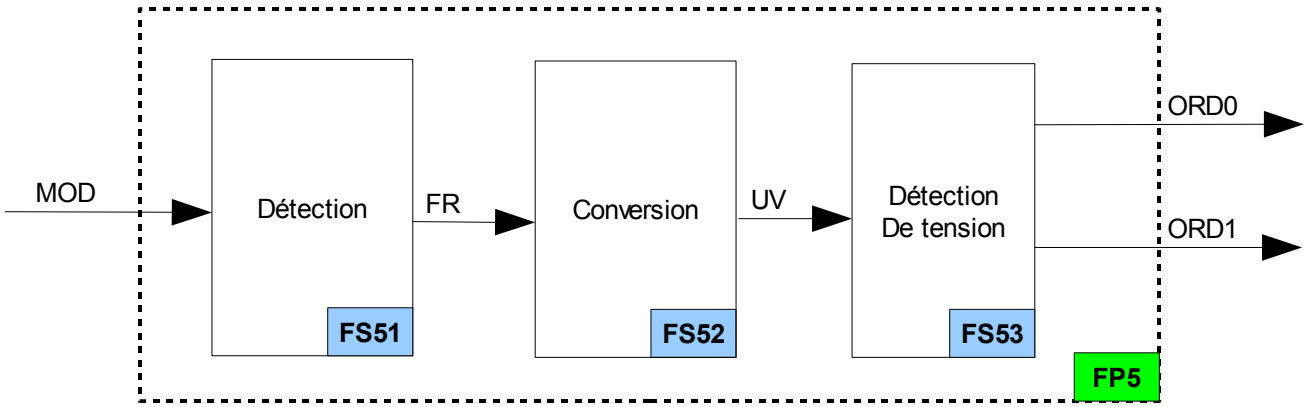
2-3-1 Étude fonctionnelle de FP5

rôle : Recevoir et décoder les ordres transmis par la « gare ».

entrée(s) :
MOD : Signal HF codé.
sortie(s) :
ORD[0..1] : Mot de 2 bits donnant le type d'ordre reçu

ORD1	ORD0	Ordre
0	0	Faire arrêter le train
0	1	Faire ralentir le train
1	0	Non utilisé
1	1	Faire partir le train

Schéma fonctionnel



Étude de FS51

rôle : Démoduler l'ordre reçu de la gare.

entrée(s) :
MOD : Signal HF codé.
sortie(s) :
FR : Fréquence image de la fonction à réaliser.

Étude de FS52

rôle : Convertir une fréquence en une tension.

entrée(s) :
FR : Fréquence image de la fonction à réaliser.
sortie(s) :
UV : Tension image de la fonction à réaliser.

Étude de FS53

rôle : Mémoriser l'ordre reçu

entrée(s) :
UV : Tension image de la fonction à réaliser.
sortie(s) :
ORD[0..1] : Mot de 2 bits donnant le type d'ordre reçu
(voir tableau précédent)

2-3-2 Étude fonctionnelle de FP6

rôle : Générer la trame DCC NMRA

entrée(s) :
ORD[0..1] : Mot de 2 bits donnant le type d'ordre reçu
(voir tableau précédent)
sortie(s) :
TRAME : Information au format DCC NMRA dédié aux locomotives ou aux accessoires.

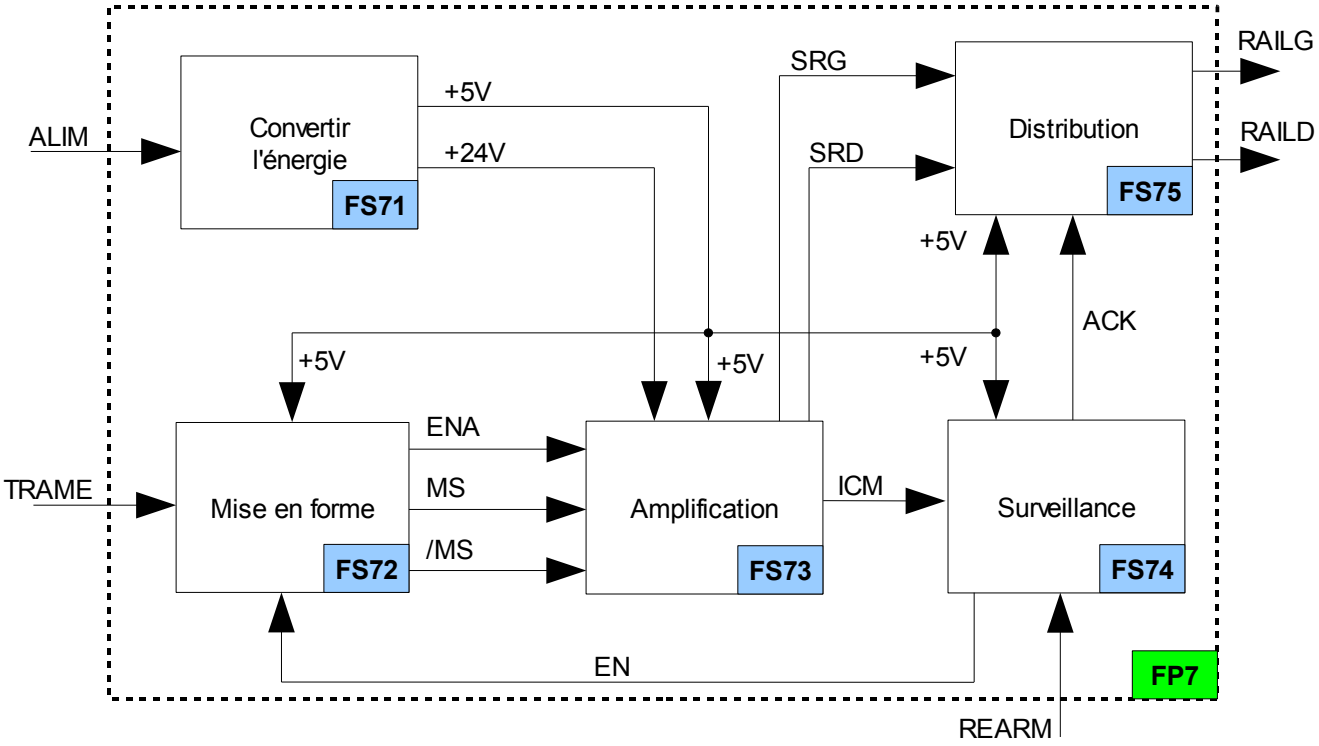
Pas d'étude fonctionnelle de degré 2 pour la fonction FP6, utilisation de la carte ATMEL.

2-3-1 Étude fonctionnelle de FP7

Rôle : Amplifier l'information dédiée aux locomotives.

entrée(s) :
ALIM : Tension alternative sinusoïdale 16V eff, ou 24V continue.
TRAME : Information au format DCC NMRA dédiée aux locomotives ou aux accessoires.
Réarm : Information manuelle de réarmement après un incident sur les voies.
sortie(s) :
RAILG : Trame série compatible NMEA d'amplitude ±20V.
RAILD : Trame série compatible NMEA d'amplitude ±20V, en opposition avec RAILG.

Schéma fonctionnel



Etude de FS71

rôle : Convertir une tension alternative sinusoïdale de valeur efficace de 16V, en plusieurs tensions continues positives.

entrée(s) :
- ALIM : Tension alternative sinusoïdale 16V eff, ou 24V continue.

sortie(s) :
- +24V : Alimentation positive 24V.
- +5V : Alimentation positive 5V.

Etude de FS72

rôle : Mettre en forme la trame TTL au format DCC NMRA et autoriser son amplification.

entrée(s) :
- TRAME : Information au format DCC NMRA dédié aux locomotives ou aux accessoires.
- EN : Niveau logique actif à l'état 0 bloquant l'amplification de la trame suite à un court circuit sur les rails.

sortie(s) :
- ENA : Niveau logique actif à l'état 1 autorisant l'amplification de la trame.
- MS : Trame série à envoyer sur les rails.
- /MS : Trame série complémentée à envoyer sur les rails.

Etude de FS73

rôle : Amplifier la trame à envoyer sur les rails.

entrée(s) :
- ENA : Niveau logique actif à l'état 1 autorisant l'amplification de la trame.
- MS : Trame série à envoyer sur les rails.
- /MS : Trame série complémentée à envoyer sur les rails.

sortie(s) :
- ICM : Information analogique représentant le courant dans les rails.
- SRG : Trame série compatible NMEA d'amplitude ±20V.
- SRD : Trame série compatible NMEA d'amplitude ±20V, en opposition avec RAILG.

Etude de FS74

rôle : Vérifier l'absence de court-circuit sur les rails.

entrée(s) :
- ICM : Information analogique représentant le courant dans les rails.
- Réarm : Information manuelle permettant de nouveau l'envoi de la trame sur les rails après un court circuit.

sortie(s) :
- EN : Niveau logique actif à l'état 0 bloquant l'amplification de la trame suite à un court circuit sur les rails.
- ACK : Information logique actif à l'état logique "0" autorisant l'envoi de la trame amplifiée sur les rails.

Etude de FS75

rôle : Distribuer l'énergie et les informations destinées aux décodeurs.

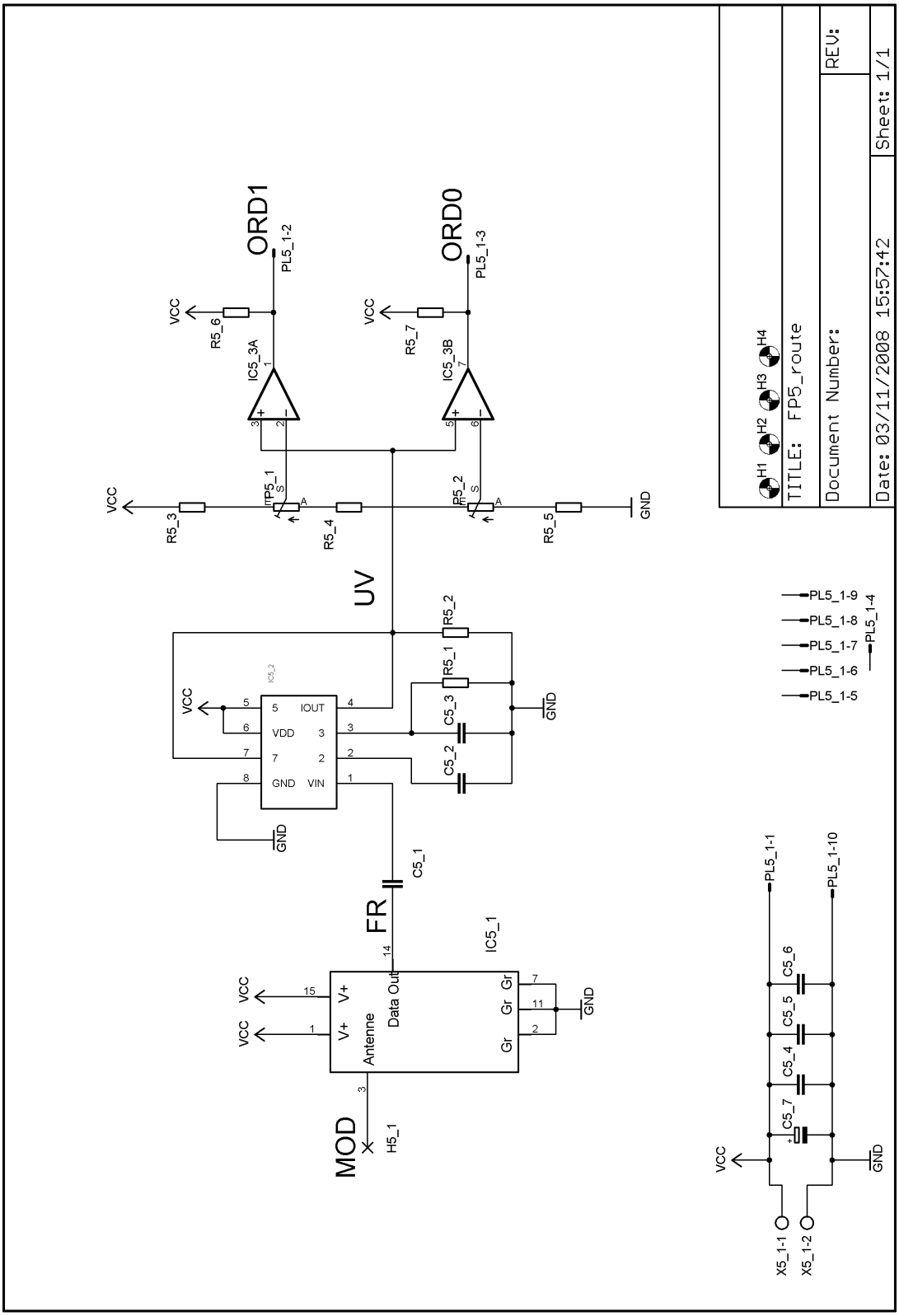
entrée(s) :
- ACK : Information logique « actif à l'état logique 0 » autorisant l'envoi de la trame amplifiée sur les rails.
- SRG : Trame série compatible NMEA d'amplitude ±20V.
- SRD : Trame série compatible NMEA d'amplitude ±20V, en opposition avec RAILG.

sortie(s) :
- RAILG : Trame série compatible NMEA d'amplitude ±20V.
- RAILD : Trame série compatible NMEA d'amplitude ±20V, en opposition avec RAILG.

3.Étude structurelle

3-1 Schémas structurels

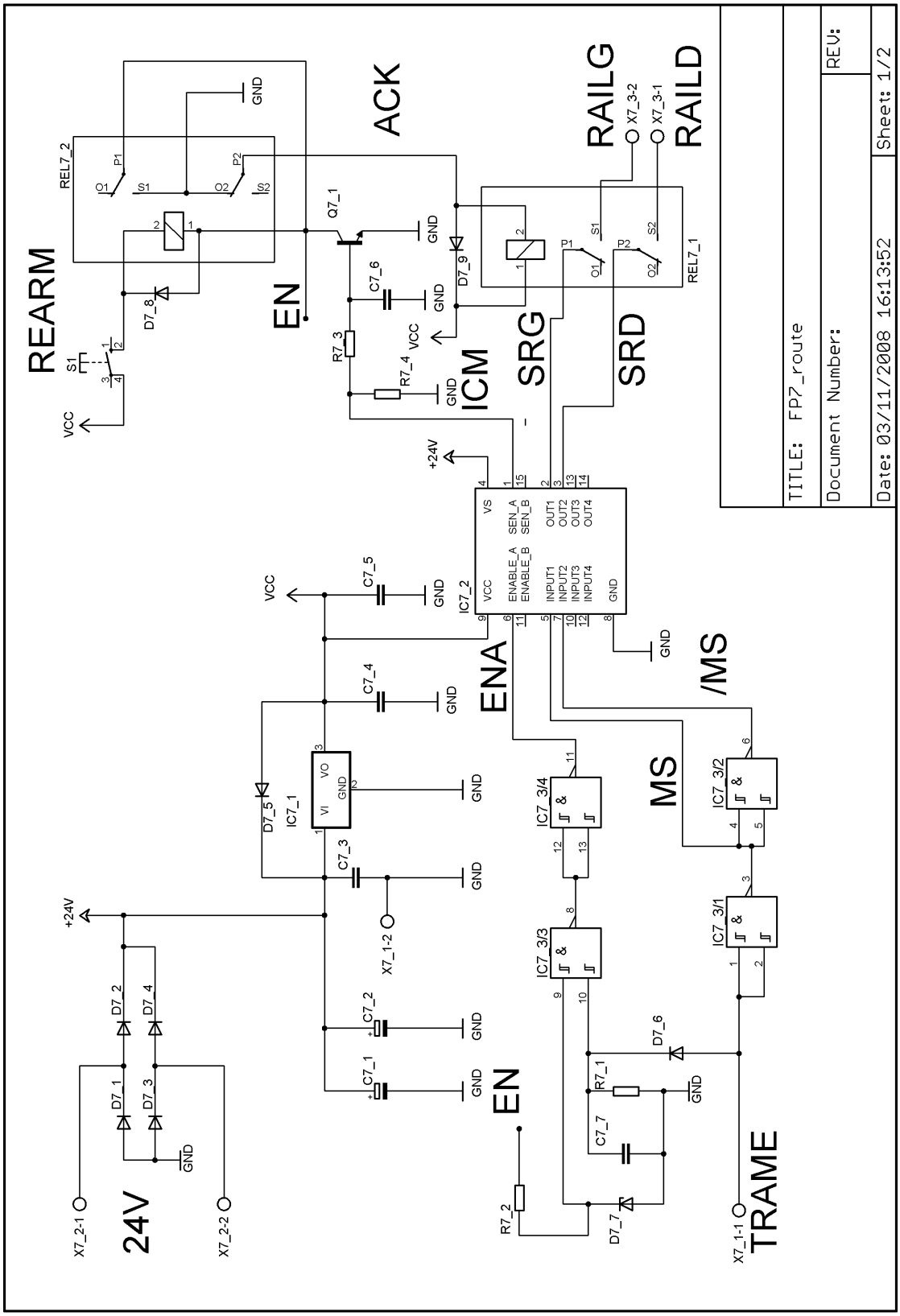
Structure de FP5



Structure de FP6

Pour la fonction FP6, on utilise une carte ATMEGA, voir fonction FP1.

Structure de FP7



3-2 Nomenclature

Réf.	Désignation	Valeur	Qte	Réf.	Désignation	Valeur	Qte
IC5_1	Module AUREL	BC-NBK	1	IC7_1	Régulateur	7805	1
IC5_2	Convertisseur	LM2917	1	IC7_2	Amplificateur	L298	1
IC5_3	AOP	LM393	1	IC7_3	Portes Logiques	74132	1
R5_1	Résistance			R7_1	Résistance		
R5_2	Résistance	10K	1	R7_2	Résistance	10K	1
R5_3	Résistance	56K	1	R7_3	Résistance	27K	1
R5_4	Résistance	6,8K	1	R7_4	Résistance	1	1
R5_5	Résistance	5,6K	1	C7_1 et C7_2	Condensateur	220u	2
R5_6 et R5_7	Résistance	10K	2	C7_3 à C7_5	Condensateur	100nF	3
P5_1	Potentiomètre			C7_6	Condensateur	1nF	1
P5_2	Potentiomètre			C7_7	Condensateur		
C5_1	Condensateur	100nF	1	D7_1 à D7_6	Diode	1N4004	6
C5_2	Condensateur			D7_7	Diode Zener	BZX85 5v	1
C5_3	Condensateur	220uF	1	D7_8 et D7_9	Diode	BYV27	2
C5_4 à C5_6	Condensateur	100nF	3	Q7_1	Transistor	BC548	1
C5_7	Condensateur	100uF	1	REL7_1 et REL7_2	Relais	G2R2	2
PL5_1	Connecteur	HE10	1	X7_1 à X7_3	Bornier	2 plots	3
H5_1	Antenne		1	S1	Interrupteur		
X5_1	Bornier	2 plots	1				
PL5_1	Connecteur	HE10	1				

OT3 Circuit ferroviaire

1 Mise en situation du système technique

1-1 Introduction

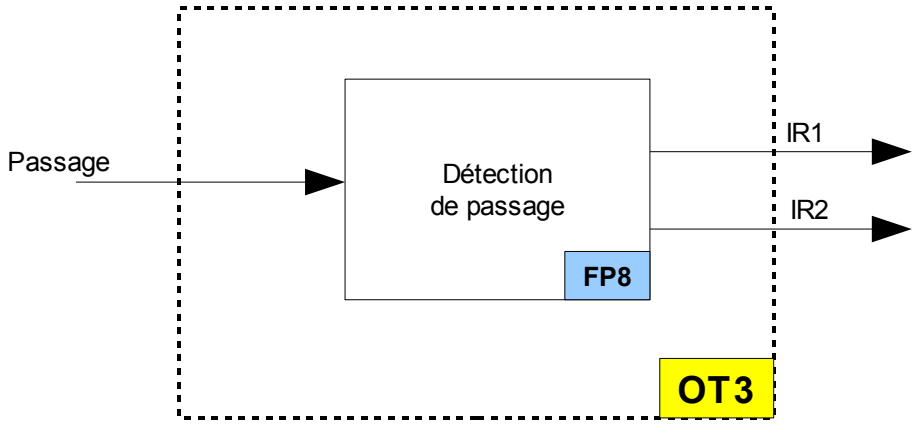
Le circuit ferroviaire est constitué de rails et de capteurs infra-rouge qui permettent la détection du passage du train.

1-2 Fonction d'usage

Transporter les commandes et l'énergie nécessaires au fonctionnement du train.

2 Étude fonctionnelle

2-1 Schéma fonctionnel de degré 1



2-2 Définition des fonctions principales

FP8 (Détection de passage)

- Elle transmet à la gare les signaux tout ou rien qui informent du passage du train.

2-3 Étude fonctionnelle de degré 2

2-3-1 Étude fonctionnelle de FP8

rôle : Détecter le passage du train à 2 endroits du circuit, légèrement avant l'arrivée en gare, et à l'arrivée en gare.

entrée(s) :
Passage : Passage du train devant les barrières infra-rouge.
sortie(s) :
IR1 : Signal binaire informant que le train va arriver en gare.
(actif à l'état bas).
IR2 : Signal binaire informant que le train arrive en gare.
(actif à l'état bas).

Pas d'étude fonctionnelle de degré 2 pour la fonction FP8, utilisation de module infra rouge.

OT4 Locomotive fictive

1 Mise en situation du système technique

1-1 Introduction

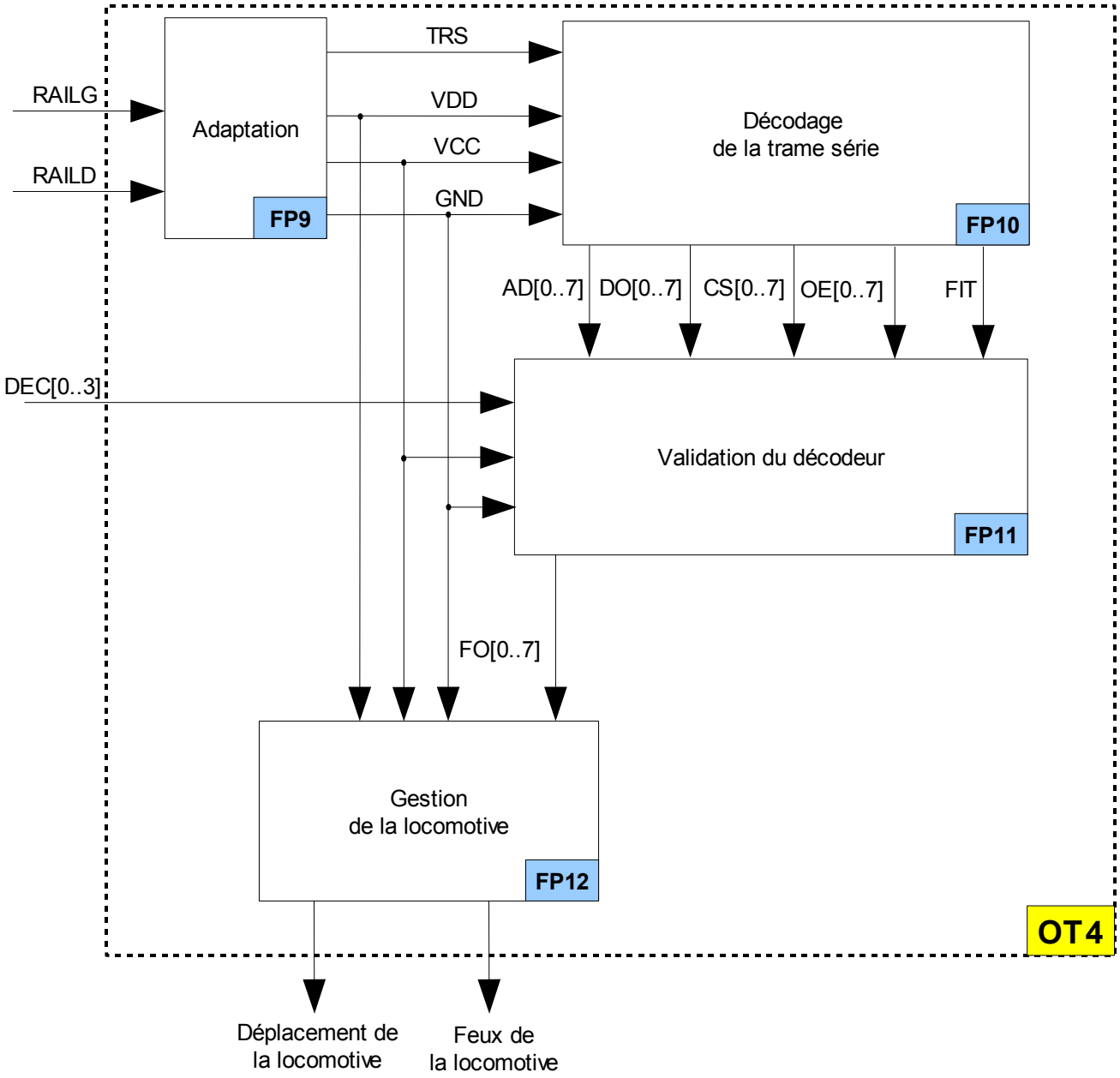
La locomotive est l'élément central du système. On la retrouve ici sous forme d'un moteur commandé par des composants discrets. On peut aussi utiliser (OT6) une locomotive ROCO©.

1-2 Fonction d'usage

Déplacer sur un circuit des wagons.

2 Étude fonctionnelle

2-1 Schéma fonctionnel de degré 1



2-2 Définition des fonctions principales

FP9 (Adaptation)

- Elle adapte l'énergie reçue par les rails au système.

FP10 (Décodage de la trame série)

- Elle décode la trame reçue par les rails et la convertit en parallèle sous deux mots de 8 bits.

FP11 (Validation du décodeur)

- Elle vérifie si l'ordre émis est correct et s'il est pour ce décodeur.

FP12 (Gestion de la locomotive)

- Elle gère le sens de déplacement et la vitesse de la locomotive.

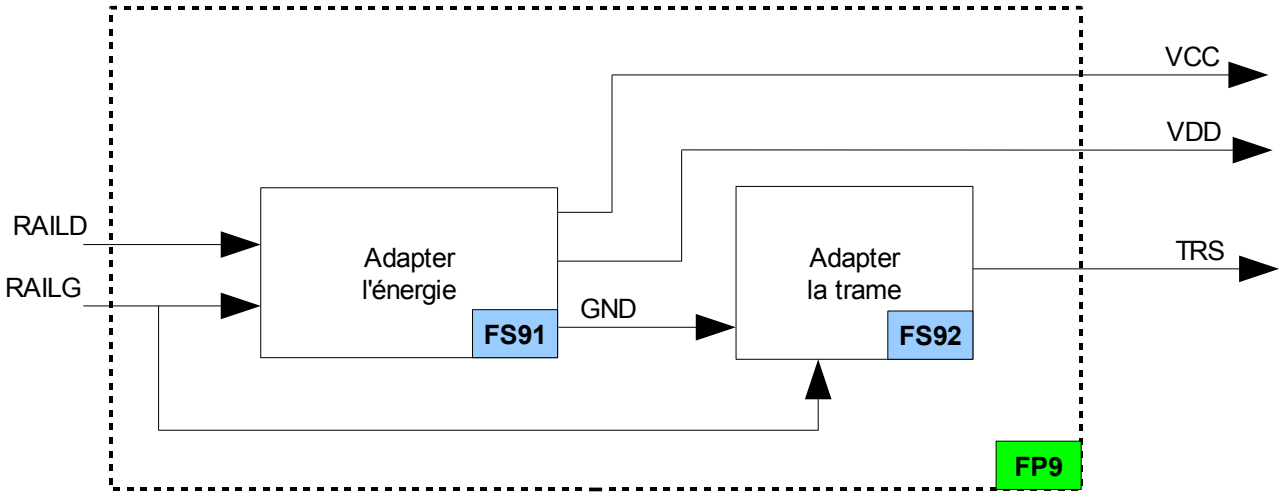
2-3 Étude fonctionnelle de degré 2

2-3-1 Étude fonctionnelle de FP9

rôle : Convertir l'énergie reçue en tensions continues, et rendre les signaux de commande compatibles TTL.

entrée(s) :
RAILG : Trame série compatible NMRA d'amplitude ±20V.
RAILD : Trame série compatible NMRA d'amplitude ±20V, en opposition avec RAILG.
sortie(s) :
VCC : Alimentation continue +5V.
VDD : Alimentation continue +12V.
GND : Point commun.
TRS : Trame série compatible niveau TTL.

Schéma fonctionnel :



Etude de FS91

rôle : Convertir l'énergie reçue en tensions continues

entrée(s) :
RAILG : Trame série compatible NMEA d'amplitude ±20V.
RAILD : Trame série compatible NMEA d'amplitude ±20V, en opposition avec RAILG.
sortie(s) :
VCC : Alimentation continue +5V.
VDD : Alimentation continue +12V.
GND : Point commun.

Etude de FS92

rôle : Rendre les signaux de commande compatibles TTL.

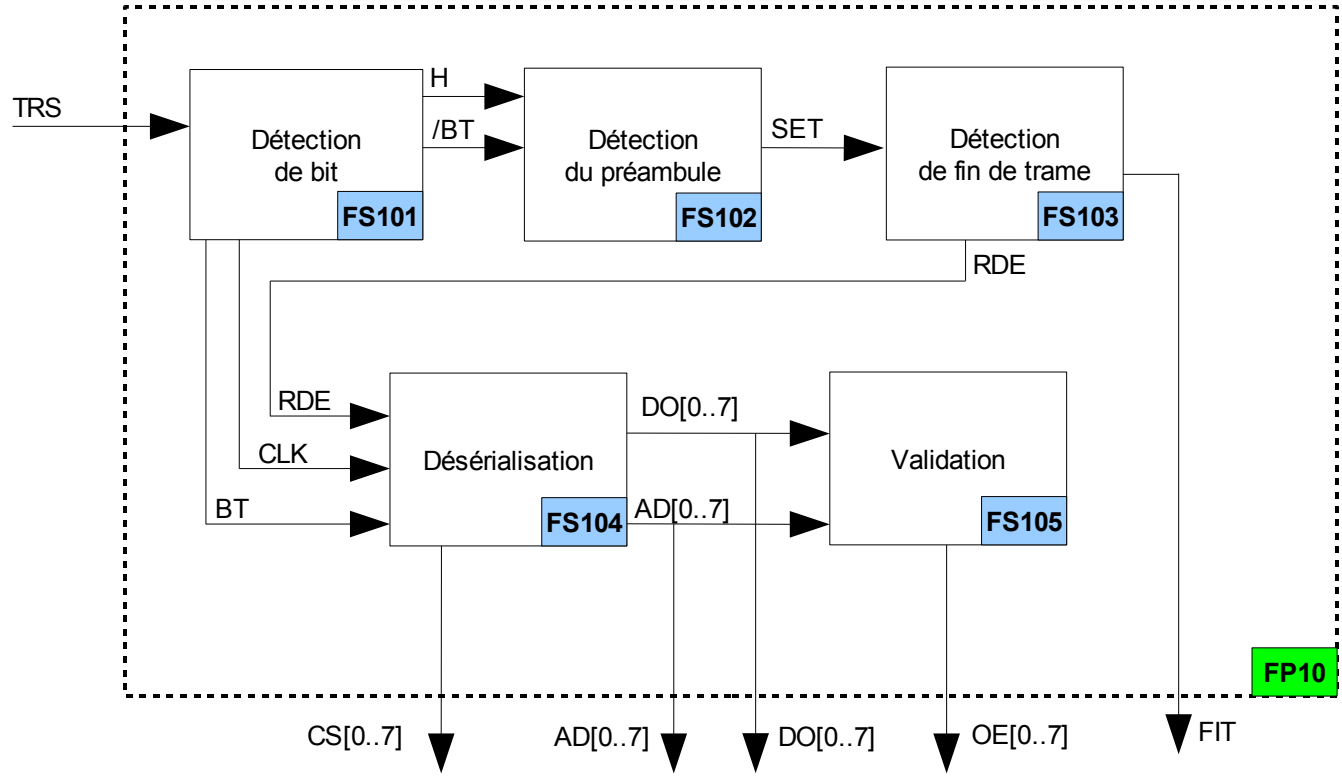
entrée(s) :
RAILG : Trame série compatible NMEA d'amplitude ±20V.
sortie(s) :
TRS : Trame série compatible niveau TTL.

2-3-2 Étude fonctionnelle de FP10

rôle : Mettre les informations reçues par la trame série en parallèle.

entrée(s) :
TRS : Trame série compatible niveau TTL
sortie(s) :
AD[0..7] : Octet image de l'adresse récupérée par la trame série.
DO[0..7] : Octet image de la donnée récupérée par la trame série.
CS[0..7] : Octet image du contrôle récupéré par la trame série.
OE[0..7] : Octet image du calcul du contrôle.
FIT : Information logique indiquant la fin d'une trame série.

Schéma fonctionnel



Etude de FS101

rôle : Détecter les états logiques des bits reçus par la trame série

entrée(s) :
TRS : Trame série compatible niveau TTL

sortie(s) :
CLK : Signal d'horloge permettant la désérialisation
H : Signal d'horloge pour la détection du préambule
BT : État du bit reçu (1 ou 0)
/BT : État complémentaire du bit reçu

Etude de FS102

rôle : détecter le préambule de la trame série (au moins 10 bits successifs à l'état « 1 »).

entrée(s) :
H : Signal d'horloge pour la détection du préambule
/BT : État complémentaire du bit reçu

sortie(s) :
SET : Information logique indiquant la fin d'un préambule.

Etude de FS103

rôle : détecter la fin de la trame série

entrée(s) :
- H : Signal d'horloge pour la détection du préambule
- SET : Information logique indiquant la fin d'un préambule.

sortie(s) :
- RDE : Information logique active pendant la transmission des 3 derniers octets de la trame série.
- FIT : Information logique indiquant la fin d'une trame série.

Etude de FS104
rôle : récupérer en parallèle les mots reçus de la trame série

entrée(s) :
- CLK : Signal d'horloge permettant la désérialisation
- BT : État du bit reçu (1 ou 0)
- RDE : Information logique active pendant la transmission des 3 derniers octets de la trame série.

sortie(s) :
- AD[0..7] : Octet image de l'adresse récupérée par la trame série.
- DO[0..7] : Octet image de la donnée récupérée par la trame série.
- CS[0..7] : Octet image du contrôle récupéré par la trame série.

Etude de FS105

rôle : calculer l'octet de contrôle de la trame reçue.

entrée(s) :
- AD[0..7] : Octet image de l'adresse récupérée par la trame série.
- DO[0..7] : Octet image de la donnée récupérée par la trame série.

sortie(s) :
- OE[0..7] : Octet image du calcul du contrôle.

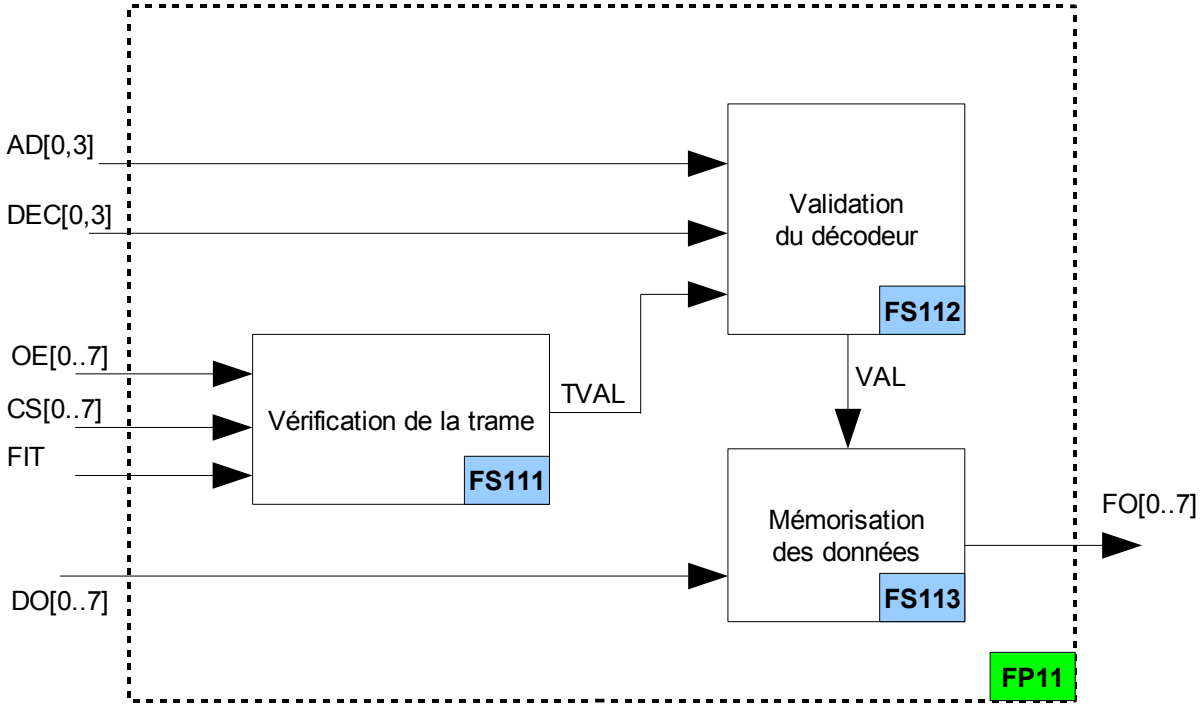
2-3-3 Étude fonctionnelle de FP11

rôle : Vérifier que la trame reçue est pour le bon décodeur.

entrée(s) :
- AD[0..7] : Octet image de l'adresse récupérée par la trame série.
- DO[0..7] : Octet image de la donnée récupérée par la trame série.
- CS[0..7] : Octet image du contrôle récupéré par la trame série.
- OE[0..7] : Octet image du calcul du contrôle.
- DEC[0..3] : Information binaire sur 4 bits représentant le numéro du décodeur.

sortie(s) :
- FO[0..7] : Mot de 8 bits image de la fonction à réaliser sur l'OT.

Schéma fonctionnel



Etude de FS111
rôle : Vérifier la bonne adresse de consigne.

entrée(s) :
- OE[0..7] : Mot de 8 bits image du calcul du contrôle.
- CS[0..7] : Mot de 8 bits image du contrôle récupéré par la trame série.
- FIT : Information logique indiquant la fin d'une trame série.

sortie(s) :
- TVAL : Information binaire actif à l'état haut validant la bonne réception de la trame NMEA.

Etude de FS112
rôle : Permettre d'identifier la commande reçue si l'adresse de consigne est correcte.

entrée(s) :
- AD[0..3] : les 4 bits de poids faible du bus AD identifiant le numéro du décodeur auquel la trame est destinée.
- DEC[0..3] : Information binaire sur 4 bits représentant le numéro du décodeur.
- TVAL : Information binaire actif à l'état haut validant la bonne réception de la trame NMEA.

sortie(s) :
- VAL : Information binaire actif à l'état haut validant le bon décodeur.

Etude de FS113
rôle : Mémorise l'octet de donnée si c'est le bon décodeur

entrée(s) :
- DO[0..7] : Mot de 8 bits image de la donnée de la trame NMEA
- VAL : Information binaire actif à l'état haut validant le bon décodeur.

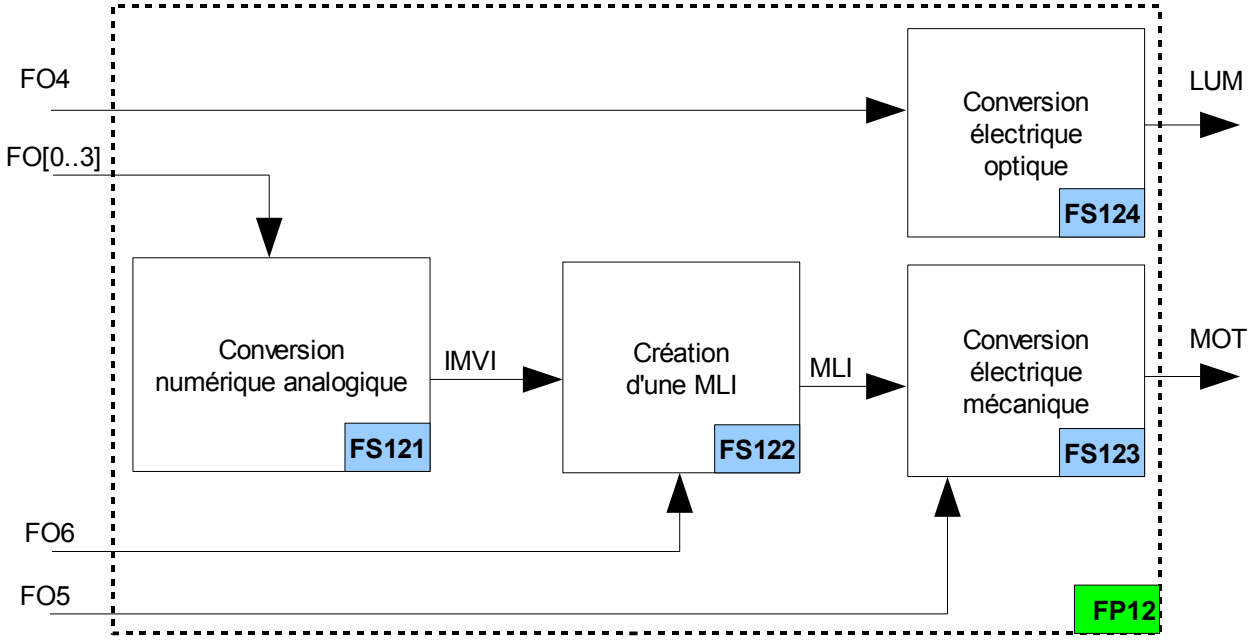
sortie(s) :
- FO[0..7] : Mot de 8 bits image de la fonction à réaliser sur l'OT.

2-3-4 Étude fonctionnelle de FP12

rôle : Commander la locomotive.

entrée(s) :
FO[0..7] : Mot de 8 bits image de la fonction à réaliser sur l'OT.
sortie(s) :
LUM : Allumage des feux de la locomotive
MOT : Déplacement de la locomotive

Schéma fonctionnel



Etude de FS121

rôle : Créer une tension analogique image de la vitesse de consigne.
entrée(s) :
FO[0..3] : Mot de 4 bits image de la fonction à réaliser sur l'OT.
sortie(s) :
IMVI : Information analogique image d'une vitesse de locomotive.

Etude de FS122

rôle : Créer un signal carré de fréquence fixe et de rapport cyclique variable.
entrée(s) :
IMVI : Information analogique image d'une vitesse de locomotive.
FO6 : Information binaire actif à l'état haut commandant une vitesse de locomotive.
sortie(s) :
MLI : Signal carré à rapport cyclique variable.

Etude de FS123

rôle : Faire déplacer la locomotive.
entrée(s) :
MLI : Signal carré à rapport cyclique variable.
FO5 : Information binaire donnant le sens de déplacement de la locomotive (0 arrière, 1 avant).

sortie(s) :
MOT : Déplacement de la locomotive.

Étude de FS124

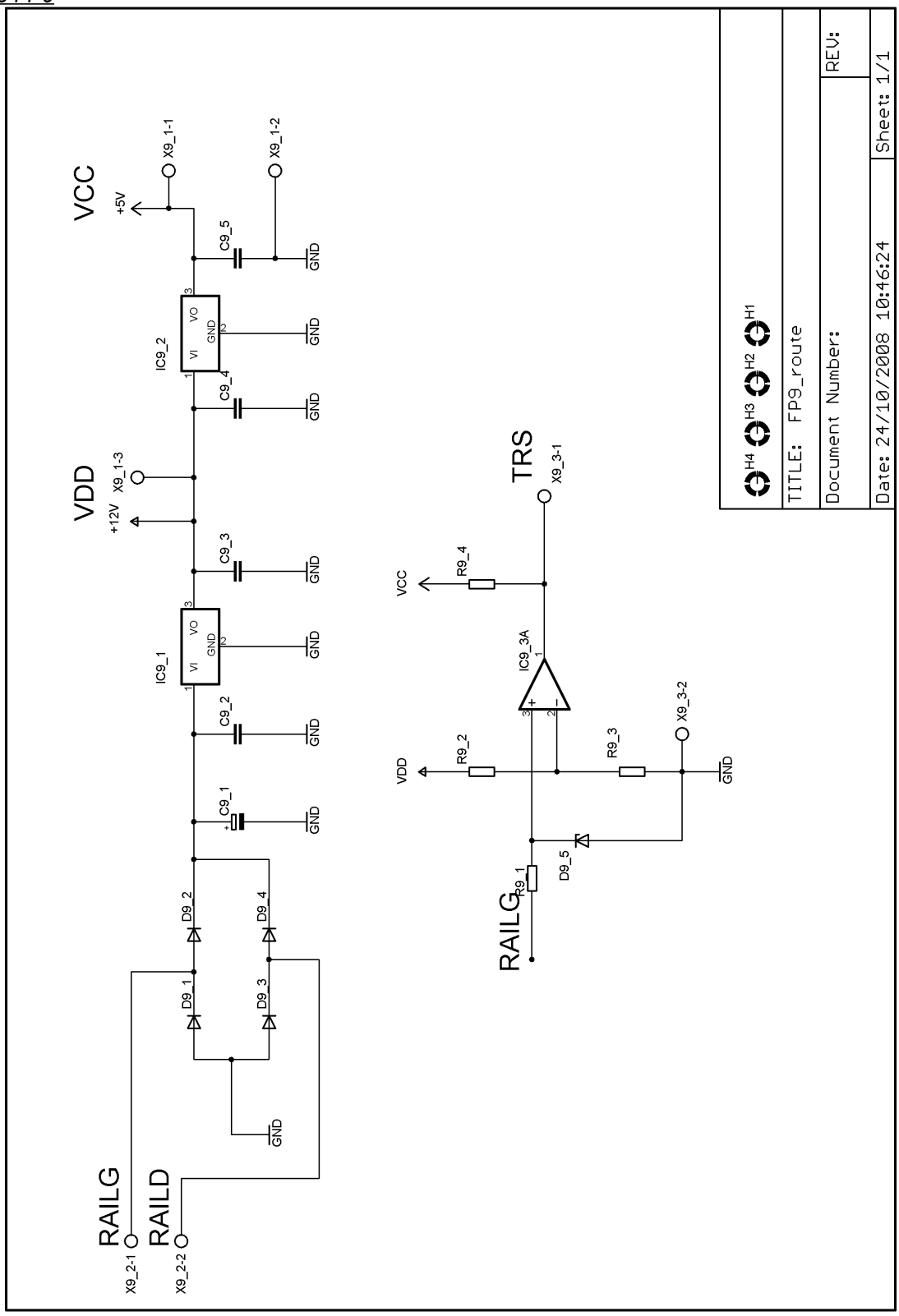
rôle : Allumer la lumière de la locomotive.
entrée(s) :
FO4 : information binaire activant ou non la lumière de la locomotive.

sortie(s) :
LUM : information visuelle.

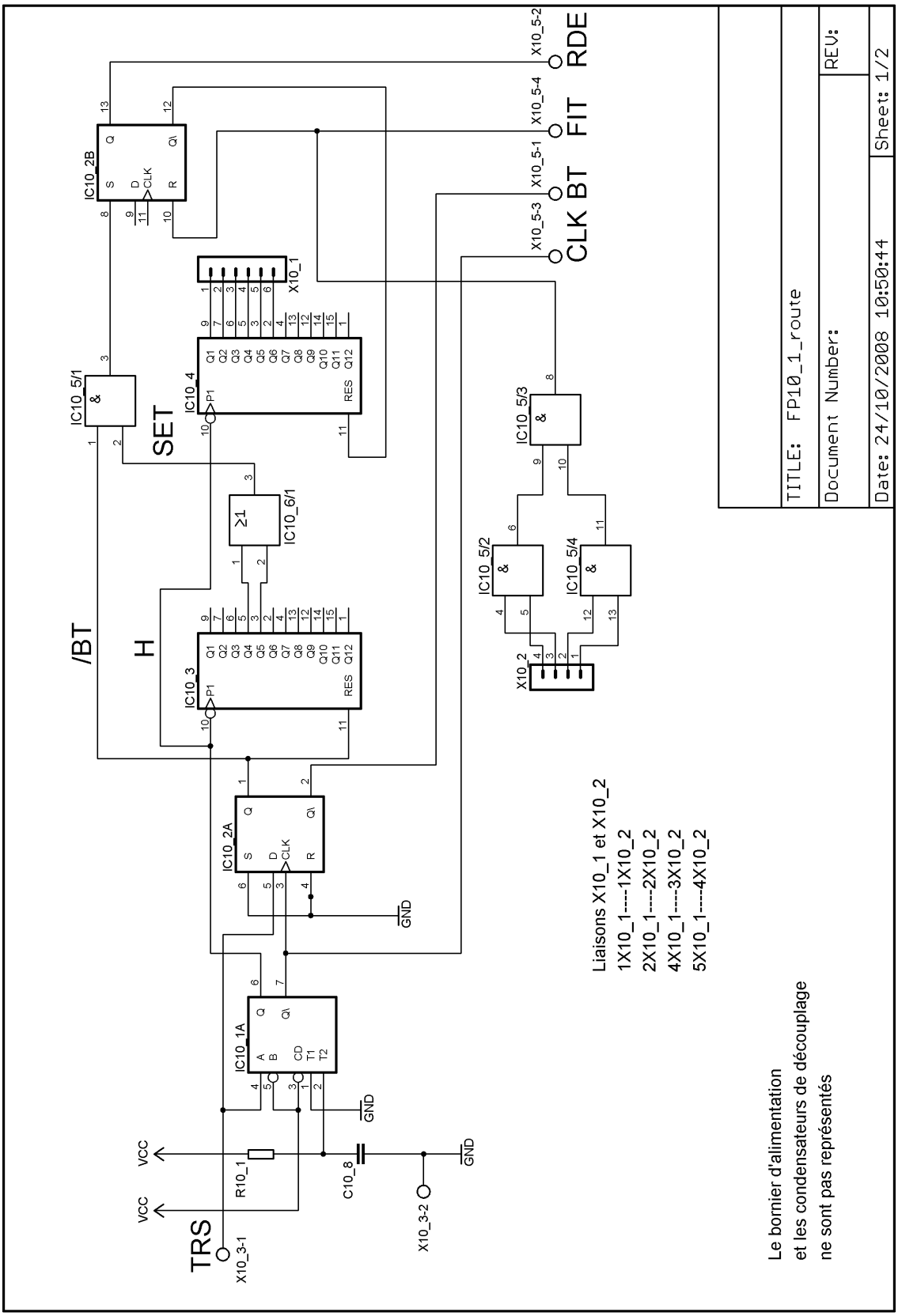
3.Étude structurelle

3-1 Schémas structurels

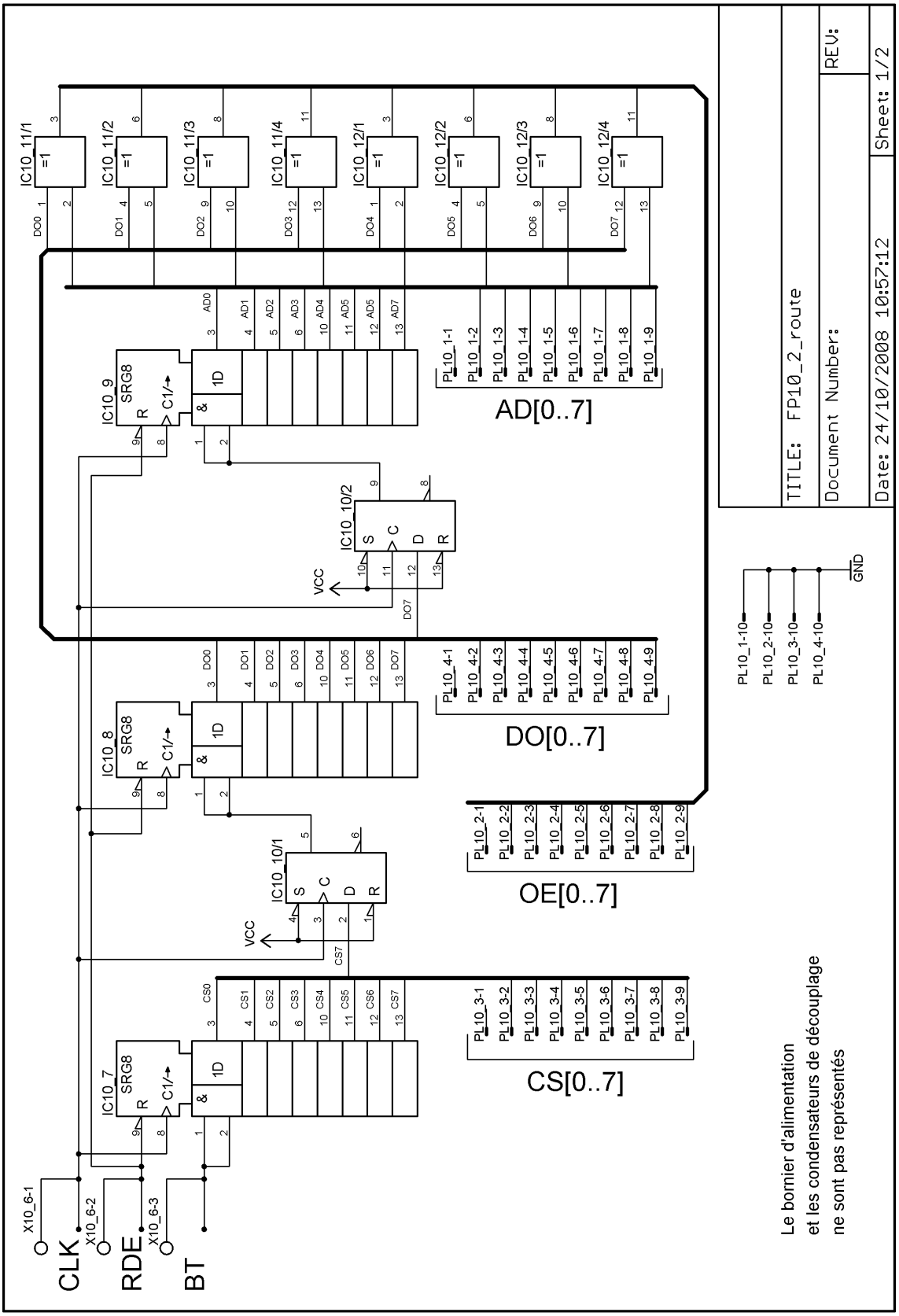
Structure de FP9



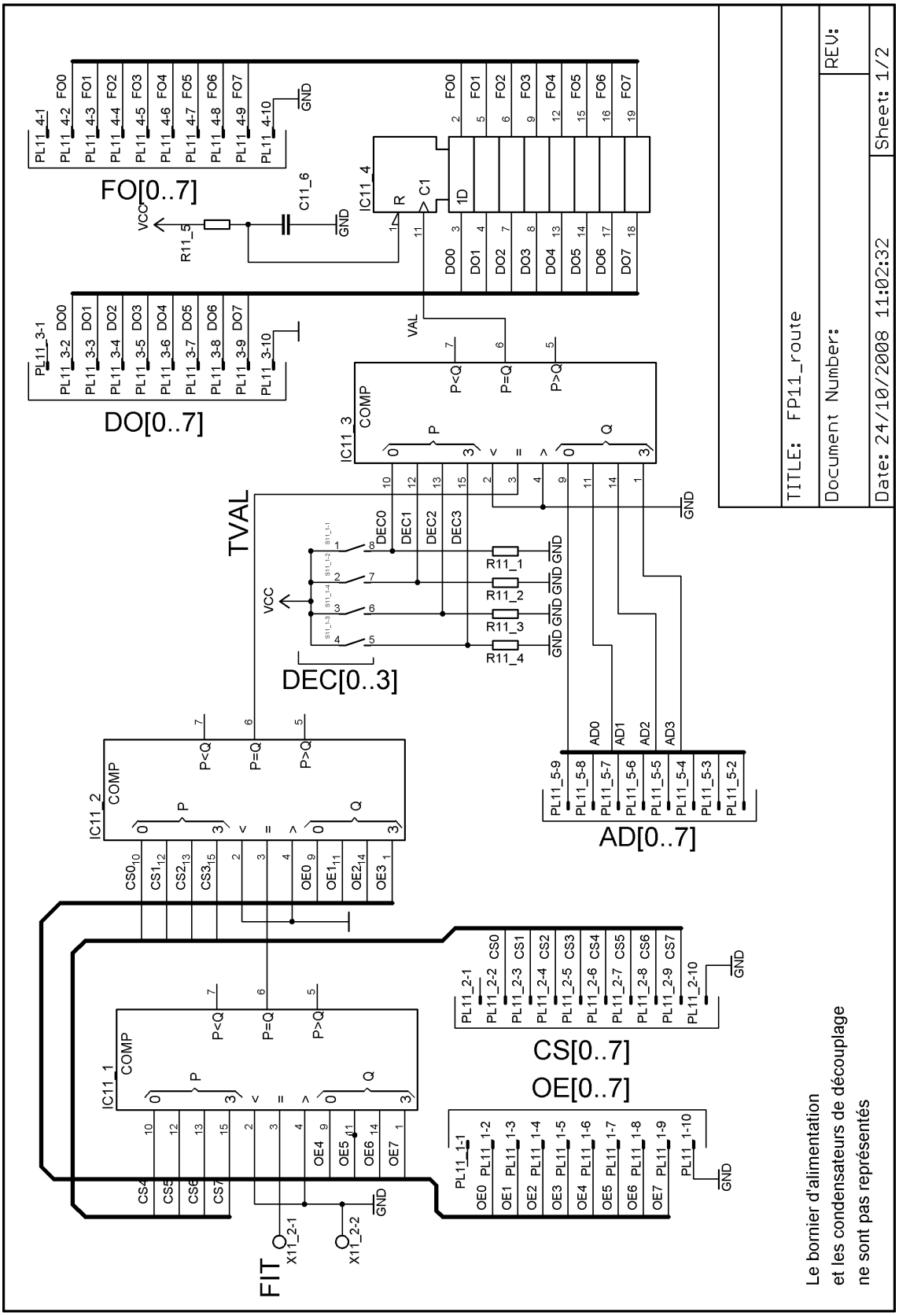
Structure partielle de FP10 (FS101 – FS102 – FS103)



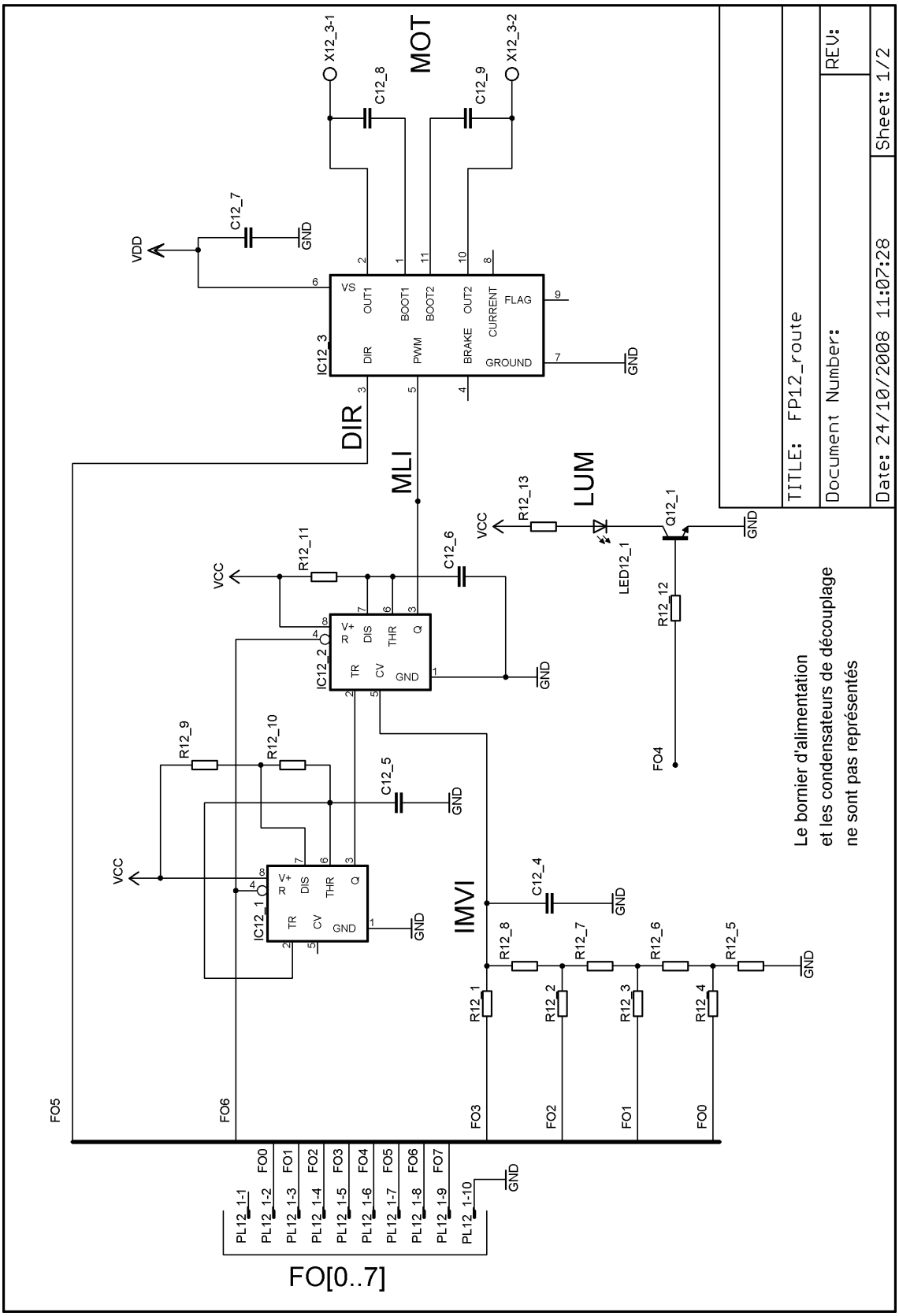
Structure partielle de FP10 (FS104 – FS105)



Structure de FP11



Structure de FP12



3-2 Nomenclature

Réf.	Désignation	Valeur	Qte	Réf.	Désignation	Valeur	Qte
IC9_1	Régulateur	7812	1	IC11_1 à IC11_3	Comparateur	7485	3
IC9_2	Régulateur	7805	1	IC11_4	Bascules	74273	1
IC9_3	Ampli Op	LM393	1	R11_1 à R11_4	Résistance	10K	4
R9_1	Résistance		1	R11_5	Résistance		
R9_2	Résistance			C11_1 à C11_4	Condensateur	100nF	4
R9_3				C11_5	Condensateur	220uF	1
R9_4	Résistance	12K	1	C11_6	Condensateur		
C9_1	Condensateur	220uF	1	PL11_1 à PL11_5	Connecteur	HE10	5
C9_2	Condensateur	330nF	1	S11_1	Dip switch	4	
C9_3	Condensateur	100nF	1	X11_1 et X11_2	Bornier	2 plots	2
C9_4	Condensateur	330nF	1	IC12_1 et IC12_2		NE555	2
C9_5	Condensateur	100nF	1	IC12_3	Amplificateur	LMD18200	1
D9_1 à D9_4	Diode	1N4004	4	R12_1 à R12_5	Résistance	4,7K	5
D9_5	Diode Zener	BZX85C	1	R12_6 à R12_8	Résistance	2,2KK	3
X9_1	Bornier	3 plots	1	R12_9	Résistance		
X9_2 et X9_3	Bornier	2 plots	2	R12_10	Résistance		
IC10_1	Monostable	4538	1	R12_11	Résistance	33K	1
IC10_2	Portes Logiques	4013	1	R12_12	Résistance		
IC10_3 et IC10_4	Compteur	4040	2	R12_13	Résistance		
IC10_5	Portes Logiques	7408	1	C12_1 et C12_2	Condensateur	100nF	2
IC10_6	Portes Logiques	7432	1	C12_3	Condensateur	220uF	1
IC10_7 à IC10_9	Bascules	74164	3	C12_4	Condensateur	15nF	1
IC10_10	Bascules	7474	1	C12_5	Condensateur		
IC10_11 et IC10_12	Portes Logiques	7486	2	C12_6	Condensateur	15nF	1
R10_1	Résistance			C12_7	Condensateur	100nF	1
C10_1 à C10_6	Condensateur	100nF	6	C12_8 et C12_9	Condensateur	10nF	2
C10_7	Condensateur	220uF	1	LED12_1	LED 5mm		1
C10_8	Condensateur			Q12_1	Transistor	BC337	
C10_9 à C10_14	Condensateur	100nF	6	PL12_1	Connecteur	HE10	1
C10_15	Condensateur	220uF	1	X12_1 à X12_3	Bornier	2 plots	3
PL10_1 à PL10_4	Connecteur	HE10	4				
X10_1	Connecteur		1				
X10_2	Connecteur		1				
X10_3 et X10_4	Bornier	2 plots	2				
X10_5	Bornier	4 plots	1				
X10_6	Bornier	3 plots	1				
X10_7	Bornier	2 plots	1				

OT5 La souris

1 Mise en situation du système technique

1-1 Introduction

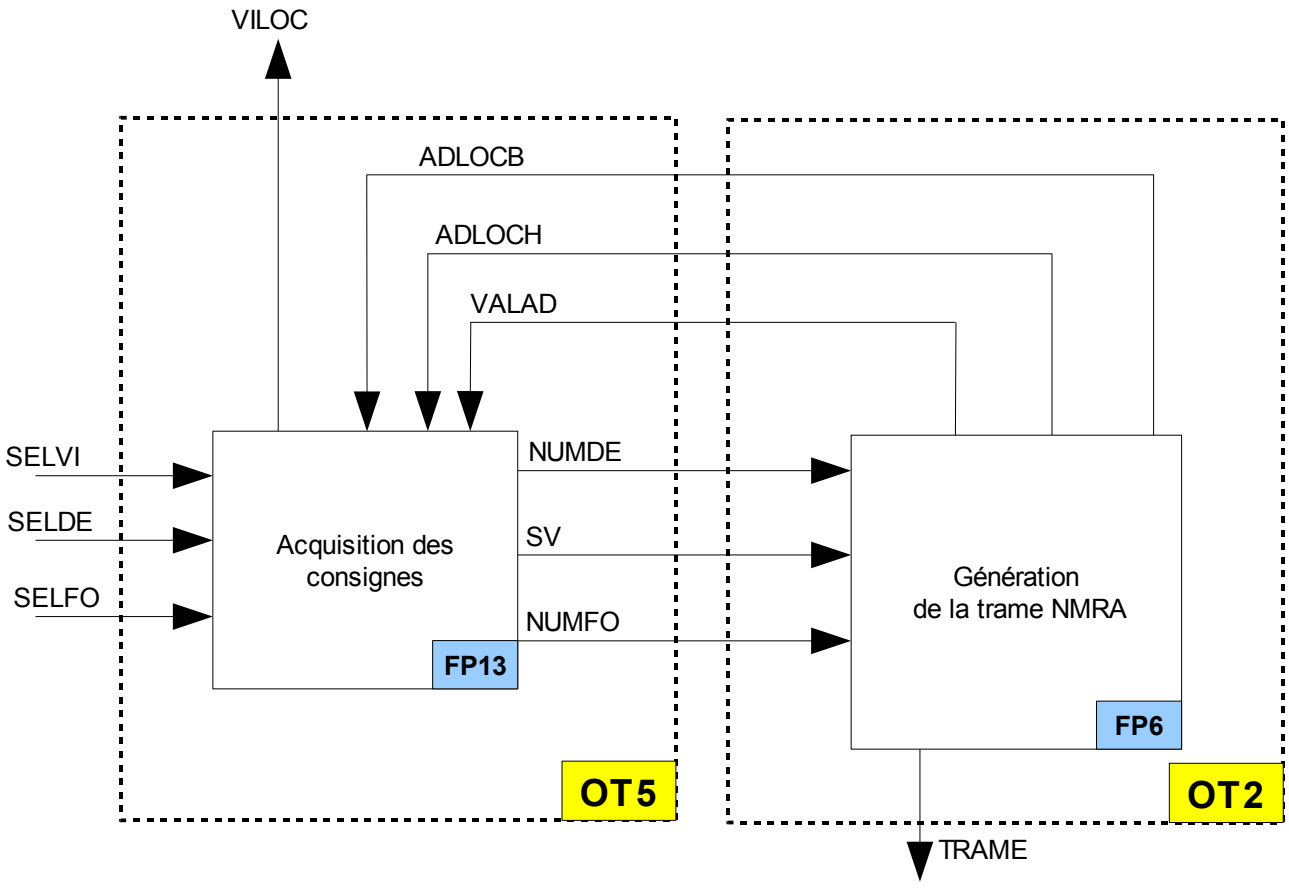
La souris permet la commande d'un train ou éventuellement d'accessoires (éclairage des voies, barrière ...). Elle doit être facile d'emploi pour pouvoir être utilisée par un enfant.

1-2 Fonction d'usage

Commander des locomotives.

2 Étude fonctionnelle

2-1 Schéma fonctionnel de degré1



2-2 Définition de la fonction principale

FP13 (Acquisition des consignes)

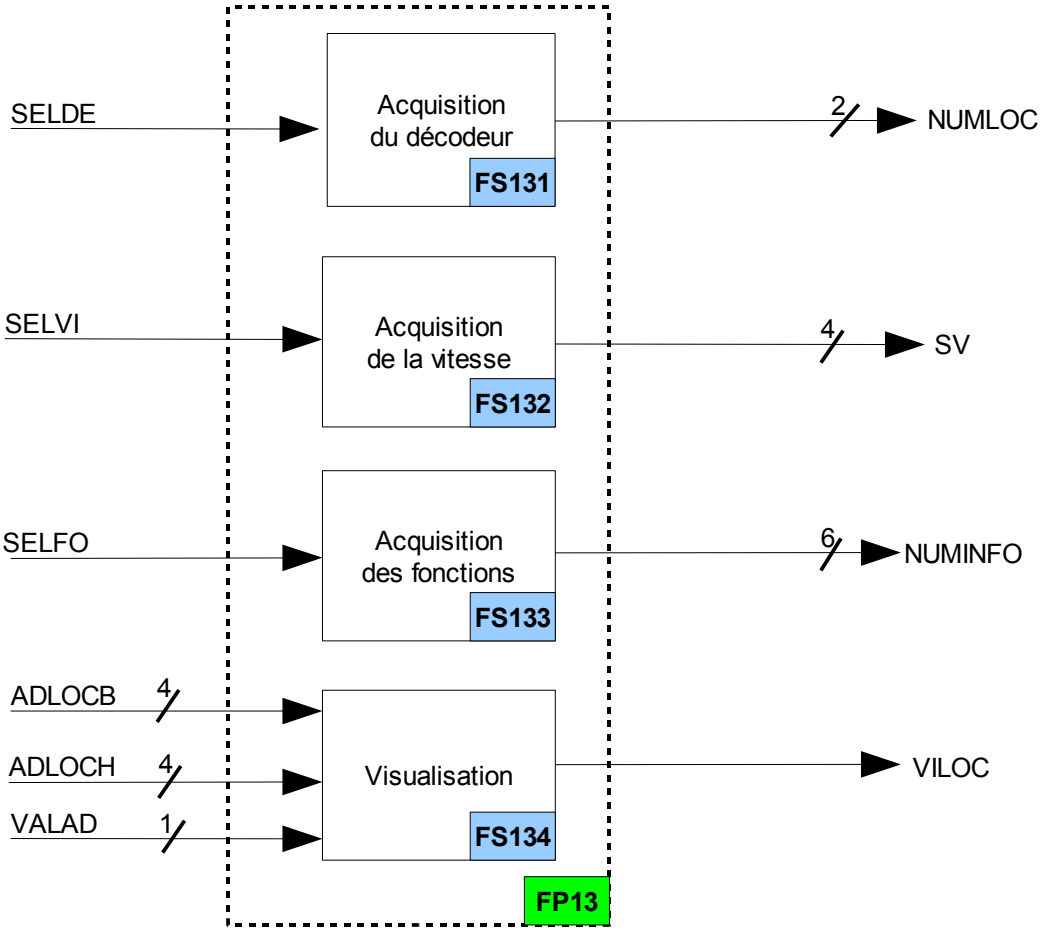
- Elle acquièrt les consignes de l'utilisateur :
  - Numéro du décodeur.
  - Vitesse et sens de déplacement.
  - Utilisation des fonctions.
- Elle visualise certaines consignes acquises :
  - Numéro du décodeur.

2-3 Étude fonctionnelle de degré2

2-3-1 Étude fonctionnelle de FP13

rôle : Acquérir et visualiser les consignes de l'utilisateur.

Schéma fonctionnel :



Étude de FS131
rôle : Acquérir le numéro du décodeur à commander.

entrée(s) :
SELDE : Information manuelle par l'intermédiaire de 2 boutons poussoirs (Haut et Bas) permettant de sélectionner un numéro de décodeur.
sortie(s) :
NUMLOC : Mot binaire de 2 bits (Up et Down), actifs sur des fronts descendants.

Étude de FS132
rôle : Acquérir la vitesse et le sens de déplacement de la locomotive.

entrée(s) :
SELVI : Information manuelle par l'intermédiaire d'un encodeur rotatif, permettant de sélectionner une vitesse et un sens de déplacement.
sortie(s) :
SV : Mot binaire de 5 bits, image de la vitesse et du sens de déplacement désiré.

SV_4	SV_3	SV_2	SV_1	SV_0	
X	0	0	0	0	Vitesse nulle
0	0	0	0	1	Marche arrière : Vitesse mini
0	1	1	1	1	Marche arrière : Vitesse maxi
1	0	0	0	0	Marche avant : Vitesse mini
1	1	1	1	1	Marche avant : Vitesse maxi

Étude de FS133
rôle : Acquérir la commande des différentes fonctions disponibles.

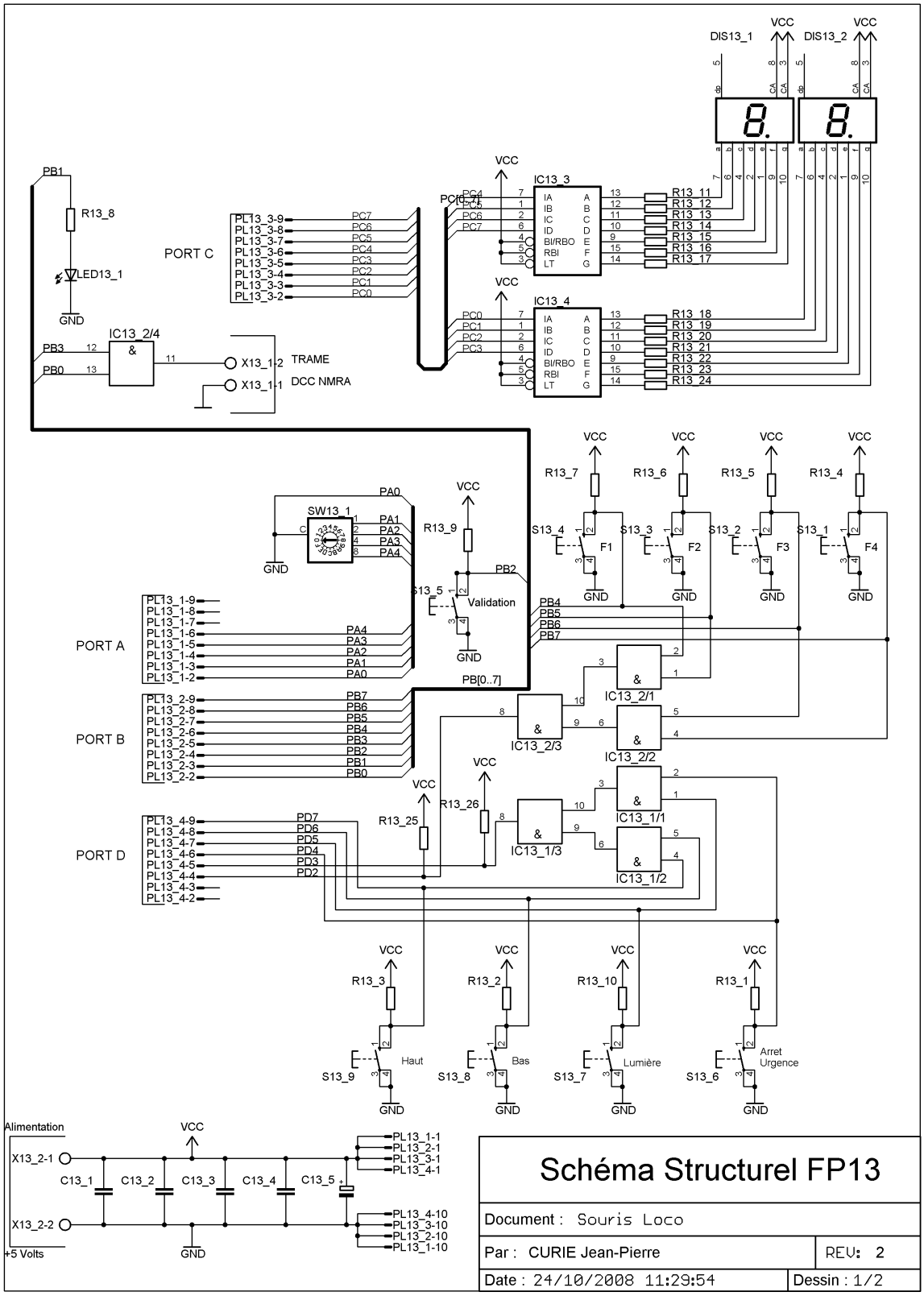
entrée(s) :
SELFO : Information manuelle par l'intermédiaire de 6 boutons poussoirs (Haut et Bas) permettant de sélectionner une fonction parmi 5 et de la valider.
sortie(s) :
NUMFO : Mot binaire de 6 bits, actifs sur des fronts descendants.

Étude de FS134
rôle : Afficher le numéro du décodeur à utiliser.

entrée(s) :
ADLOCB : Mot binaire sur 4 bits image de l'unité du numéro du décodeur codé en BCD.
ADLOCH : Mot binaire sur 4 bits image de la dizaine du numéro du décodeur codé en BCD.
VALAD : Mot binaire sur 1 bit image actif à l'état 1 lorsque le décodeur choisi est validé.
sortie(s) :
VILOC : Information visuelle du numéro du décodeur et de sa validation.

3 Étude structurelle

3-1 Schéma structurel



3-2 Nomenclature

Réf.	Désignation	Valeur	Qte	Réf.	Désignation	Valeur	Qte
IC13_1 et IC13_2	Portes logiques	7408	2	S13_1 à S13_9	Poussoir	DT6	9
IC13_3 et IC13_4	Décodeurs	74LS47	2	SW13_1	Switch dil		1
R13_1 à R13_7	Résistances	10K	7	X13_1 et X13_2	Borniers	2 plots	2
R13_8	Résistance						
R13_9 et R13_10	Résistances	10K	2	PL13_1 à PL13_4	Connecteur	HE10	4
R13_11 à R13_24	Résistance						
R13_25 et R13_26	Résistances	10K	2				
C13_1 à C13_4	Condensateurs	100nF	4				
C13_5	Condensateur	100uF	1				
DIS13_1 à DIS13_2	Afficheur	TDSR5150	2				

Travail demandé

1 Constitution des groupes de travail

L'étude du système est répartie entre 6 groupes de travail (binôme).

Groupe n°1 :

- OT1 Fonctions FP1 et FP2.

Groupe n°2 :

- OT1 Fonctions FP1 et FP3.

Groupe n°3 :

- OT1 Fonction FP4.
- OT2 Fonction FP5 et FP6.

Groupe 4 :

- OT2 Fonctions FP6 et FP7.
- OT4 Fonction FP9.

Groupe 5 :

- OT2 Fonction FP6.
- OT5 Fonction FP13.

Groupe 6 :

- OT4 Fonctions FP10 à FP12.

2 Travail commun à tous les groupes

- Connaissance de la trame DCF-77.
- Connaissance de la trame DCC NMRA.
- Connaissance fonctionnelle jusqu'au 1er degré du système.
- Étude qualitative de vos fonctions.
- Étude quantitative de vos fonctions.
- Simulation de vos fonctions.
- Réalisation des maquettes
- Validation expérimentale : tests et relevés "commentés" de mesures
- (oscillogrammes etc. …..)
- Montage de l'ensemble sur un support tout en permettant au jury un contrôle aisé des cartes.
- Rédaction d'un rapport (voir proposition de plan du rapport au paragraphe 4).
- Préparer un exposé oral en tenant compte de la grille d'évaluation qui vous sera présentée.

Conseil : La présentation fonctionnelle jusqu'au 1er degré ne doit pas excéder 5mn pour l'épreuve orale.

Etude fonctionnelle:

Entourer les fonctions secondaires sur le schéma structurel et identifier les signaux reliant ces fonctions.

Transcrire l'analyse fonctionnelle de second degré en chronogrammes décrivant le fonctionnement des fonctions principales étudiées.

Réalisation et essais :

Réaliser le(s) typon(s), fabriquer la carte et procéder aux réglages.

Faire un ou plusieurs relevés expérimentaux (**oscillogrammes**) permettant de valider le fonctionnement.

Programmation :

Pour tous les travaux de programmation, produire algorithme et programme avec commentaires.

Remarque importante relative à tous les groupes

Les questions posées ne sont pas exhaustives. Elles sont un guide pour vous aider dans la compréhension de votre système et la rédaction de votre dossier.

Ce dernier ne devra donc pas se présenter comme une suite chronologique de réponses à ces questions.

3 Travail de chaque binôme

Travail groupe 1 :

Étude de FP1

Écrire l'algorithme et le programme permettant d'afficher un compteur de 0 à 9999.

Étude de FP2

Choisir la fréquence de multiplexage des afficheurs.
Concevoir FS21.
Concevoir FS22 à bascule JK.
Choisir les afficheurs.
Dimensionner les résistances R2_2 à R2_5.
Dimensionner les résistances R2_6 à R2_12.
Réaliser la fonction FP2.

Travail groupe 2 :

Étude de FP1

Écrire l'algorithme et le programme permettant le départ du train à intervalles réguliers.

Étude de FP3

Analyser la documentation de l'ISD1400.
Analyser la documentation du TDA 2040.
Analyser le fonctionnement total de FP3.
Concevoir FS31, pour que le message de départ dure 4 à 5 secondes.
Concevoir FS32.
Modifier le schéma pour pouvoir n'utiliser qu'une seule mémoire analogique.
Réaliser la fonction FP3 avec une seule ou deux mémoires..

Travail groupe 3 :

Étude de FP4

Expliquer le fonctionnement de IC4_5.
Dimensionner R4_2 à R4_5.
Dimensionner les composants : C4_2 à C4_6 , R4_6 et P4_1 afin d'avoir des fréquences de sortie de :

- 500 Hz lorsque la sortie 5 de IC4_3 est à « 1 ».
- 1000 Hz lorsque la sortie 9 de IC4_3 est à « 1 ».
- 1500 Hz lorsque la sortie 5 de IC4_4 est à « 1 ».
- 3000 Hz lorsque la sortie 9 de IC4_4 est à « 1 ».

Réaliser FP4.

Étude de FP5

Analyser la documentation du LM2917.
Dimensionner C5_2 et R5_1 pour avoir le maximum d'amplitude à la sortie de IC5_2.
Concevoir FS53, afin de délivrer les signaux suivants :

ORD0 =« 0 », ORD0 =« 0 » pour une fréquence de 500 Hz.
ORD0 =« 1 », ORD0 =« 0 » pour une fréquence de 1000 Hz.
ORD0 =« 1 », ORD0 =« 1 » pour une fréquence de 1500 Hz.

Réaliser FP5.

Étude de FP6

Écrire l'algorithme et le programme permettant en fonction de PB0 et PB1 de placer une donnée sur le PORTC :

Si PB0 =« 0 » et PB1 =« 0 » alors PORTC = $FF.
Si PB0 =« 0 » et PB1 =« 1 » alors PORTC = $80.
Si PB0 =« 1 » et PB1 =« 1 » alors PORTC = $00.

Travail groupe 4 :

Étude de FP6

Écrire l'algorithme et le programme permettant de réaliser un signal d'horloge de 10 kHz sur la sortie PB3.

Étude de FP7

Expliquer le fonctionnement du système en cas de court circuit sur les rails.
Dimensionner C7_7 et R7_1.
Expliquer le rôle des diodes D7_8 et D7_9.
Réaliser FP7.

Étude de FP9

Expliquer le fonctionnement de IC9_3A.
Dimensionner R9_2 et R9_3.
Réaliser FP9.

Travail groupe 5 :

Étude de FP6

Écrire l'algorithme et le programme permettant d'afficher sur FP13 un compteur et d'incrémenter ou de décrémenter cette valeur grâce aux touches Haut et Bas (S13_9 et S13_8).
La valeur du compteur variera entre 0 et 99.

Étude de FP13

Dimensionner R13_8 et R13_11 à R13_24.
Modifier le schéma en remplaçant SW13_1 par un CAN 4bits.
Réaliser FP13.

Travail groupe 6 :

Étude de FP10

Déterminer la fonction réalisée par IC10_1A.
Dimensionner R10_1 et C10_8.
Quel est le rôle des portes OU Exclusif.
Réaliser la partie de FP10 contenant FS101 à FS103.

Étude de FP11

Définir le rôle de la structure composée de R11_5 et C11_6
Dimensionner R11_5 et C11_6.

Étude de FP12

Dimensionner R12_9, R12_10 et C12_5 pour avoir une fréquence de 1KHz à la sortie de IC12_1.
Quelle fonction réalisent les résistances R12_1 à R12_7 ?
Dimensionner R12_12 et R12_13.
Réaliser FP12.

4 Plan du rapport

Le rapport devra comporter environ 25 pages hors annexe.

Au début, Il devra contenir obligatoirement le cahier des charges du groupe (le travail demandé).

En annexe, ne pourront figurer que les documents constructeurs nécessaires à la compréhension du rapport. Il devra comporter un sommaire et les pages devront être numérotées.

Le rapport pourra suivre le plan suivant:

La partie présentation n'apparaît pas dans le dossier mais doit être parfaitement connue pour l'épreuve orale.

1. ***Étude fonctionnelle de 1er degré des objets techniques.***

- Schémas fonctionnels de 1er degré.
- Explications des fonctions principales.
- Définitions des liaisons.

2. Explications à propos des fonctions étudiées.

- Position et justification de la présence des fonctions au sein du système ;
- Schéma fonctionnel de 2nd degré des fonctions principales ;
- Schémas structurels et nomenclatures ;
- Définitions des liaisons ;
- Étude détaillée de chaque fonction secondaire qui peut comporter par exemple :
  - Schéma structurel de la fonction secondaire ;
  - Explications du fonctionnement de la fonction secondaire ;
  - Calcul ou justification des composants ;
  - Définitions des points tests ;
  - Chronogrammes théoriques et/ou oscillogrammes ;
  - Algorithme de fonctionnement ;
  - Programme de test ;
  - Etc…
- Méthode de mise en œuvre des cartes ;
- Relevés des mesures.

3. Algorithme et programmation des cartes étudiées.

4. Documents de fabrication.

- Schémas structurels (réalisés par le binôme) et nomenclatures chiffrées.
- Typons avec identification des faces (réalisés par le binôme) et schémas d'implantation.
- Plan de câblage (définition de la connectique).

Annexes

1 Le système de réception « DCF-77 »

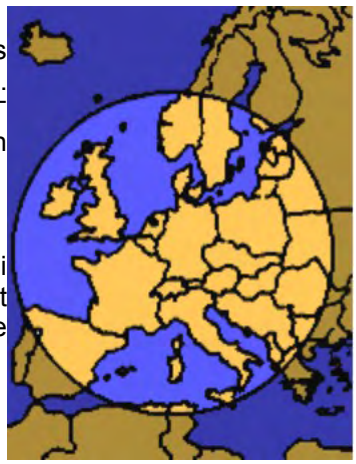
Introduction

La réception des signaux horaires DCF77 est le seul moyen en Europe d'obtenir une heure précise, de manière fiable, avec un récepteur simple et peu cher. (La réception de signaux horaires provenant d'un satellite GPS est plus difficile à mettre en oeuvre).

On peut ainsi recevoir l'heure, la date et le jour de la semaine. Le changement entre l'heure d'été et d'hiver est automatique.

L'émetteur

L'émetteur des signaux horaires DCF77 est situé en Allemagne, à Mainflingen (près de Francfort), plus précisément à 50,02° de latitude Nord, et 9,00° de longitude Est. L'information horaire est donnée par l'horloge atomique de l'INSTITUT PHYSIQUE ET DE METROLOGIE DE BRUNSWICK. Cette horloge est très précise, puisque son écart théorique est de ±1 seconde pour 1 millions d'années.



Grâce à sa position centrale en Europe, à sa puissance d'émission de 50 kW, ainsi qu'à sa grande puissance rayonnée (30 kW), les informations de cet émetteur peuvent être correctement reçues dans un rayon de 2000 km, c'est à dire dans une grande partie de l'Europe, et même dans l'extrême nord de l'Afrique.

La porteuse a une fréquence très stable, de 77,5 kHz (d'où le nom DCF77), qui dérive de l'horloge atomique. Les faibles fluctuations de cette fréquence sont principalement dues à la propagation des grandes ondes dans l'atmosphère. Son écart relatif par rapport à la fréquence de 77,5 kHz est en moyenne sur 100 jours, de moins de 2.10E-13. Par conséquent, elle peut être utilisée pour la synchronisation d'oscillateurs nécessitant une grande précision.

En cas de maintenance ou de dysfonctionnement, un émetteur de réserve est mis en fonction. Il arrive cependant que les signaux horaires cessent d'être émis, notamment lors d'orages, pendant un temps généralement très court. Il est donc nécessaire que l'horloge radio pilotée possède sa propre horloge interne.

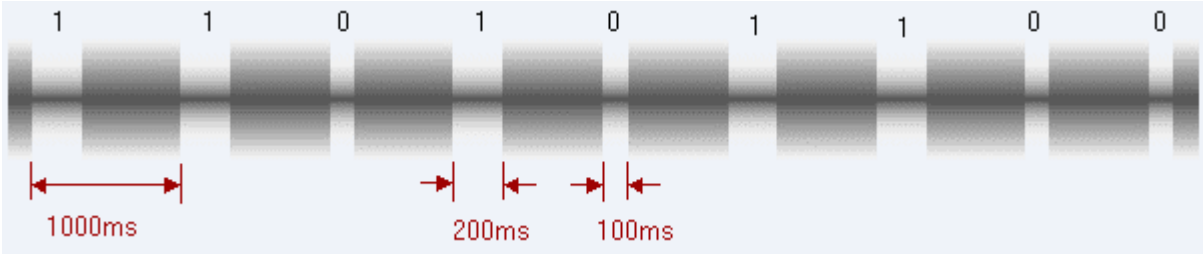
Le signal horaire DCF77 est composé d'une fréquence porteuse très stable de 77,5 kHz, modulée en amplitude par les signaux horaires codés en BCD (binary coded digital).

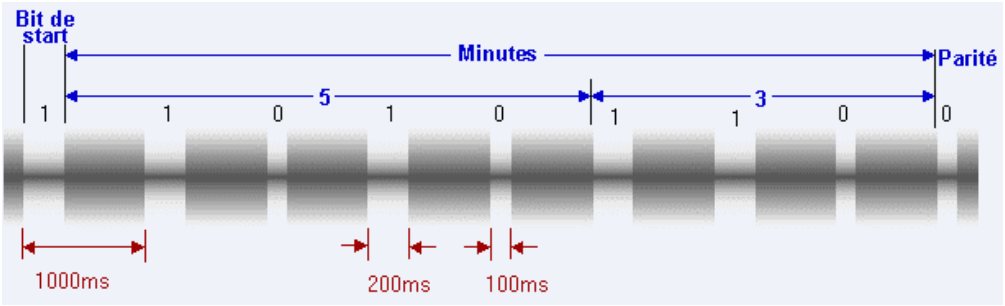
Les informations horaires sont émises par trame d'une minute. Chaque trame est divisée en soixante secondes, chacune d'entre elles débutant par le front de l'impulsion.

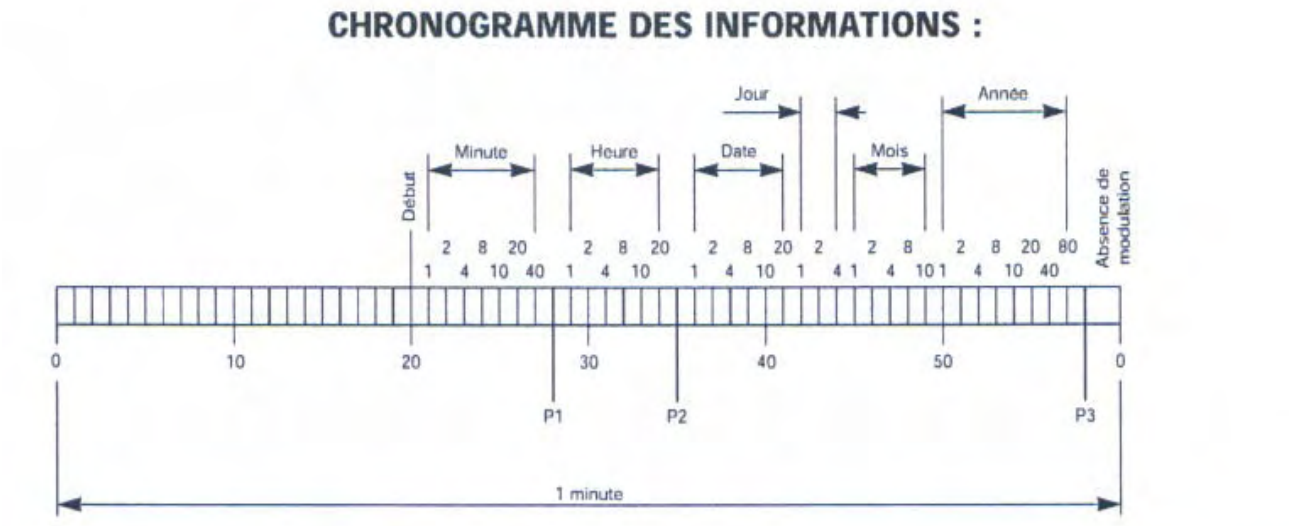
Il faut noter que, pour la 59ème seconde, il n'y a pas d'impulsion afin de permettre au décodeur de repérer le début d'une trame. Ainsi, l'impulsion suivante détermine le début de la trame suivante. Toute absence d'impulsion plus grande que 999 ms doit donc être considérée comme le début d'une nouvelle trame.

L'onde porteuse est modulée par des impulsions, au rythme d'une par seconde. Ces impulsions se traduisent chaque seconde par une diminution de 25% de l'amplitude du signal reçu. La durée d'une impulsion détermine le niveau du bit reçu, à savoir :

- une impulsion de 100 ms représente un bit à 0
- une impulsion de 200 ms représente un bit à 1







CORRESPONDANCE ENTRE LE NUMÉRO DE BIT, SA DÉNOMINATION ET SA SIGNIFICATION

2 La trame DCC NMRA

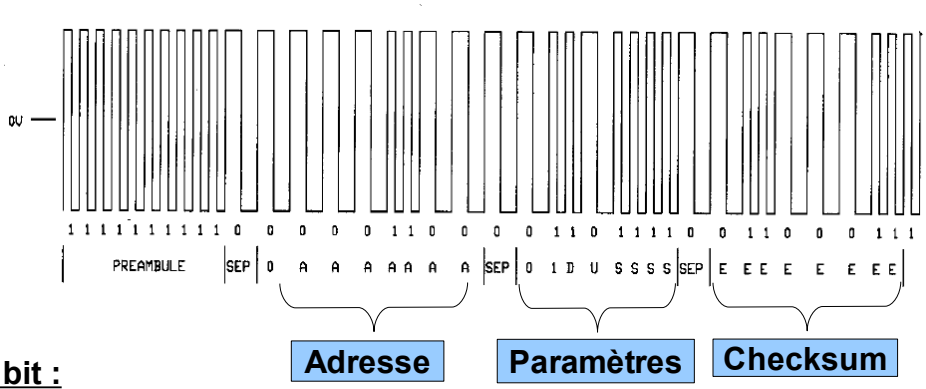
Le protocole DCC a été défini par la NMRA (National Model Railroad Association) aux USA. Le protocole en question a été validé définitivement en 1994, en tant que 'standard' national.

La trame (ensemble des codes envoyés)

Les messages du protocole DCC sont précédés d'un **préambule**[1] qui permet de repérer le début d'un message, et formés de **mots de huit bits**, séparés par un bit de séparation.

Les mots qui forment le corps du message contiennent des informations de type de commande, adresse, et des paramètres si nécessaire, suivis d'un code de vérification (checksum) qui permet de s'assurer de l'intégrité du message reçu.

Dans le protocole DCC utilisé, les messages contiennent 3 mots.

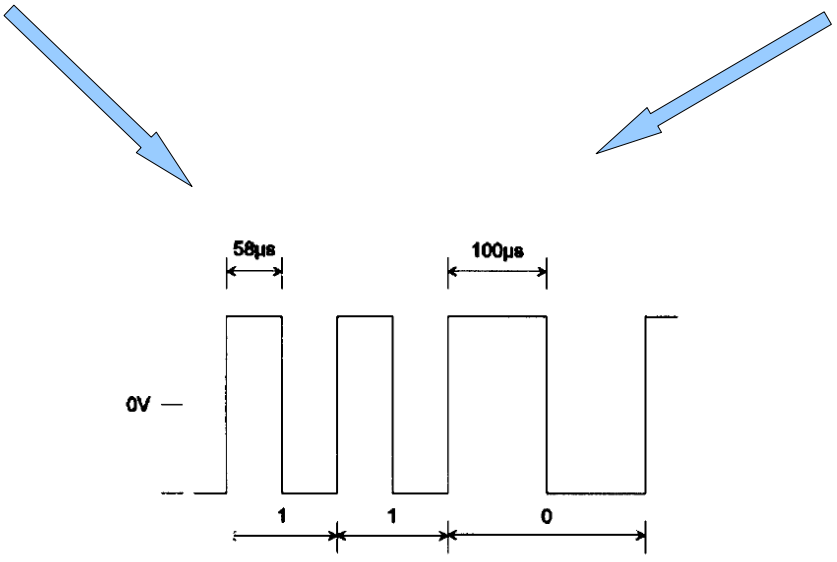


Codage d'un bit :

Dans le protocole DCC, chaque bit transmis est représenté par deux paliers successifs de polarité opposée.

Deux paliers ayant chacun une durée de 58 microsecondes forment un bit de valeur 1.

Deux paliers de durée supérieure ou égale à 100 microsecondes forment un bit de valeur O.



Enchaînement des trames

1 au moins 10 bits successifs à 1

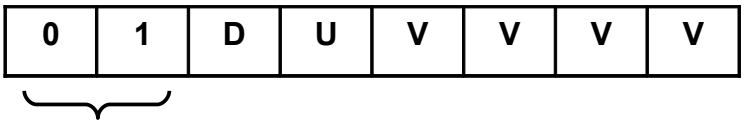
Une trame complète démarrant par un préambule (au moins 10 bits successifs à 1), elles peuvent être envoyées en continue.

L'octet d'adresse :

L'octet d'adresse permet au contrôleur d'indiquer le numéro du décodeur à qui est destiné le message. L'octet d'adresse étant formé de 8 bits, 256 adresses sont utilisables. L'adresse d'usine de tous les décodeurs est configurée à **0x03**.

L'octet de donnée :

Cet octet décrit au décodeur ce que l'on attend de lui.

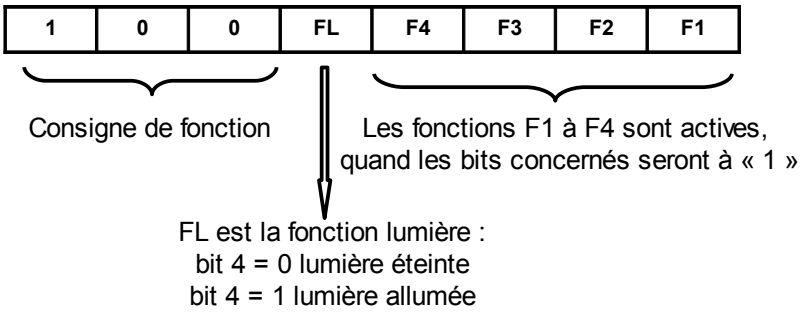


Les bits 7 et 6 informent le décodeur qu'il s'agit d'une consigne de vitesse, le bit 5 donnant le sens de circulation.

Information vitesse : bit 5 = 0, marche arrière
bit 5 = 1, marche avant

bit 7 =1 et bit 6 et 5 = 0, c'est une consigne de fonction :

Bit 7	Bit 6	Bit 5
0	1	**0**
0	1	**1**
1	**0**	**0**



L'octet de contrôle :

L'octet de contrôle est calculé comme étant le "ou exclusif" des deux précédents codes émis (l'adresse et la donnée) bit par bit. Lorsqu'un décodeur reçoit une trame, il refait le même calcul et compare son résultat au code de contrôle reçu. Si le résultat est identique, la trame reçue est bonne, le décodeur exécute l'ordre. S'il y a erreur le décodeur rejette la trame, et l'ordre n'est pas exécuté.

Ce système permet de détecter des erreurs avec une fiabilité supérieur à 99,5%.

3 La programmation

3.1 Algorithmes de la gare automatisée

Le programme de la gare automatisée comporte **2 phases** :

- ✓ Une phase d'initialisation qui permet de lire l'heure sur le module **DCF-77**.
- ✓ Une phase de gestion de l'heure et du signal de départ automatique qui fonctionne par une interruption Timer toutes les **250 µs**.

La phase d'initialisation :

Variable Heure

Variable Minute

Variable Trame[60]

DEBUT

- Initialisation des registres du microcontrôleur
- **TANT QUE** (bit de synchronisation non trouvé) **FAIRE**
    - Gérer l'affichage (défilement des chiffres)

  FIN TANT QUE
- **TANT QUE** (59ième bit non lu) **FAIRE**
    - Lire le bit
    - **SI** (bit lu = 1) **ALORS**
        - Bit Trame correspondant = 1

      SINON
        - Bit Trame correspondant = 0

      FIN SI
    - Gérer l'affichage (clignotement des chiffres)

  FIN TANT QUE
- Lecture de la Trame et récupération des minutes en DCB
- Lecture de la Trame et récupération de l'heure en DCB
- Synchronisation des secondes
- Passage de l'heure en Hexadécimal
- Passage des minutes en Hexadécimal
- Autoriser les interruptions (Timer)
- **TANT QUE** (toujours) **FAIRE**
    - Convertir l'heure en DCB et afficher.
    - Convertir les minutes en DCB et afficher.

  FIN TANT QUE

FIN

La phase de gestion de l'heure : (Timer toute les 250 µs)

Variable Compteur

Variables Heure, Minute, Seconde

DEBUT

- Incrémentation du Compteur
- **SI** (Compteur = 4000 (1 seconde)) **ALORS**
  - Incrémenter Secondes
  - **SI** (Seconde >= 60) **ALORS**
    - **SI** (mode départ automatique) **ALORS**
      - Lancer début du signal départ automatique

      FIN SI
    - Seconde = 0
    - Incrémentation Minute
    - **SI** (Minute >= 60) **ALORS**
      - Minute = 0
      - Incrémenter Heure
      - **SI** (Heure >= 24) **ALORS**
        - Heure = 0Bit Trame correspondant = 1

        FIN SI

      FIN SI

    FIN SI
  - Compteur = 0
  - **SI** (Seconde = 6) **ALORS**
    - Fin du signal départ automatique

    FIN SI

FIN SI

FIN

3.2 Algorithmes du train automatisé

Le programme du train automatisé comporte 2 **phases** :

- ✓ Une phase d'initialisation qui permet d'initialiser les récepteurs (trains ou autres) et qui ensuite commande un train à l'adresse 3 en fonction de deux bits de consignes (vitesse rapide, vitesse lente ou arrêt). Cette phase ne fait que programmer une trame dans la mémoire du microcontrôleur.
- ✓ Une phase d'envoi de la trame en mémoire sur la sortie du Microcontrôleur par l'intermédiaire d'un Timer.

La phase d'initialisation :

Variable Adresse

Variable Donnée

Variable Trame[40 x Nombre de récepteurs désiré]

DEBUT

- Initialisation des registres du microcontrôleur
- Initialisation par des 1 de la Trame en mémoire
- Initialisation de tous les récepteurs (Trame en mémoire)
- Autorisation des Interruptions (Timer)
- Attente de 5 ms (permet envoi de la Trame par l'interruption Timer)
- Initialisation Adresse à 3
- Initialisation Donnée sur vitesse lente
- **REPETER**
    - Remplir Trame en mémoire (adresse et donnée)
    - Attente de 5 ms (permet envoi de la Trame par l'interruption Timer)
    - **SI** (Vitesse rapide) **ALORS**
        - Donnée = Vitesse rapide

      FIN SI
    - **SI** (Vitesse lente) **ALORS**
        - Donnée = Vitesse lente

      FIN SI
    - **SI** (Arrêt Train) **ALORS**
        - Donnée = Arrêt Train

      FIN SI

  TANT QUE (Toujours)

FIN

La phase d'envoi de la Trame : (Timer)

Variable Compteur

Variable Trame[40 x Nombre de récepteurs désiré]

DEBUT

- **SI** (Compteur = 0) **ALORS**
  - Synchronisation front montant pour début de Trame

  FIN SI
- Incrémentation du compteur
- **SI** (Valeur Trame pointée par (compteur-1)/2 = 0) **ALORS**
  - Emission d'un zéro

  SINON
  - Emission d'un un

  FIN SI
- **SI** (Compteur = 2x 40 x Nombre de récepteurs désiré) **ALORS**
  - Compteur = 0

  FIN SI

FIN

3.3 Algorithmes de la souris

Le programme de la souris comporte 5 phases :

- ✓ Une phase d'initialisation qui permet d'initialiser les récepteurs (trains ou autre) et qui permet l'affichage des informations (Adresse décodeur et validation).
- ✓ Une phase d'envoi de la trame en mémoire sur la sortie du Microcontrôleur par l'intermédiaire d'un Timer.
- ✓ Une phase de gestion de la validation d'envoi d'une Trame, par l'intermédiaire de l'interruption INT2.
- ✓ Une phase de sélection des touches haut, bas, lumière et Arrêt d'urgence, par l'intermédiaire de l'interruption INT1.
- ✓ Une phase de sélection des touches de fonctions F1 à F4, par l'intermédiaire de l'interruption INT0.

La phase d'initialisation :

Variable Adresse

Variable Donnée

Variable Trame[40 x Nombre de récepteurs désiré]

DEBUT

- Initialisation des registres du microcontrôleur
- Initialisation par des 1 de la Trame en mémoire
- Initialisation de tous les récepteurs (Trame en mémoire)
- Autorisation des Interruptions (Timer)
- Attente de 5 ms (permet envoi de la Trame par l'interruption Timer)
- Initialisation Adresse à 3 par défaut
- Initialisation Donnée à 0 par défaut
- **REPETER**
  - Affichage de l'adresse du décodeur
  - **SI** (Modification adresse décodeur) **ALORS**
    - **SI** (premier passage) **ALORS**
      - Initialisation de la Trame en mémoire (IDLE)

      FIN SI
    - Remplissage de la trame en mémoire
    - **SI** (modification lumière train) ALORS
      - Gestion de la lumière (passage mode fonction)

      FIN SI

    FIN SI
  - Gestion affichage point de validation

TANT QUE (Toujours)

FIN

La phase Timer :

Variable Compteur
Variable Trame[40 x Nombre de récepteurs désiré]

DEBUT

- **SI** (Compteur = 0) **ALORS**
  - Synchronisation front montant pour début de Trame

  FIN SI
- Incrémentation du compteur
- **SI** (Valeur Trame pointée par (compteur-1)/2 = 0) ALORS
  - Émission d'un zéro

  SINON
  - Émission d'un un

  FIN SI
- **SI** (Compteur = 2x 40 x Nombre de récepteurs désiré) ALORS
  - Compteur = 0

  FIN SI

FIN

La phase interruption INT2 :

DEBUT

- Attendre 10 ms
- Passage en mode Loco
- Acquisition de la vitesse
- Validation modification Trame en mémoire
- Attendre 400 ms

FIN

La phase interruption INT1 :

DEBUT

- Attendre 10 ms
- **SI** (Appui sur touche Haut) **ALORS**
  - Sauvegarde donnée pour adresse précédente
  - **SI** (Adresse = Adresse Maximum) **ALORS**
    - Adresse = 1

    SINON
    - Incrémenter Adresse

    FIN SI
  - Restauration de la donnée pour la nouvelle adresse

  FIN SI
- **SI** (Appui sur touche Bas) **ALORS**
  - Sauvegarde donnée pour adresse précédente
  - **SI** (Adresse = 1) **ALORS**
    - Adresse = Adresse Maximum

    SINON
    - Décrémenter Adresse

    FIN SI
  - Restauration de la donnée pour la nouvelle adresse

  FIN SI
- **SI** (Appui sur touche Lumière) **ALORS**
  - Passage en mode fonction
  - **SI** (lumière éteinte) **ALORS**
    - Allumer lumière

    SINON
    - Éteindre lumière

    FIN SI
  - Restauration de la donnée pour la nouvelle adresse

  FIN SI
- **SI** (Appui sur touche Arrêt d'urgence) **ALORS**
  - **SI** (Arrêt d'urgence activé) **ALORS**
    - Désactiver Arrêt d'urgence

    SINON
    - Activer Arrêt d'urgence

    FIN SI

  FIN SI
- Attendre 400 ms

FIN

La phase interruption INT0 :

DEBUT

- Attendre 10 ms
- Passage en mode fonction
- **SI** (Appui sur touche F1) **ALORS**
    - **SI** (Fonction activée) **ALORS**
        - Désactiver la fonction

      SINON
        - Activer la fonction

      FIN SI

  FIN SI
- **SI** (Appui sur touche F2) **ALORS**
    - **SI** (Fonction activée) **ALORS**
        - Désactiver la fonction

      SINON
        - Activer la fonction

      FIN SI

  FIN SI
- **SI** (Appui sur touche F3) **ALORS**
    - **SI** (Fonction activée) **ALORS**
        - Désactiver la fonction

      SINON
        - Activer la fonction

      FIN SI

  FIN SI
- **SI** (Appui sur touche F4) **ALORS**
    - **SI** (Fonction activée) **ALORS**
        - Désactiver la fonction

      SINON
        - Activer la fonction

      FIN SI

  FIN SI
- Attendre 400 ms

FIN

4 Affectation des ports de l'ATMEL

4.1 ATMEL de OT1

Fonction principale FP1 :

Port	Sens	Affectation
PA[0..7]	Sortie	AF[0..7]
PC[0..7]	Sortie	AF[8..15]
PB6	Entrée	A/M
PB7	Sortie	DEP_M
PD2	Entrée	DCF-77

4.1 ATMEL de OT2

Fonction principale FP6 :

Port	Sens	Affectation
PB0	Entrée	ORD0
PB1	Entrée	ORD1
PB3	Sortie	TRAME

4.1 ATMEL de OT5

Fonction principale FP6 :

Port	Sens	Affectation
PA[0..4]	Entrée	Sélection du sens et de la vitesse
PC[0..7]	Sortie	Affichage numéro du décodeur
PD4	Entrée	Arrêt urgence
PD5	Entrée	Lumière
PD6	Entrée	Bas
PD7	Entrée	Haut

Port	Sens	Affectation
PB0	Sortie	Arrêt urgence
PB1	Sortie	LED
PB2	Entrée	Validation
PB3	Sortie	TRAME
PB4	Entrée	F1
PB5	Entrée	F2
PB6	Entrée	F3
PB7	Entrée	F4

Webographie

Fournisseurs :

http://www.jura-modelisme.fr/
http://www.conrad.fr/coffrets_de_depart_et_voies_c_19379_19464_26703

Des normes :

http://normes.rieger.de.com/

Des infos

http://fr.wikipedia.org/wiki/DCF77

divers :

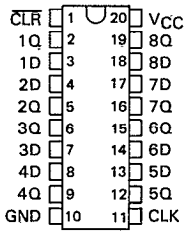
http://www.espacetrain.com/
http://www.espacerails.com/
http://www.letrainpassion.com/

SN74ALS273, SN54ALS273
OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

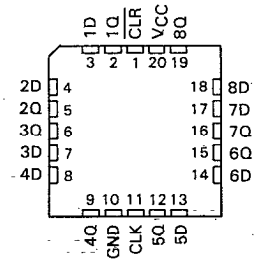
D2661, APRIL 1982 – REVISED MAY 1986

- Contains Eight Flip-Flops with Single-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-FLop
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS273 . . . J PACKAGE
SN74ALS273 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS273 . . . FK PACKAGE
(TOP VIEW)



description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input.

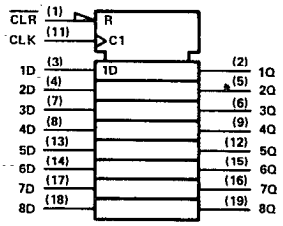
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

The SN54ALS273 is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74ALS273 is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

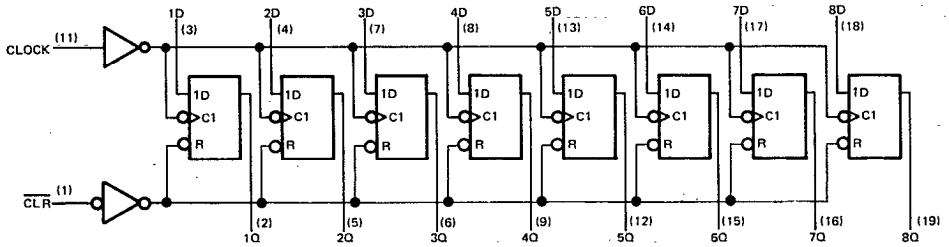
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

TEXAS INSTRUMENTS

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS273 . . . . . −55 °C to 125 °C
SN74ALS273 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS273			SN74ALS273			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		30	0		35	MHz
t_w	Pulse duration	$\overline{CLR}$ low	10			10			ns
		CLK high	16.5			14			
		CLK low	16.5			14			
t_{su}	Setup time before CLK↑	Data	10			10			ns
		Clear inactive state	15			15			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS273			SN74ALS273			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V			11	20		11	20	mA
I_{CCL}	V_{CC} = 5.5 V			19	29		19	29	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS273		SN74ALS273		
			MIN	MAX	MIN	MAX	
f_{max}			30		35		MHz
t_{PHL}	$\overline{CLR}$	Any Q	4	24	4	18	ns
t_{PLH}	CLK	Any Q	2	20	2	12	ns
t_{PHL}			3	17	3	15	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

National Semiconductor

June 1989

54LS00/DM54LS00/DM74LS00 Quad 2-Input NAND Gates

General Description

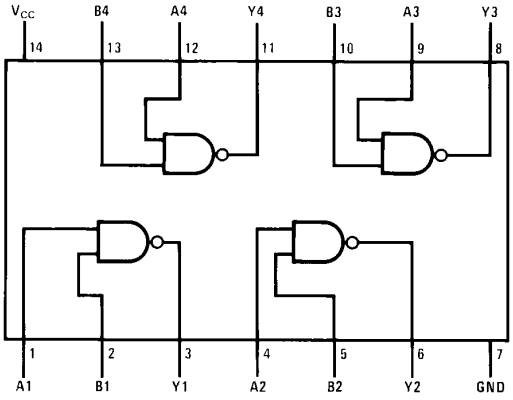
This device contains four independent gates each of which performs the logic NAND function.

Features

- Alternate Military/Aerospace device (54LS00) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6439–1

Order Number 54LS00DMQB, 54LS00FMQB, 54LS00LMQB, DM54LS00J, DM54LS00W, DM74LS00M or DM74LS00N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS00			DM74LS00			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.8	1.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			2.4	4.4	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	10	4	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

February 1995

LMD18200 3A, 55V H-Bridge

General Description

The LMD18200 is a 3A H-Bridge designed for motion control applications. The device is built using a multi-technology process which combines bipolar and CMOS control circuitry with DMOS power devices on the same monolithic structure. Ideal for driving DC and stepper motors; the LMD18200 accommodates peak output currents up to 6A. An innovative circuit which facilitates low-loss sensing of the output current has been implemented.

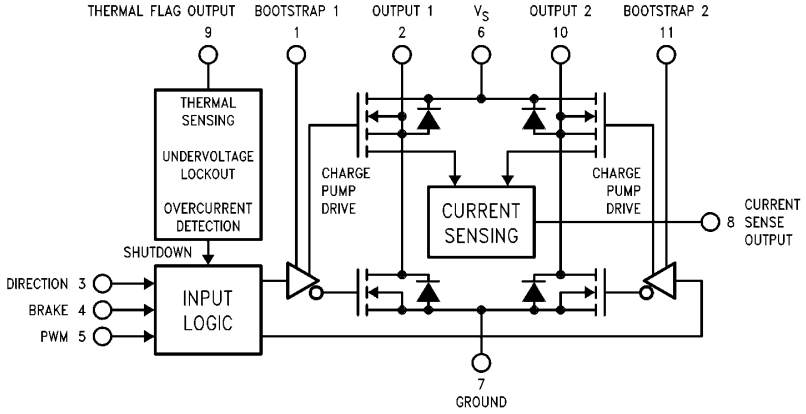
Features

- Delivers up to 3A continuous output
- Operates at supply voltages up to 55V
- Low $R_{DS}(ON)$ typically 0.3Ω per switch
- TTL and CMOS compatible inputs
- No "shoot-through" current
- Thermal warning flag output at 145°C
- Thermal shutdown (outputs off) at 170°C
- Internal clamp diodes
- Shorted load protection
- Internal charge pump with external bootstrap capability

Applications

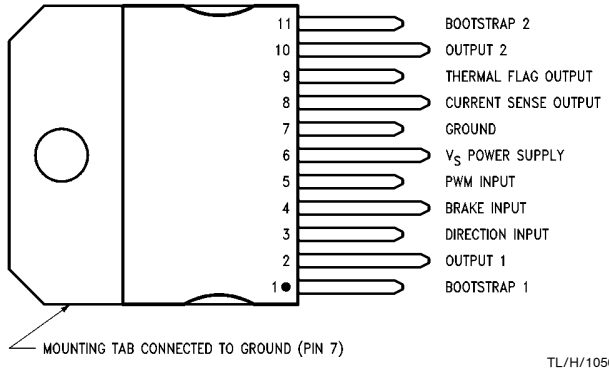
- DC and stepper motor drives
- Position and velocity servomechanisms
- Factory automation robots
- Numerically controlled machinery
- Computer printers and plotters

Functional Diagram



TL/H/10568–1

Connection Diagram and Ordering Information



TL/H/10568–2

Top View

Order Number LMD18200T
See NS Package TA11B

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Supply Voltage (V_S, Pin 6)	60V
Voltage at Pins 3, 4, 5, 8 and 9	12V
Voltage at Bootstrap Pins (Pins 1 and 11)	V_{OUT} + 16V
Peak Output Current (200 ms)	6A
Continuous Output Current (Note 2)	3A
Power Dissipation (Note 3)	25W
Power Dissipation (T_A = 25°C, Free Air)	3W
Junction Temperature, $T_{J(max)}$	150°C
ESD Susceptibility (Note 4)	1500V
Storage Temperature, T_{STG}	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Ratings (Note 1)

Junction Temperature, T_J	−40°C to +125°C
V_S Supply Voltage	+12V to +55V

Electrical Characteristics

The following specifications apply for V_S = 42V, unless otherwise specified. **Boldface** limits apply over the entire operating temperature range, −40°C ≤ T_J ≤ +125°C, all other limits are for T_A = T_J = 25°C. (Note 5)

Symbol	Parameter	Conditions	Typ	Limit	Units
R_{DS}(ON)	Switch ON Resistance	Output Current = 3A (Note 6)	0.33	0.4/**0.6**	Ω (max)
R_{DS}(ON)	Switch ON Resistance	Output Current = 6A (Note 6)	0.33	0.4/**0.6**	Ω (max)
V_{CLAMP}	Clamp Diode Forward Drop	Clamp Current = 3A (Note 6)	1.2	1.5	V (max)
V_{IL}	Logic Low Input Voltage	Pins 3, 4, 5		**−0.1** **0.8**	V (min) V (max)
I_{IL}	Logic Low Input Current	V_{IN} = −0.1V, Pins = 3, 4, 5		**−10**	μA (max)
V_{IH}	Logic High Input Voltage	Pins 3, 4, 5		**2** **12**	V (min) V (max)
I_{IH}	Logic High Input Current	V_{IN} = 12V, Pins = 3, 4, 5		**10**	μA (max)
	Current Sense Output	I_{OUT} = 1A (Note 8)	377	325/**300** 425/**450**	μA (min) μA (max)
	Current Sense Linearity	1A ≤ I_{OUT} ≤ 3A (Note 7)	±6	±9	%
	Undervoltage Lockout	Outputs turn OFF		9 11	V (min) V (max)
T_{JW}	Warning Flag Temperature	Pin 9 ≤ 0.8V, I_L = 2 mA	145		°C
V_F(ON)	Flag Output Saturation Voltage	T_J = T_{JW}, I_L = 2 mA	0.15		V
I_F(OFF)	Flag Output Leakage	V_F = 12V	0.2	10	μA (max)
T_{JSD}	Shutdown Temperature	Outputs Turn OFF	170		°C
I_S	Quiescent Supply Current	All Logic Inputs Low	13	25	mA (max)
t_{Don}	Output Turn-On Delay Time	Sourcing Outputs, I_{OUT} = 3A Sinking Outputs, I_{OUT} = 3A	300 300		ns ns
t_{on}	Output Turn-On Switching Time	Bootstrap Capacitor = 10 nF Sourcing Outputs, I_{OUT} = 3A Sinking Outputs, I_{OUT} = 3A	 100 80		 ns ns
t_{Doff}	Output Turn-Off Delay Times	Sourcing Outputs, I_{OUT} = 3A Sinking Outputs, I_{OUT} = 3A	200 200		ns ns
t_{off}	Output Turn-Off Switching Times	Bootstrap Capacitor = 10 nF Sourcing Outputs, I_{OUT} = 3A Sinking Outputs, I_{OUT} = 3A	 75 70		 ns ns
t_{pw}	Minimum Input Pulse Width	Pins 3, 4 and 5	1		μs
t_{cpr}	Charge Pump Rise Time	No Bootstrap Capacitor	20		μs

Electrical Characteristics Notes

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: See Application Information for details regarding current limiting.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any temperature is $P_{D(max)} = (T_{J(max)} - T_A)/\theta_{JA}$, or the number given in the Absolute Ratings, whichever is lower. The typical thermal resistance from junction to case (θ_{JC}) is 1.0°C/W and from junction to ambient (θ_{JA}) is 30°C/W. For guaranteed operation $T_{J(max)} = 125$°C.

Note 4: Human-body model, 100 pF discharged through a 1.5 kΩ resistor. Except Bootstrap pins (pins 1 and 11) which are protected to 1000V of ESD.

Note 5: All limits are 100% production tested at 25°C. Temperature extreme limits are guaranteed via correlation using accepted SQC (Statistical Quality Control) methods. All limits are used to calculate AOQL, (Average Outgoing Quality Level).

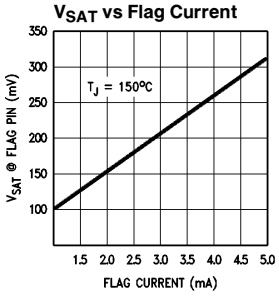
Note 6: Output currents are pulsed ($t_W < 2$ ms, Duty Cycle $< 5\%$).

Note 7: Regulation is calculated relative to the current sense output value with a 1A load.

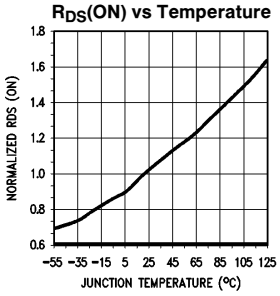
Note 8: Selections for tighter tolerance are available. Contact factory.

Typical Performance Characteristics

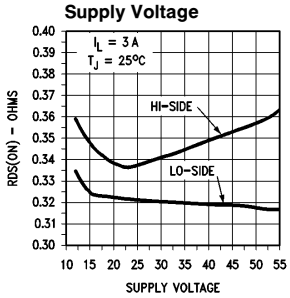
V_{SAT} vs Flag Current



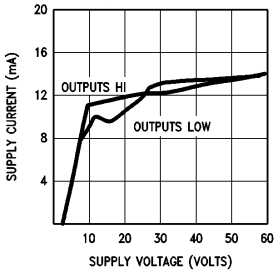
R_{DS}(ON) vs Temperature



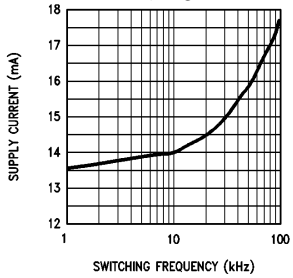
R_{DS}(ON) vs Supply Voltage



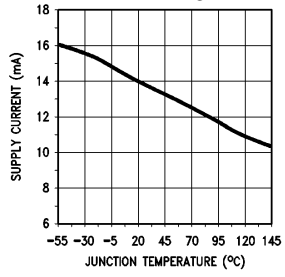
Supply Current vs Supply Voltage



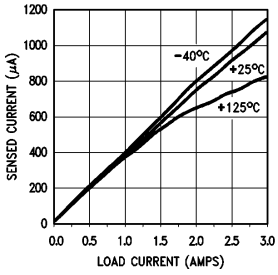
Supply Current vs Frequency (V_S = 42V)



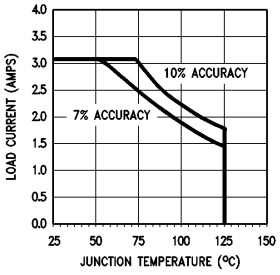
Supply Current vs Temperature (V_S = 42V)



Current Sense Output vs Load Current



Current Sense Operating Region



TL/H/10568–3

Pinout Description (See Connection Diagram)

Pin 1, BOOTSTRAP 1 Input: Bootstrap capacitor pin for half H-bridge number 1. The recommended capacitor (10 nF) is connected between pins 1 and 2.

Pin 2, OUTPUT 1: Half H-bridge number 1 output.

Pin 3, DIRECTION Input: See Table I. This input controls the direction of current flow between OUTPUT 1 and OUTPUT 2 (pins 2 and 10) and, therefore, the direction of rotation of a motor load.

Pin 4, BRAKE Input: See Table I. This input is used to brake a motor by effectively shorting its terminals. When braking is desired, this input is taken to a logic high level and it is also necessary to apply logic high to PWM input, pin 5. The drivers that short the motor are determined by the logic level at the DIRECTION input (Pin 3): with Pin 3 logic high, both current sourcing output transistors are ON; with Pin 3 logic low, both current sinking output transistors are ON. All output transistors can be turned OFF by applying a logic high to Pin 4 and a logic low to PWM input Pin 5; in this case only a small bias current (approximately −1.5 mA) exists at each output pin.

Pin 5, PWM Input: See Table I. How this input (and DIRECTION input, Pin 3) is used is determined by the format of the PWM Signal.

Pin 6, V_S Power Supply

Pin 7, GROUND Connection: This pin is the ground return, and is internally connected to the mounting tab.

Pin 8, CURRENT SENSE Output: This pin provides the sourcing current sensing output signal, which is typically 377 μA/A.

Pin 9, THERMAL FLAG Output: This pin provides the thermal warning flag output signal. Pin 9 becomes active-low at 145°C (junction temperature). However the chip will not shut itself down until 170°C is reached at the junction.

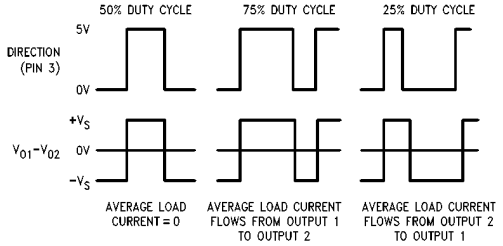
Pin 10, OUTPUT 2: Half H-bridge number 2 output.

Pin 11, BOOTSTRAP 2 Input: Bootstrap capacitor pin for Half H-bridge number 2. The recommended capacitor (10 nF) is connected between pins 10 and 11.

TABLE I. Logic Truth Table

PWM	Dir	Brake	Active Output Drivers
H	H	L	Source 1, Sink 2
H	L	L	Sink 1, Source 2
L	X	L	Source 1, Source 2
H	H	H	Source 1, Source 2
H	L	H	Sink 1, Sink 2
L	X	H	NONE

Locked Anti-Phase PWM Control



TL/H/10568–4

Application Information

TYPES OF PWM SIGNALS

The LMD18200 readily interfaces with different forms of PWM signals. Use of the part with two of the more popular forms of PWM is described in the following paragraphs.

Simple, locked anti-phase PWM consists of a single, variable duty-cycle signal in which is encoded both direction and amplitude information. A 50% duty-cycle PWM signal represents zero drive, since the net value of voltage (integrated over one period) delivered to the load is zero. For the LMD18200, the PWM signal drives the direction input (pin 3) and the PWM input (pin 5) is tied to logic high.

Sign/magnitude PWM consists of separate direction (sign) and amplitude (magnitude) signals. The (absolute) magnitude signal is duty-cycle modulated, and the absence of a pulse signal (a continuous logic low level) represents zero drive. Current delivered to the load is proportional to pulse width. For the LMD18200, the DIRECTION input (pin 3) is driven by the sign signal and the PWM input (pin 5) is driven by the magnitude signal.

USING THE CURRENT SENSE OUTPUT

The CURRENT SENSE output (pin 8) has a sensitivity of 377 μA per ampere of output current. For optimal accuracy and linearity of this signal, the value of voltage generating resistor between pin 8 and ground should be chosen to limit the maximum voltage developed at pin 8 to 5V, or less. The maximum voltage compliance is 12V.

It should be noted that the recirculating currents (free wheeling currents) are ignored by the current sense circuitry. Therefore, only the currents in the upper sourcing outputs are sensed.

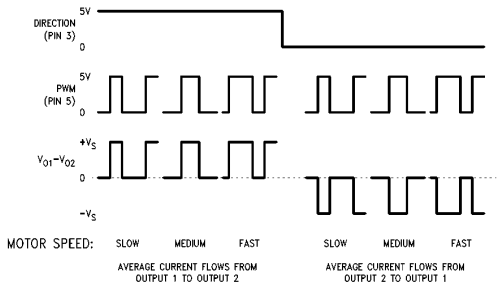
USING THE THERMAL WARNING FLAG

The THERMAL FLAG output (pin 9) is an open collector transistor. This permits a wired OR connection of thermal warning flag outputs from multiple LMD18200's, and allows the user to set the logic high level of the output signal swing to match system requirements. This output typically drives the interrupt input of a system controller. The interrupt service routine would then be designed to take appropriate steps, such as reducing load currents or initiating an orderly system shutdown. The maximum voltage compliance on the flag pin is 12V.

SUPPLY BYPASSING

During switching transitions the levels of fast current changes experienced may cause troublesome voltage transients across system stray inductance.

Sign/Magnitude PWM Control



TL/H/10568–5

Application Information (Continued)

It is normally necessary to bypass the supply rail with a high quality capacitor(s) connected as close as possible to the V_S Power Supply (Pin 6) and GROUND (Pin 7). A 1 μF high-frequency ceramic capacitor is recommended. Care should be taken to limit the transients on the supply pin below the Absolute Maximum Rating of the device. When operating the chip at supply voltages above 40V a voltage suppressor (transorb) such as P6KE62A is recommended from supply to ground. Typically the ceramic capacitor can be eliminated in the presence of the voltage suppressor. Note that when driving high load currents a greater amount of supply bypass capacitance (in general at least 100 μF per Amp of load current) is required to absorb the recirculating currents of the inductive loads.

CURRENT LIMITING

Current limiting protection circuitry has been incorporated into the design of the LMD18200. With any power device it is important to consider the effects of the substantial surge currents through the device that may occur as a result of shorted loads. The protection circuitry monitors this increase in current (the threshold is set to approximately 10 Amps) and shuts off the power device as quickly as possible in the event of an overload condition. In a typical motor driving application the most common overload faults are caused by shorted motor windings and locked rotors. Under these conditions the inductance of the motor (as well as any series inductance in the V_{CC} supply line) serves to reduce the magnitude of a current surge to a safe level for the LMD18200. Once the device is shut down, the control circuitry will periodically try to turn the power device back on. This feature allows the immediate return to normal operation in the event that the fault condition has been removed. While the fault remains however, the device will cycle in and out of thermal shutdown. This can create voltage transients on the V_{CC} supply line and therefore proper supply bypassing techniques are required.

The most severe condition for any power device is a direct, hard-wired (''screwdriver'') long term short from an output to ground. This condition can generate a surge of current through the power device on the order of 15 Amps and require the die and package to dissipate up to 500 Watts of power for the short time required for the protection circuitry to shut off the power device. This energy can be destructive, particularly at higher operating voltages ($>$30V) so some precautions are in order. Proper heat sink design is essential and it is normally necessary to heat sink the V_{CC} supply pin (pin 6) with 1 square inch of copper on the PCB.

INTERNAL CHARGE PUMP AND USE OF BOOTSTRAP CAPACITORS

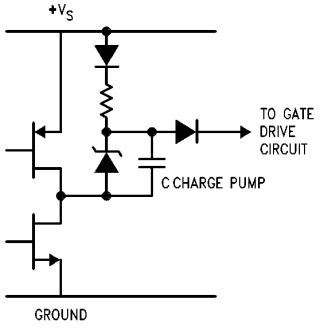
To turn on the high-side (sourcing) DMOS power devices, the gate of each device must be driven approximately 8V more positive than the supply voltage. To achieve this an internal charge pump is used to provide the gate drive voltage. As shown in *Figure 1*, an internal capacitor is alternately switched to ground and charged to about 14V, then switched to V supply thereby providing a gate drive voltage greater than V supply. This switching action is controlled by a continuously running internal 300 kHz oscillator. The rise time of this drive voltage is typically 20 μs which is suitable for operating frequencies up to 1 kHz.

For higher switching frequencies, the LMD18200 provides for the use of external bootstrap capacitors. The bootstrap principle is in essence a second charge pump whereby a large value capacitor is used which has enough energy to quickly charge the parasitic gate input capacitance of the power device resulting in much faster rise times. The switching action is accomplished by the power switches themselves *(Figure 2)*. External 10 nF capacitors, connected from the outputs to the bootstrap pins of each high-side switch provide typically less than 100 ns rise times allowing switching frequencies up to 500 kHz.

INTERNAL PROTECTION DIODES

A major consideration when switching current through inductive loads is protection of the switching power devices from the large voltage transients that occur. Each of the four switches in the LMD18200 have a built-in protection diode to clamp transient voltages exceeding the positive supply or ground to a safe diode voltage drop across the switch.

The reverse recovery characteristics of these diodes, once the transient has subsided, is important. These diodes must come out of conduction quickly and the power switches must be able to conduct the additional reverse recovery current of the diodes. The reverse recovery time of the diodes protecting the sourcing power devices is typically only 70 ns with a reverse recovery current of 1A when tested with a full 6A of forward current through the diode. For the sinking devices the recovery time is typically 100 ns with 4A of reverse current under the same conditions.



TL/H/10568–6

FIGURE 1. Internal Charge Pump Circuitry

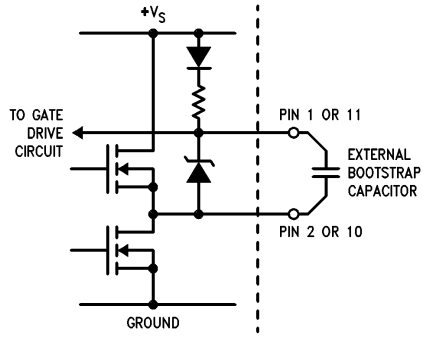


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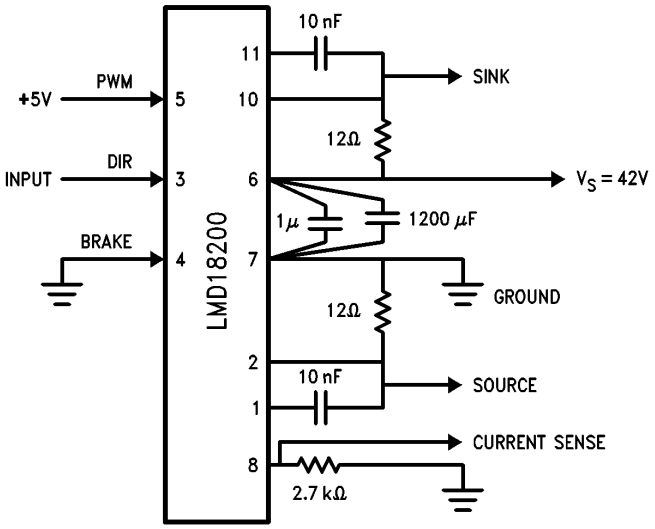
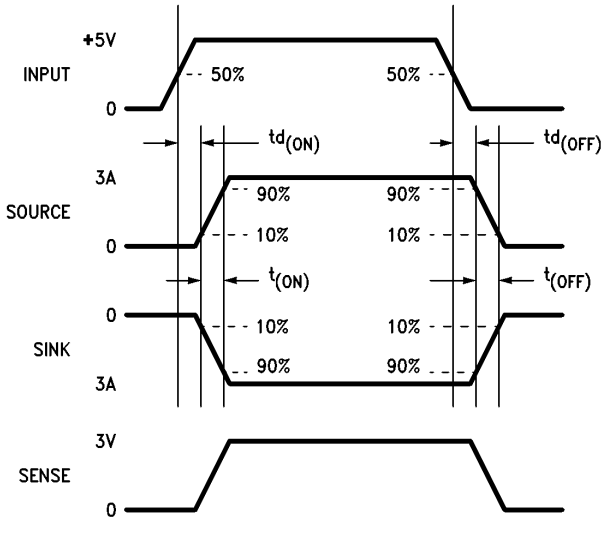
FIGURE 2. Bootstrap Circuitry

Test Circuit



TL/H/10568–8

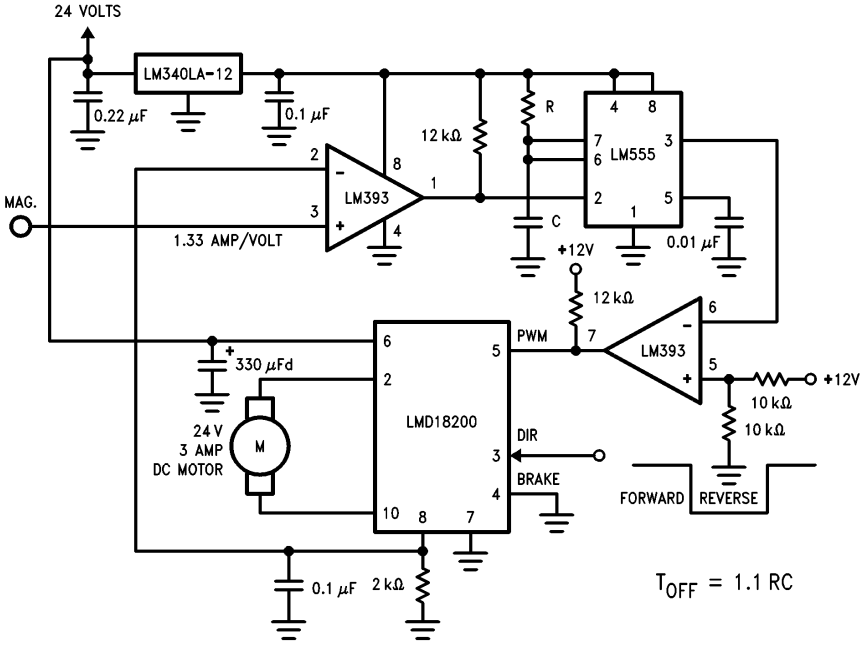
Switching Time Definitions



TL/H/10568–9

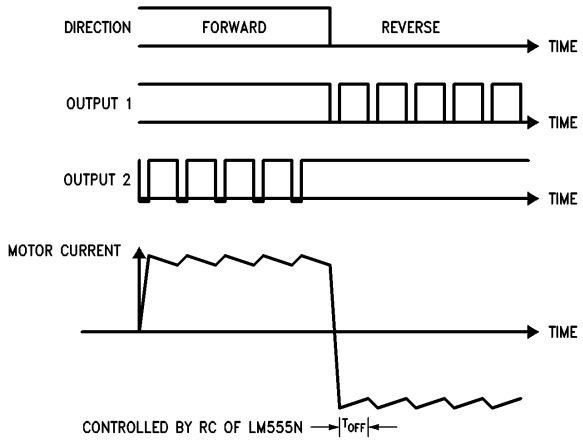
Typical Applications

Fixed Off-Time Control: This circuit controls the current through the motor by applying an average voltage equal to zero to the motor terminals for a fixed period of time, whenever the current through the motor exceeds the commanded current. This action causes the motor current to vary slightly about an externally controlled average level. The duration of the Off-period is adjusted by the resistor and capacitor combination of the LM555. In this circuit the Sign/Magnitude mode of operation is implemented (see Types of PWM Signals).



TL/H/10568–10

Switching Waveforms

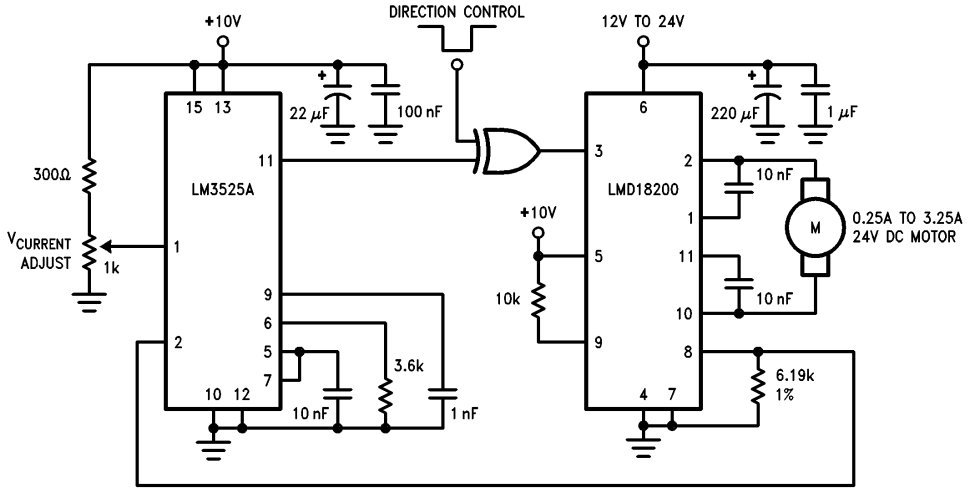


TL/H/10568–11

Typical Applications (Continued)

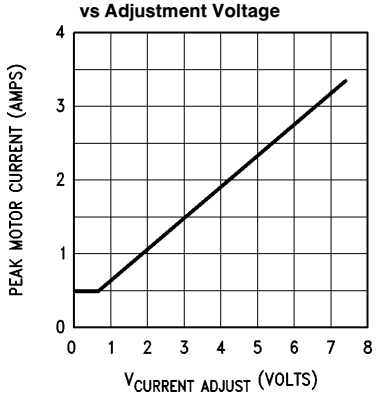
TORQUE REGULATION

Locked Anti-Phase Control of a brushed DC motor. Current sense output of the LMD18200 provides load sensing. The LM3525A is a general purpose PWM controller.



TL/H/10568–12

Peak Motor Current vs Adjustment Voltage

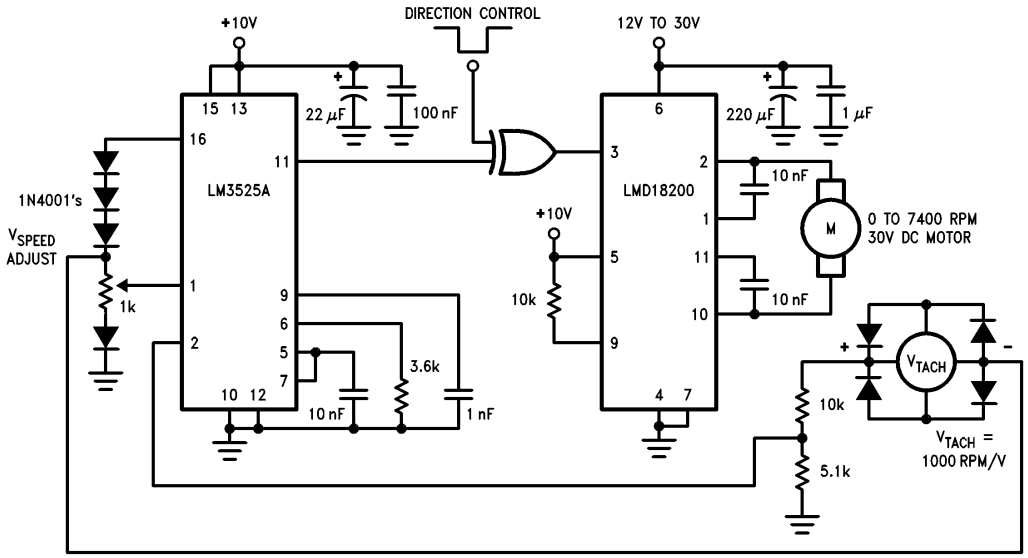


TL/H/10568–13

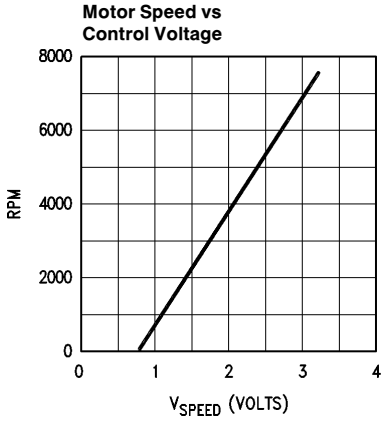
Typical Applications (Continued)

VELOCITY REGULATION

Utilizes tachometer output from the motor to sense motor speed for a locked anti-phase control loop.



TL/H/10568–14



TL/H/10568–15

National Semiconductor

February 1995

LM2907/LM2917 Frequency to Voltage Converter

General Description

The LM2907, LM2917 series are monolithic frequency to voltage converters with a high gain op amp/comparator designed to operate a relay, lamp, or other load when the input frequency reaches or exceeds a selected rate. The tachometer uses a charge pump technique and offers frequency doubling for low ripple, full input protection in two versions (LM2907-8, LM2917-8) and its output swings to ground for a zero frequency input.

Advantages

- Output swings to ground for zero frequency input
- Easy to use; $V_{OUT} = f_{IN} \times V_{CC} \times R1 \times C1$
- Only one RC network provides frequency doubling
- Zener regulator on chip allows accurate and stable frequency to voltage or current conversion (LM2917)

Features

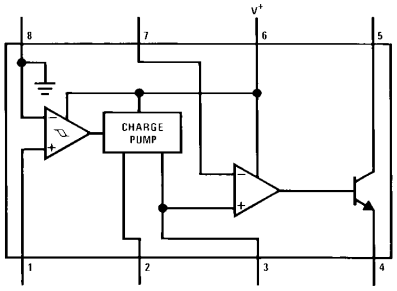
- Ground referenced tachometer input interfaces directly with variable reluctance magnetic pickups
- Op amp/comparator has floating transistor output
- 50 mA sink or source to operate relays, solenoids, meters, or LEDs
- Frequency doubling for low ripple
- Tachometer has built-in hysteresis with either differential input or ground referenced input
- Built-in zener on LM2917
- ±0.3% linearity typical
- Ground referenced tachometer is fully protected from damage due to swings above V_{CC} and below ground

Applications

- Over/under speed sensing
- Frequency to voltage conversion (tachometer)
- Speedometers
- Breaker point dwell meters
- Hand-held tachometer
- Speed governors
- Cruise control
- Automotive door lock control
- Clutch control
- Horn control
- Touch or sound switches

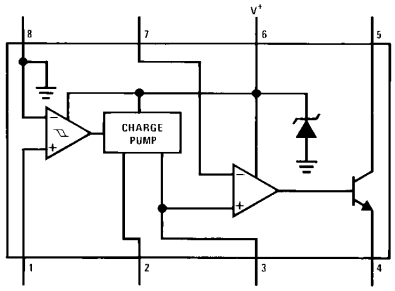
Block and Connection Diagrams

Dual-In-Line and Small Outline Packages, Top Views



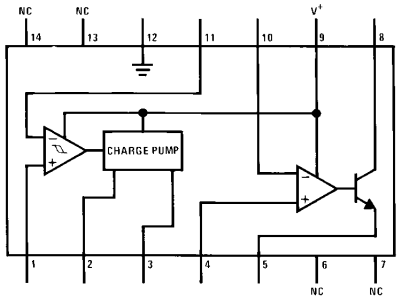
TL/H/7942–1

Order Number LM2907M-8 or LM2907N-8
See NS Package Number M08A or N08E



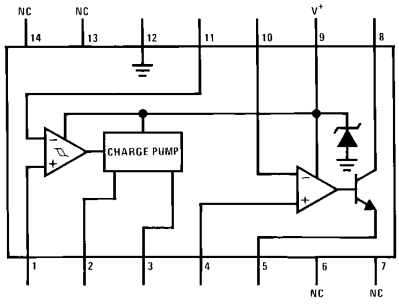
TL/H/7942–2

Order Number LM2917M-8 or LM2917N-8
See NS Package Number M08A or N08E



TL/H/7942–3

Order Number LM2907N
See NS Package Number N14A



TL/H/7942–4

Order Number LM2917M or LM2917N
See NS Package Number M14A or N14A

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	28V
Supply Current (Zener Options)	25 mA
Collector Voltage	28V
Differential Input Voltage	
Tachometer	28V
Op Amp/Comparator	28V
Input Voltage Range	
Tachometer LM2907-8, LM2917-8	±28V
LM2907, LM2917	0.0V to +28V
Op Amp/Comparator	0.0V to +28V
Power Dissipation	
LM2907-8, LM2917-8	1200 mW
LM2907-14, LM2917-14 (See Note 1)	1580 mW
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics V_{CC} = 12 V_{DC}, T_A = 25°C, see test circuit

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TACHOMETER						
	Input Thresholds	V_{IN} = 250 mVp-p @ 1 kHz (Note 2)	±10	±25	±40	mV
	Hysteresis	V_{IN} = 250 mVp-p @ 1 kHz (Note 2)		30		mV
	Offset Voltage	V_{IN} = 250 mVp-p @ 1 kHz (Note 2)				
	LM2907/LM2917			3.5	10	mV
	LM2907-8/LM2917-8			5	15	mV
	Input Bias Current	V_{IN} = ±50 mV_{DC}		0.1	1	μA
V_{OH}	Pin 2	V_{IN} = +125 mV_{DC} (Note 3)		8.3		V
V_{OL}	Pin 2	V_{IN} = −125 mV_{DC} (Note 3)		2.3		V
I_2, I_3	Output Current	V2 = V3 = 6.0V (Note 4)	140	180	240	μA
I_3	Leakage Current	I2 = 0, V3 = 0			0.1	μA
K	Gain Constant	(Note 3)	0.9	1.0	1.1	
	Linearity	f_{IN} = 1 kHz, 5 kHz, 10 kHz (Note 5)	−1.0	0.3	+1.0	%
OP/AMP COMPARATOR						
V_{OS}		V_{IN} = 6.0V		3	10	mV
I_{BIAS}		V_{IN} = 6.0V		50	500	nA
	Input Common-Mode Voltage		0		V_{CC}−1.5V	V
	Voltage Gain			200		V/mV
	Output Sink Current	V_C = 1.0	40	50		mA
	Output Source Current	V_E = V_{CC} −2.0		10		mA
	Saturation Voltage	I_{SINK} = 5 mA		0.1	0.5	V
		I_{SINK} = 20 mA			1.0	V
		I_{SINK} = 50 mA		1.0	1.5	V

Electrical Characteristics V_{CC} = 12 V_{DC}, T_A = 25°C, see test circuit (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ZENER REGULATOR						
	Regulator Voltage	R_{DROP} = 470Ω		7.56		V
	Series Resistance			10.5	15	Ω
	Temperature Stability			+1		mV/°C
	TOTAL SUPPLY CURRENT			3.8	6	mA

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 101°C/W junction to ambient for LM2907-8 and LM2917-8, and 79°C/W junction to ambient for LM2907-14 and LM2917-14.

Note 2: Hysteresis is the sum $+V_{TH} - (-V_{TH})$, offset voltage is their difference. See test circuit.

Note 3: V_{OH} is equal to ¾ × V_{CC} − 1 V_{BE}, V_{OL} is equal to ¼ × V_{CC} − 1 V_{BE} therefore $V_{OH} - V_{OL} = V_{CC}/2$. The difference, $V_{OH} - V_{OL}$, and the mirror gain, I_2/I_3, are the two factors that cause the tachometer gain constant to vary from 1.0.

Note 4: Be sure when choosing the time constant R1 × C1 that R1 is such that the maximum anticipated output voltage at pin 3 can be reached with I_3 × R1. The maximum value for R1 is limited by the output resistance of pin 3 which is greater than 10 MΩ typically.

Note 5: Nonlinearity is defined as the deviation of V_{OUT} (@ pin 3) for f_{IN} = 5 kHz from a straight line defined by the V_{OUT} @ 1 kHz and V_{OUT} @ 10 kHz. C1 = 1000 pF, R1 = 68k and C2 = 0.22 mFd.

General Description (Continued)

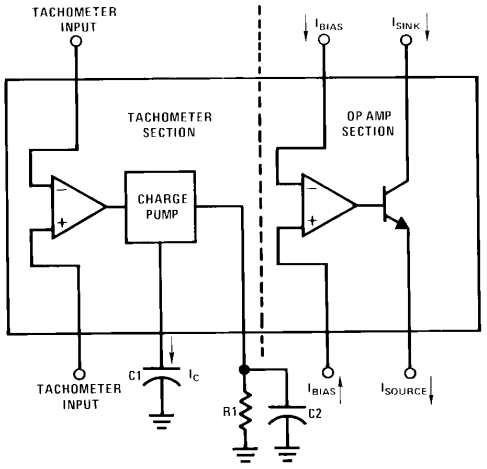
The op amp/comparator is fully compatible with the tachometer and has a floating transistor as its output. This feature allows either a ground or supply referred load of up to 50 mA. The collector may be taken above V_{CC} up to a maximum V_{CE} of 28V.

The two basic configurations offered include an 8-pin device with a *ground referenced tachometer* input and an internal connection between the tachometer output and the op amp non-inverting input. This version is well suited for single speed or frequency switching or fully buffered frequency to voltage conversion applications.

The more versatile configurations provide differential tachometer input and uncommitted op amp inputs. With this version the tachometer input may be floated and the op amp becomes suitable for active filter conditioning of the tachometer output.

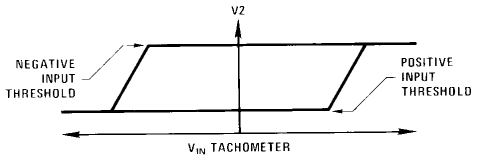
Both of these configurations are available with an active shunt regulator connected across the power leads. The regulator clamps the supply such that stable frequency to voltage and frequency to current operations are possible with any supply voltage and a suitable resistor.

Test Circuit and Waveform



TL/H/7942–6

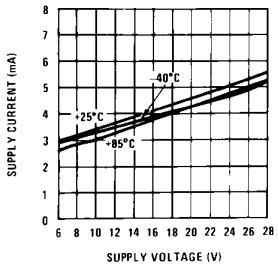
Tachometer Input Threshold Measurement



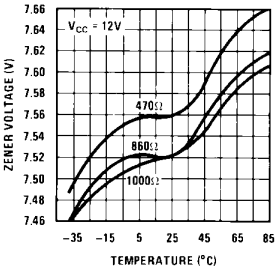
TL/H/7942–7

Typical Performance Characteristics

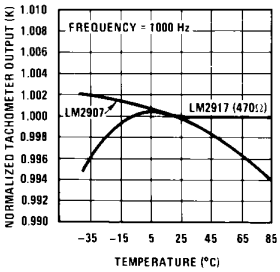
Total Supply Current



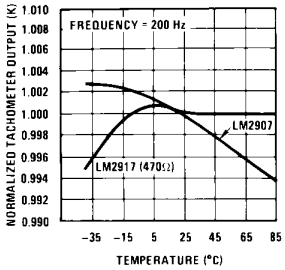
Zener Voltage vs Temperature



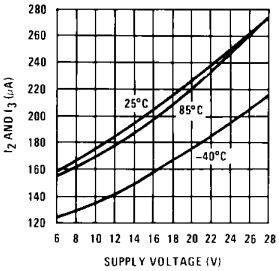
Normalized Tachometer Output vs Temperature



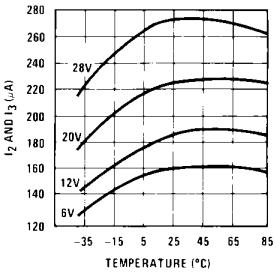
Normalized Tachometer Output vs Temperature



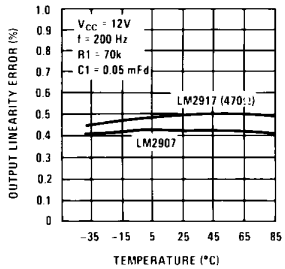
Tachometer Currents I_2 and I_3 vs Supply Voltage



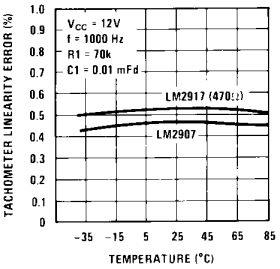
Tachometer Currents I_2 and I_3 vs Temperature



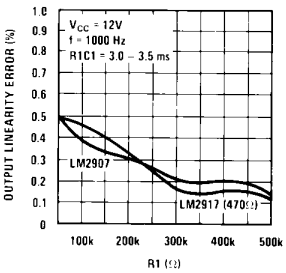
Tachometer Linearity vs Temperature



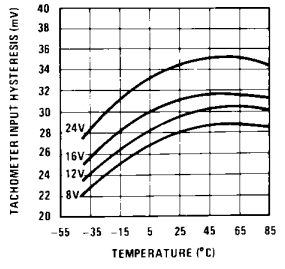
Tachometer Linearity vs Temperature



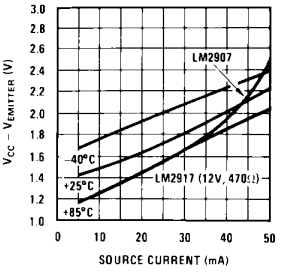
Tachometer Linearity vs R1



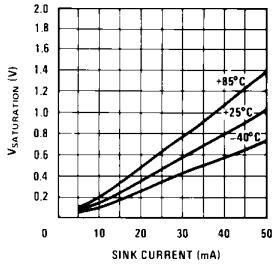
Tachometer Input Hysteresis vs Temperature



Op Amp Output Transistor Characteristics



Op Amp Output Transistor Characteristics



TL/H/7942–5

Applications Information

The LM2907 series of tachometer circuits is designed for minimum external part count applications and maximum versatility. In order to fully exploit its features and advantages let's examine its theory of operation. The first stage of operation is a differential amplifier driving a positive feedback flip-flop circuit. The input threshold voltage is the amount of differential input voltage at which the output of this stage changes state. Two options (LM2907-8, LM2917-8) have one input internally grounded so that an input signal must swing above and below ground and exceed the input thresholds to produce an output. This is offered specifically for magnetic variable reluctance pickups which typically provide a single-ended ac output. This single input is also fully protected against voltage swings to ± 28V, which are easily attained with these types of pickups.

The differential input options (LM2907, LM2917) give the user the option of setting his own input switching level and still have the hysteresis around that level for excellent noise rejection in any application. Of course in order to allow the inputs to attain common-mode voltages above ground, input protection is removed and neither input should be taken outside the limits of the supply voltage being used. It is very important that an input not go below ground without some resistance in its lead to limit the current that will then flow in the epi-substrate diode.

Following the input stage is the charge pump where the input frequency is converted to a dc voltage. To do this requires one timing capacitor, one output resistor, and an integrating or filter capacitor. When the input stage changes state (due to a suitable zero crossing or differential voltage on the input) the timing capacitor is either charged or discharged linearly between two voltages whose difference is $V_{CC}/2$. Then in one half cycle of the input frequency or a time equal to $1/2\ f_{IN}$ the change in charge on the timing capacitor is equal to $V_{CC}/2 \times C1$. The average amount of current pumped into or out of the capacitor then is:

$$\frac{\Delta Q}{T} = i_{c(AVG)} = C1 \times \frac{V_{CC}}{2} \times (2f_{IN}) = V_{CC} \times f_{IN} \times C1$$

The output circuit mirrors this current very accurately into the load resistor R1, connected to ground, such that if the pulses of current are integrated with a filter capacitor, then $V_O = i_c \times R1$, and the total conversion equation becomes:

$$V_O = V_{CC} \times f_{IN} \times C1 \times R1 \times K$$

Where K is the gain constant—typically 1.0.

The size of C2 is dependent only on the amount of ripple voltage allowable and the required response time.

CHOOSING R1 AND C1

There are some limitations on the choice of R1 and C1 which should be considered for optimum performance. The timing capacitor also provides internal compensation for the charge pump and should be kept larger than 500 pF for very accurate operation. Smaller values can cause an error current on R1, especially at low temperatures. Several considerations must be met when choosing R1. The output current at pin 3 is internally fixed and therefore $V_O/R1$ must be less than or equal to this value. If R1 is too large, it can become a significant fraction of the output impedance at pin 3 which degrades linearity. Also output ripple voltage must be considered and the size of C2 is affected by R1. An expression that describes the ripple content on pin 3 for a single R1C2 combination is:

$$V_{RIPPLE} = \frac{V_{CC}}{2} \times \frac{C1}{C2} \times \left(1 - \frac{V_{CC} \times f_{IN} \times C1}{I_2}\right) \text{ pk-pk}$$

It appears R1 can be chosen independent of ripple, however response time, or the time it takes V_{OUT} to stabilize at a new voltage increases as the size of C2 increases, so a compromise between ripple, response time, and linearity must be chosen carefully.

As a final consideration, the maximum attainable input frequency is determined by V_{CC}, C1 and I_2:

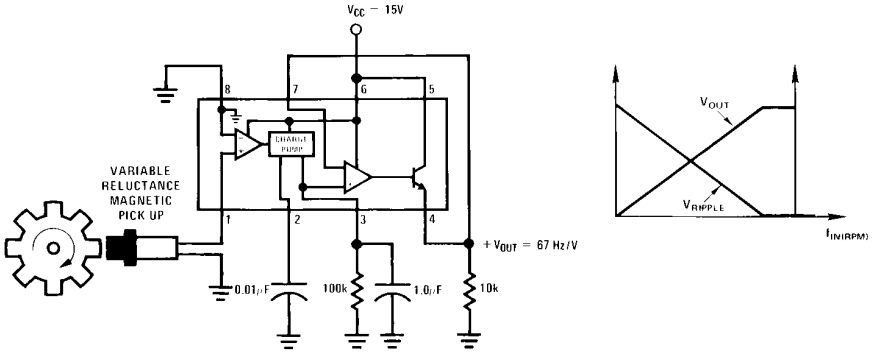
$$f_{MAX} = \frac{I_2}{C1 \times V_{CC}}$$

USING ZENER REGULATED OPTIONS (LM2917)

For those applications where an output voltage or current must be obtained independent of supply voltage variations, the LM2917 is offered. The most important consideration in choosing a dropping resistor from the unregulated supply to the device is that the tachometer and op amp circuitry alone require about 3 mA at the voltage level provided by the zener. At low supply voltages there must be some current flowing in the resistor above the 3 mA circuit current to operate the regulator. As an example, if the raw supply varies from 9V to 16V, a resistance of 470Ω will minimize the zener voltage variation to 160 mV. If the resistance goes under 400Ω or over 600Ω the zener variation quickly rises above 200 mV for the same input variation.

Typical Applications

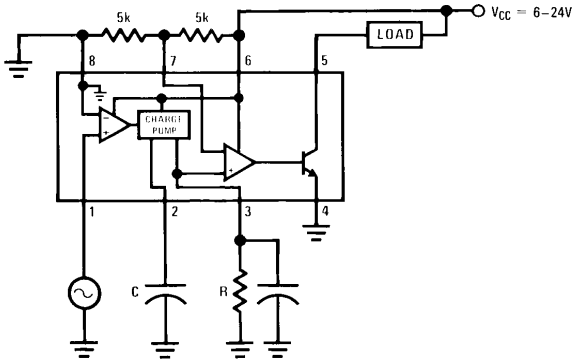
Minimum Component Tachometer



TL/H/7942–8

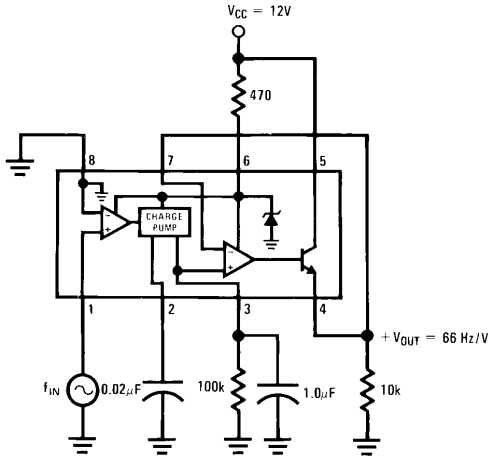
Typical Applications (Continued)

"Speed Switch" Load is Energized When $f_{IN} \geq \frac{1}{2RC}$



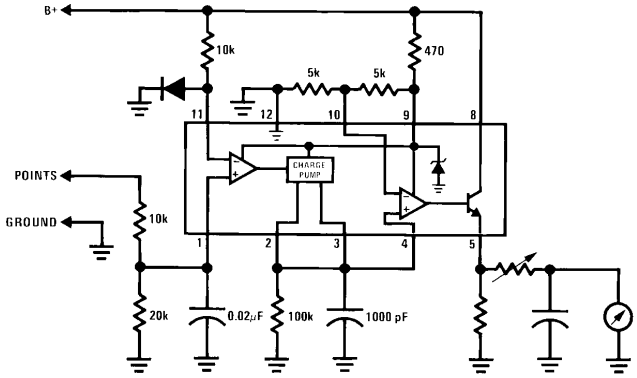
TL/H/7942–9

Zener Regulated Frequency to Voltage Converter



TL/H/7942–10

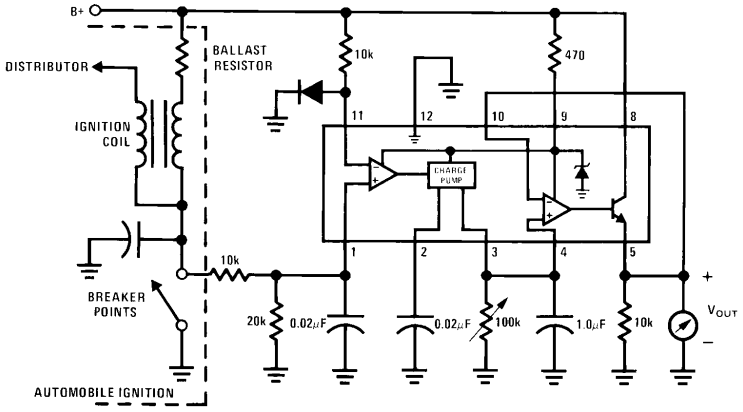
Breaker Point Dwell Meter



TL/H/7942–11

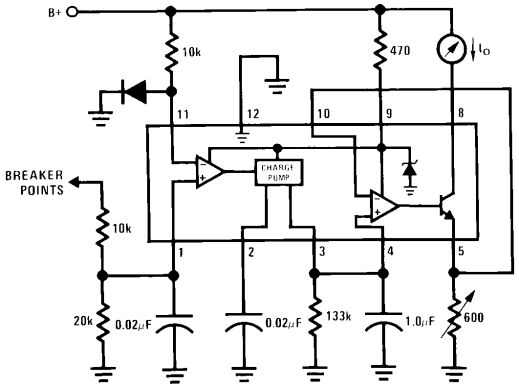
Typical Applications (Continued)

Voltage Driven Meter Indicating Engine RPM
V_O = 6V @ 400 Hz or 6000 ERPM (8 Cylinder Engine)



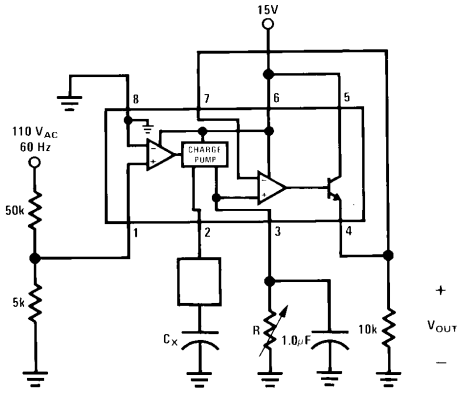
TL/H/7942–12

Current Driven Meter Indicating Engine RPM
I_O = 10 mA @ 300 Hz or 6000 ERPM (6 Cylinder Engine)



TL/H/7942–13

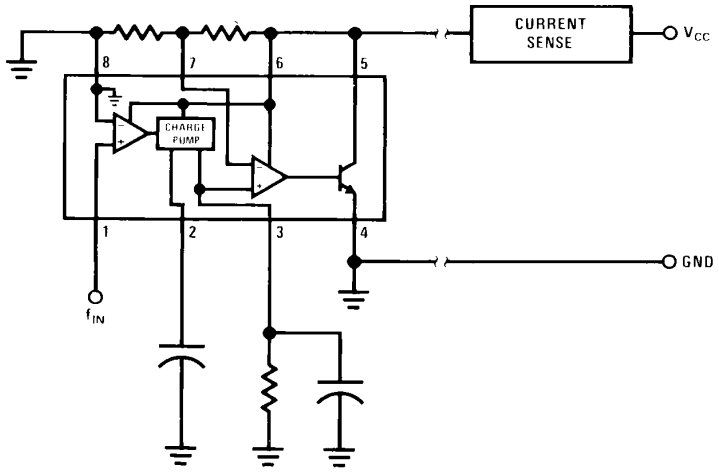
Capacitance Meter
V_{OUT} = 1V–10V for C_X = 0.01 to 0.1 mFd
(R = 111k)



TL/H/7942–14

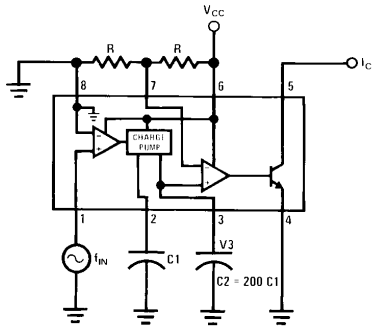
Typical Applications (Continued)

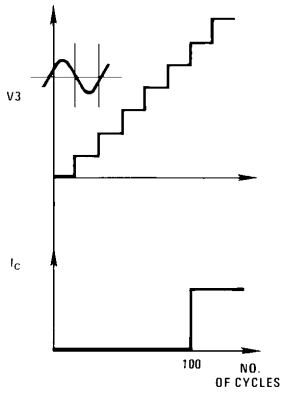
Two-Wire Remote Speed Switch



TL/H/7942–15

100 Cycle Delay Switch





TL/H/7942–16

V3 steps up in voltage by the amount $\frac{V_{CC} \times C1}{C2}$

for each complete input cycle (2 zero crossings)

Example:

If C2 = 200 C1 after 100 consecutive input cycles.

V3 = 1/2 V_{CC}

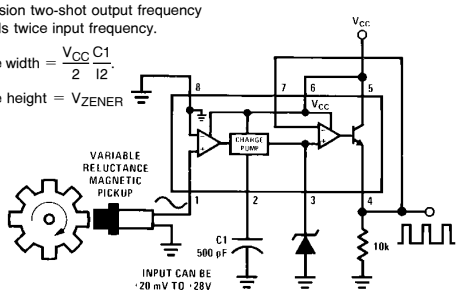
Typical Applications (Continued)

Variable Reluctance Magnetic Pickup Buffer Circuits

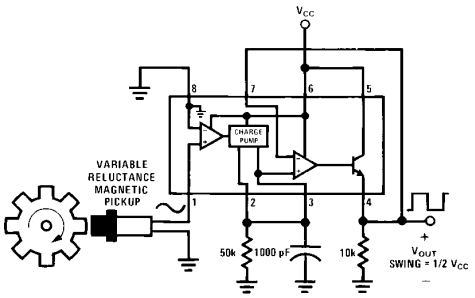
Precision two-shot output frequency equals twice input frequency.

Pulse width = $\frac{V_{CC}}{2}\frac{C1}{I2}$.

Pulse height = V_{ZENER}

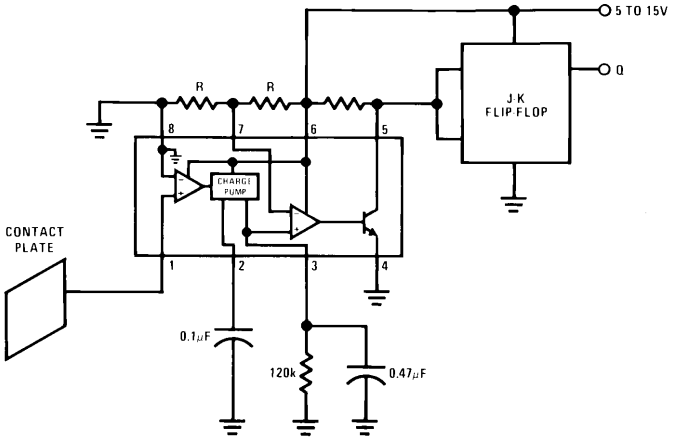


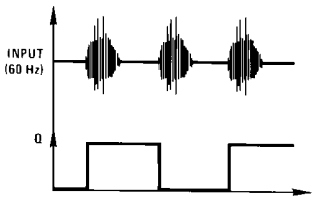
TL/H/7942–39



TL/H/7942–17

Finger Touch or Contact Switch

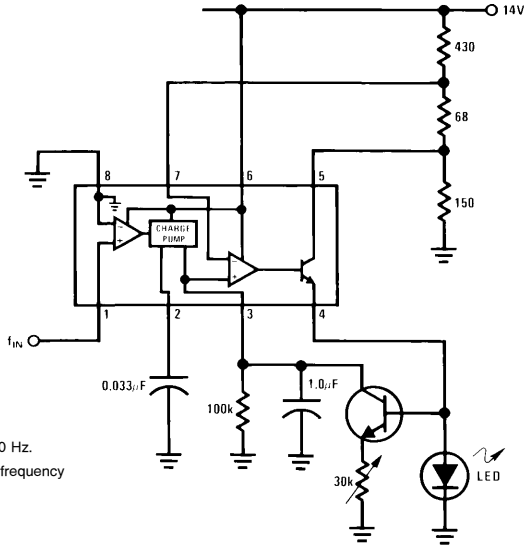




TL/H/7942–19

TL/H/7942–18

Flashing LED Indicates Overspeed



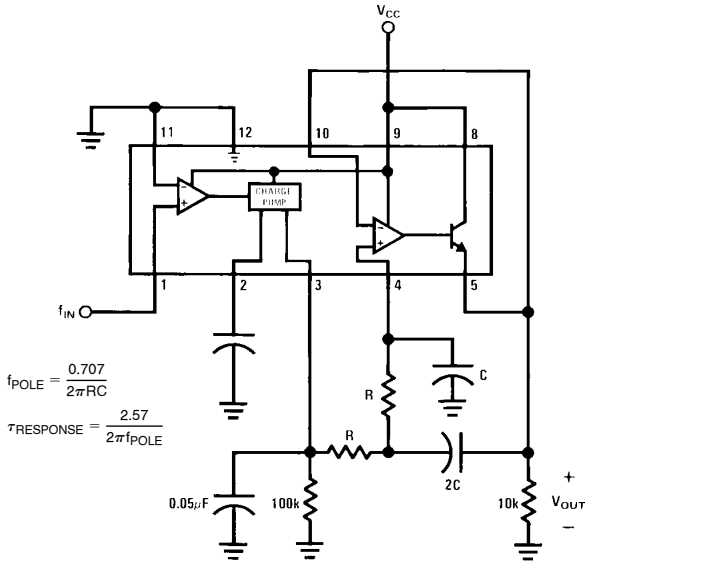
Flashing begins when $f_{IN} \geq 100$ Hz.

Flash rate increases with input frequency increase beyond trip point.

TL/H/7942–20

Typical Applications (Continued)

Frequency to Voltage Converter with 2 Pole Butterworth Filter to Reduce Ripple

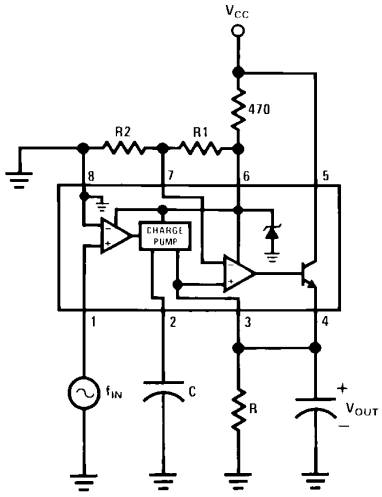


$$f_{POLE} = \frac{0.707}{2\pi RC}$$

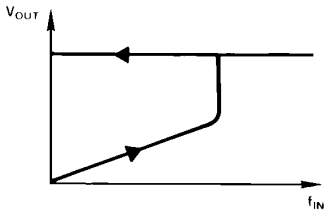
$$\tau_{RESPONSE} = \frac{2.57}{2\pi f_{POLE}}$$

TL/H/7942–21

Overspeed Latch



TL/H/7942–22



TL/H/7942–23

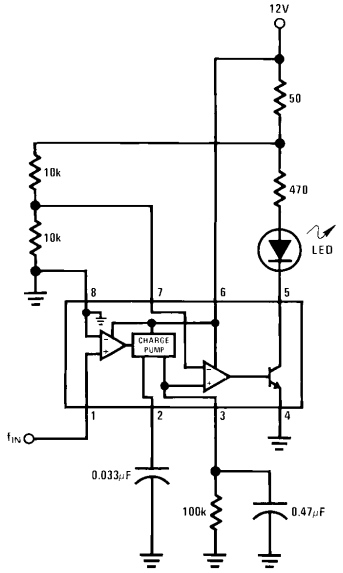
Output latches when

$$f_{IN} = \frac{R2}{R1 + R2}\frac{1}{RC}$$

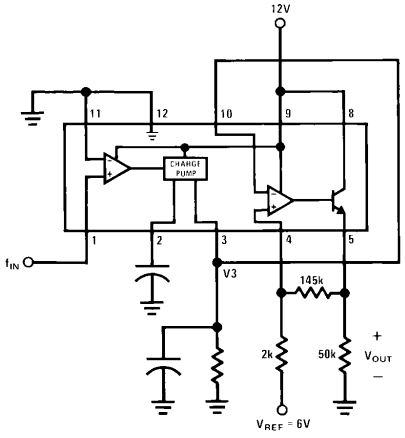
Reset by removing V_{CC}.

Typical Applications (Continued)

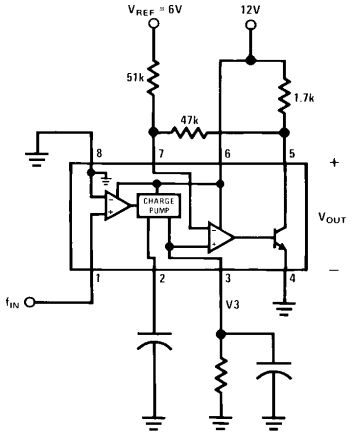
Some Frequency Switch Applications May Require Hysteresis in the Comparator Function Which can be Implemented in Several Ways:



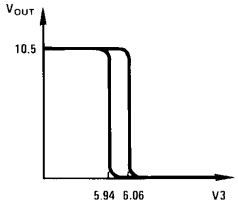
TL/H/7942–24



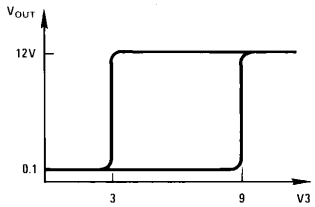
TL/H/7942–25



TL/H/7942–26



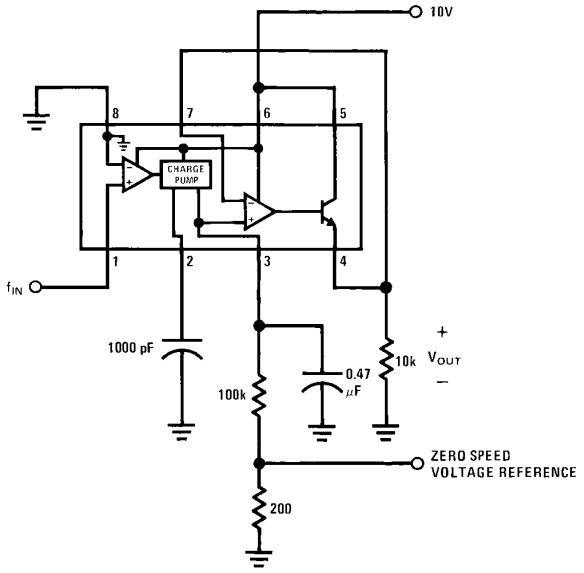
TL/H/7942–27



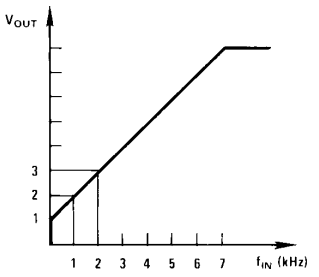
TL/H/7942–28

Typical Applications (Continued)

Changing the Output Voltage for an Input Frequency of Zero

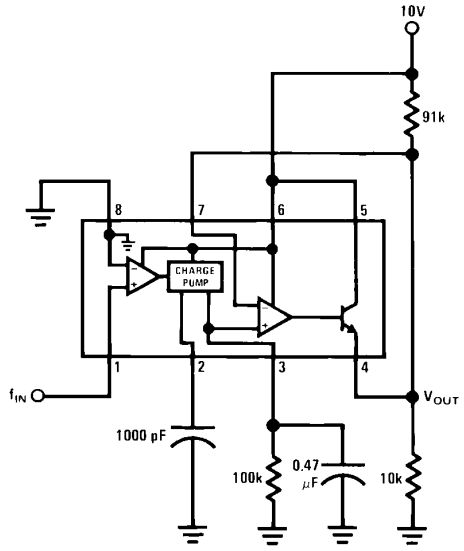


TL/H/7942–29

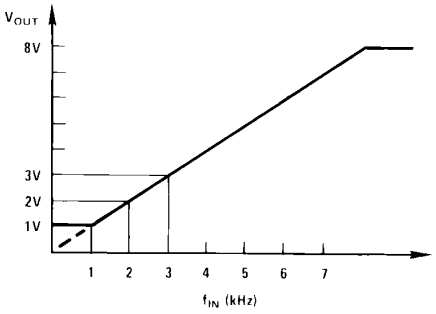


TL/H/7942–30

Changing Tachometer Gain Curve or Clamping the Minimum Output Voltage



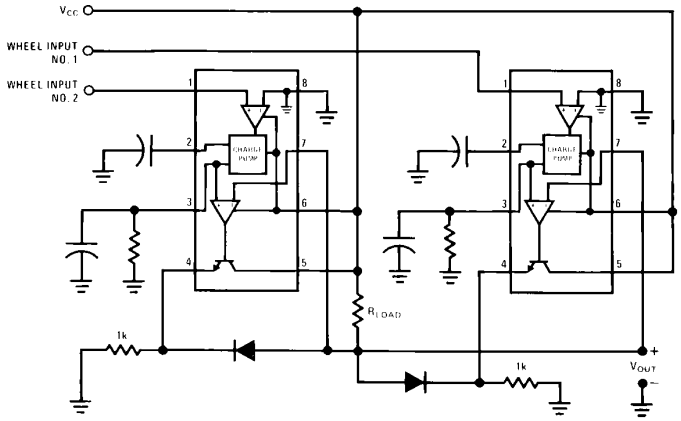
TL/H/7942–31



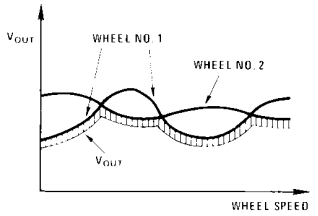
TL/H/7942–32

Anti-Skid Circuit Functions

"Select-Low" Circuit



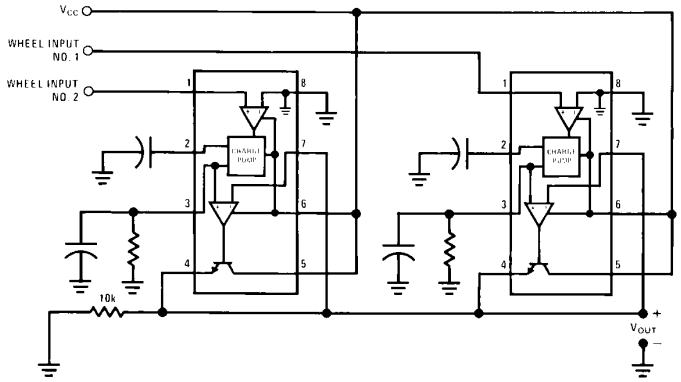
TL/H/7942–33



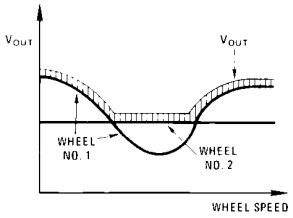
TL/H/7942–34

V_{OUT} is proportional to the lower of the two input wheel speeds.

"Select-High" Circuit



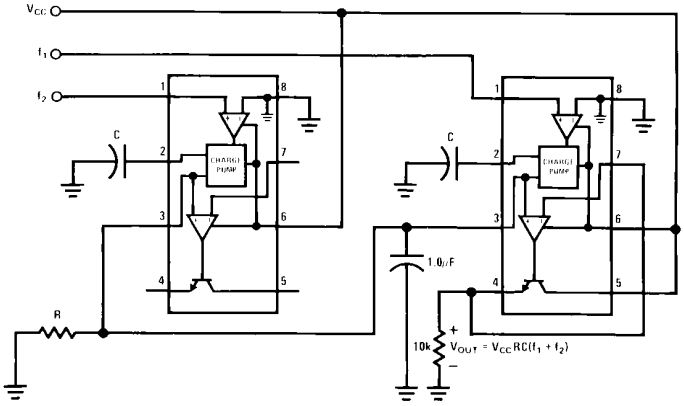
TL/H/7942–35



TL/H/7942–36

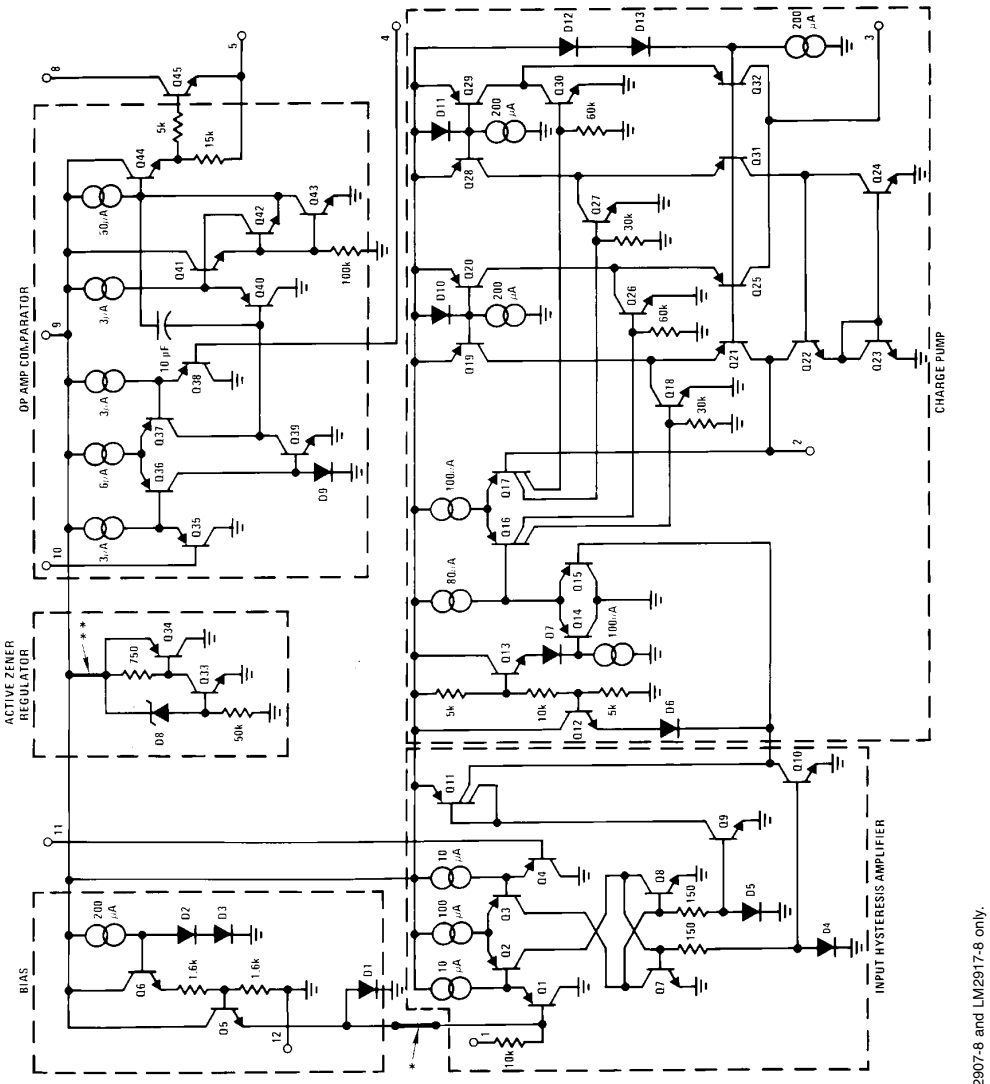
V_{OUT} is proportional to the higher of the two input wheel speeds.

"Select-Average" Circuit



TL/H/7942–37

Equivalent Schematic Diagram



TL/H/7942–38

*This connection made on LM2907-8 and LM2917-8 only.

**This connection made on LM2917 and LM2917-8 only.

National Semiconductor

January 1995

LM193/LM293/LM393/LM2903
Low Power Low Offset Voltage Dual Comparators

General Description

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

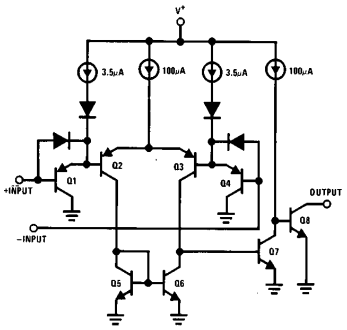
Advantages

- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near ground
- Compatible with all forms of logic
- Power drain suitable for battery operation

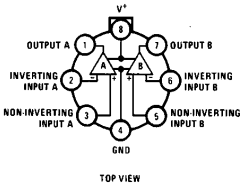
Features

- Wide supply
  - Voltage range 2.0V to 36V
  - single or dual supplies ±1.0V to ±18V
- Very low supply current drain (0.4 mA) — independent of supply voltage
- Low input biasing current 25 nA
- Low input offset current ±5 nA
  and maximum offset voltage ±3 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage, 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Schematic and Connection Diagrams

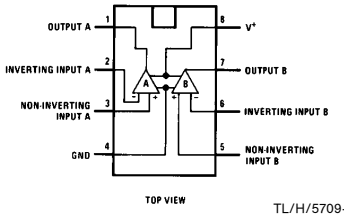


Metal Can Package



Order Number LM193H, LH193H/883*, LM193AH, LM193AH/883, LM293H, LM293AH, LM393H or LM393AH
See NS Package Number H08C

Dual-In-Line Package



TL/H/5709–1

Order Number LM193J/883*, LM193AJ/883, LM393J, LM393AJ, LM393M, LM2903M, LM393N, LM2903J or LM2903N
See NS Package Number J08A, M08A or N08E

*Also available per JM38510/11202

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
(Note 10)

Supply Voltage, V^+	36V
Differential Input Voltage (Note 8)	36V
Input Voltage	−0.3V to +36V
Input Current ($V_{IN} < -0.3V$) (Note 3)	50 mA
Power Dissipation (Note 1)	
Molded DIP	780 mW
Metal Can	660 mW
Small Outline Package	510 mW
Output Short-Circuit to Ground (Note 2)	Continuous
Operating Temperature Range	
LM393/LM393A	0°C to +70°C
LM293/LM293A	−25°C to +85°C
LM193/LM193A	−55°C to +125°C
LM2903	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 ''Surface Mounting Methods and Their Effect on Product Reliability'' for other methods of soldering surface mount devices.

ESD rating (1.5 kΩ in series with 100 pF) 1300V

Electrical Characteristics ($V^+ = 5V$, $T_A = 25°C$, unless otherwise stated)

Parameter	Conditions		LM193A			LM293A, LM393A			LM193			LM293, LM393			LM2903			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)			1.0	2.0		1.0	2.0		1.0	5.0		1.0	5.0		2.0	7.0	mV
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with Output In Linear Range, $V_{CM} = 0V$ (Note 5)			25	100		25	250		25	100		25	250		25	250	nA
Input Offset Current	$I_{IN}(+) - I_{IN}(-)$ $V_{CM} = 0V$			3.0	25		5.0	50		3.0	25		5.0	50		5.0	50	nA
Input Common Mode Voltage Range	$V^+ = 30V$ (Note 6)		0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V
Supply Current	$R_L = \infty$	$V^+ = 5V$		0.4	1		0.4	1		0.4	1		0.4	1		0.4	1.0	mA
		$V^+ = 36V$		1	2.5		1	2.5		1	2.5		1	2.5		1	2.5	mA
Voltage Gain	$R_L \geq 15\ k\Omega$, $V^+ = 15V$, $V_O = 1V$ to 11V		50	200		50	200		50	200		50	200		25	100		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, $V_{REF} = 1.4V$, $V_{RL} = 5V$, $R_L = 5.1\ k\Omega$			300			300			300			300			300		ns
Response Time	$V_{RL} = 5V$, $R_L = 5.1\ k\Omega$ (Note 7)			1.3			1.3			1.3			1.3			1.5		μs
Output Sink Current	$V_{IN}(-) = 1V$, $V_{IN}(+) = 0$, $V_O \leq 1.5V$		6.0	16		6.0	16		6.0	16		6.0	16		6.0	16		mA
Saturation Voltage	$V_{IN}(-) = 1V$, $V_{IN}(+) = 0$, $I_{SINK} \leq 4$ mA			250	400		250	400		250	400		250	400		250	400	mV
Output Leakage Current	$V_{IN}(-) = 0$, $V_{IN}(+) = 1V$, $V_O = 5V$			0.1			0.1			0.1			0.1			0.1		nA

Electrical Characteristics ($V^+ = 5V$) (Note 4)

Parameter	Conditions	LM193A			LM293A, LM393A			LM193			LM293, LM393			LM2903			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)			4.0			4.0			9			9		9	15	mV
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$			100			150			100			150		50	200	nA
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with Output in Linear Range, $V_{CM} = 0V$ (Note 5)			300			400			300			400		200	500	nA
Input Common Mode Voltage Range	$V^+ = 30V$ (Note 6)	0		$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$	V
Saturation Voltage	$V_{IN}(-) = 1V$, $V_{IN}(+) = 0$, $I_{SINK} \leq 4$ mA			700			700			700			700		400	700	mV
Output Leakage Current	$V_{IN}(-) = 0$, $V_{IN(+)} = 1V$, $V_O = 30V$			1.0			1.0			1.0			1.0			1.0	μA
Differential Input Voltage	Keep All V_{IN}'s $\geq 0V$ (or V^-, if Used), (Note 8)			36			36			36			36			36	V

Note 1: For operating at high temperatures, the LM393/LM393A and LM2903 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 170°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM193/LM193A/LM293/LM293A must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3V$.

Note 4: These specifications are limited to $-55°C \leq T_A \leq +125°C$, for the LM193/LM193A, With the LM293/LM293A all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$ and the LM393/LM393A temperature specifications are limited to $0°C \leq T_A \leq +70°C$. The LM2903 is limited to $-40°C \leq T_A \leq +85°C$.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$ at 25°C, but either or both inputs can go to 36V without damage, independent of the magnitude of V^+.

Note 7: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

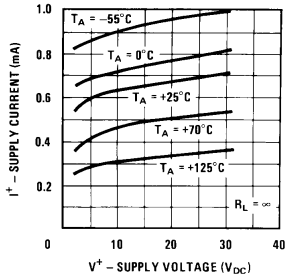
Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3V$ (or 0.3V below the magnitude of the negative power supply, if used).

Note 9: At output switch point, $V_O \cong 1.4V$, $R_S = 0\Omega$ with V^+ from 5V to 30V; and over the full input common-mode range (0V to $V^+ - 1.5V$), at 25°C.

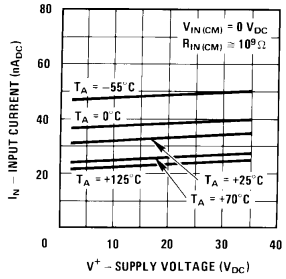
Note 10: Refer to RETS193AX for LM193AH military specifications and to RETS193X for LM193H military specifications.

Typical Performance Characteristics LM193/LM293/LM393, LM193A/LM293A/LM393A

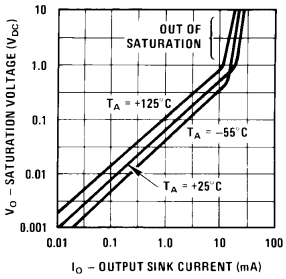
Supply Current



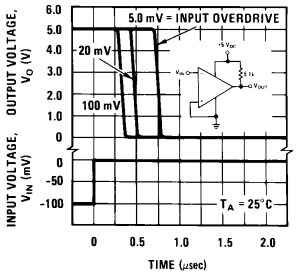
Input Current



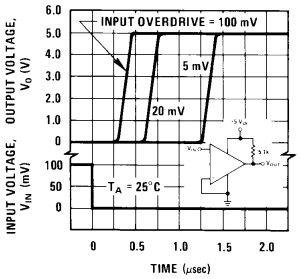
Output Saturation Voltage



Response Time for Various Input Overdrives—Negative Transition



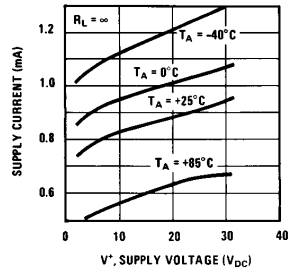
Response Time for Various Input Overdrives—Positive Transition



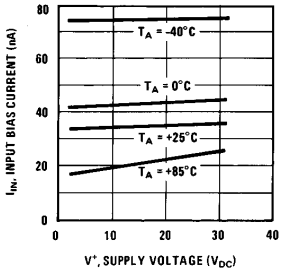
TL/H/5709–3

Typical Performance Characteristics LM2903

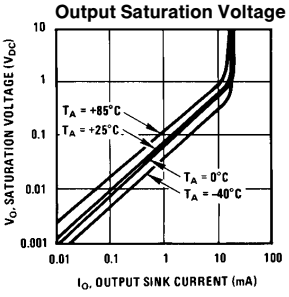
Supply Current



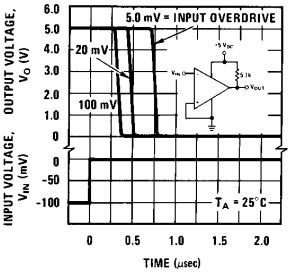
Input Current



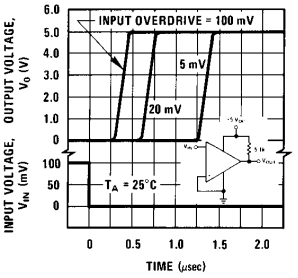
Output Saturation Voltage



Response Time for Various Input Overdrives—Negative Transition



Response Time for Various Input Overdrives—Positive Transition



TL/H/5709–4

Application Hints

The LM193 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator change states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to $< 10\ k\Omega$ reduces the feedback signal levels and finally, adding even a small amount (1.0 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

The bias network of the LM193 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2.0 V_{DC} to 30 V_{DC}.

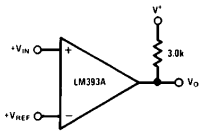
It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device (see Note 8). Protection should be provided to prevent the input voltages from going negative more than $-0.3\ V_{DC}$ (at 25°C). An input clamp diode can be used as shown in the applications section.

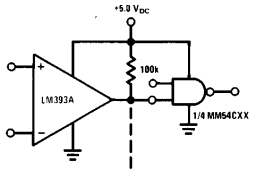
The output of the LM193 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM193 package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω r_{SAT} of the output transistor. The low offset voltage of the output transistor (1.0 mV) allows the output to clamp essentially to ground level for small load currents.

Typical Applications ($V^+ = 5.0\ V_{DC}$)

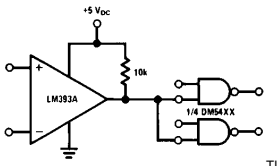
Basic Comparator



Driving CMOS



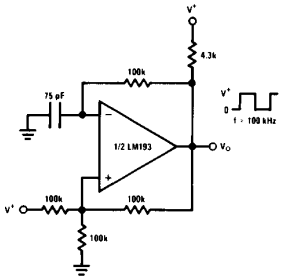
Driving TTL



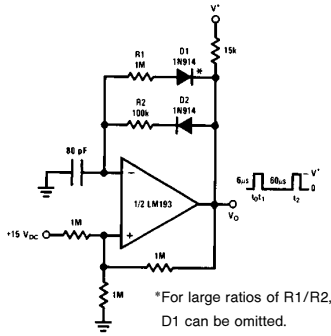
TL/H/5709–2

Typical Applications (Continued)

Squarewave Oscillator

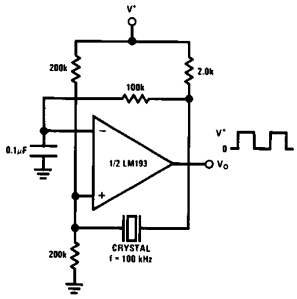


Pulse Generator

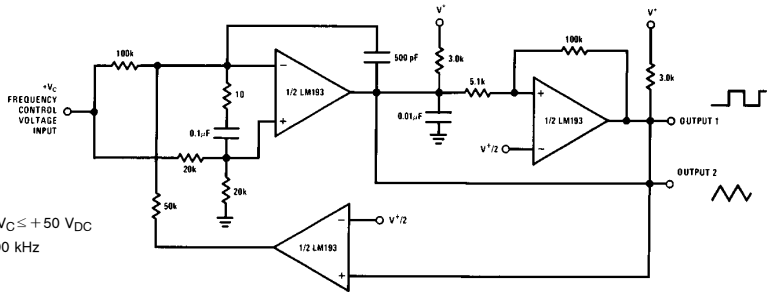


*For large ratios of R1/R2, D1 can be omitted.

Crystal Controlled Oscillator



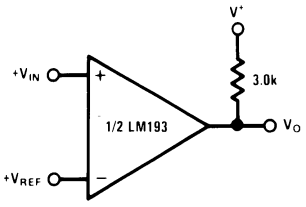
Two-Decade High-Frequency VCO



V* = +30 V_{DC}
+250 $mV_{DC} \leq V_C \leq +50\ V_{DC}$
700 Hz $\leq f_O \leq$ 100 kHz

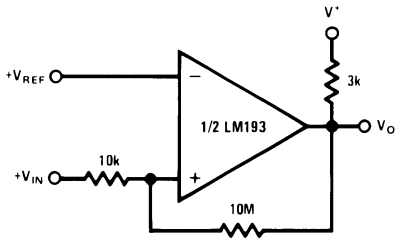
TL/H/5709–5

Basic Comparator



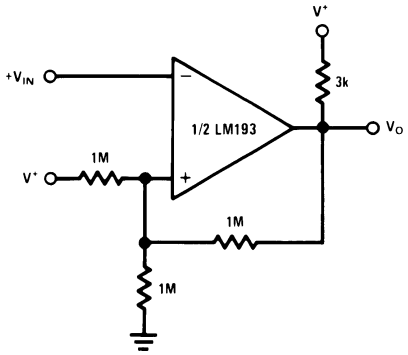
TL/H/5709–6

Non-Inverting Comparator with Hysteresis



TL/H/5709–9

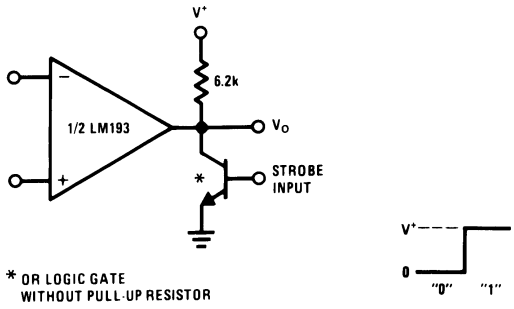
Inverting Comparator with Hysteresis



TL/H/5709–10

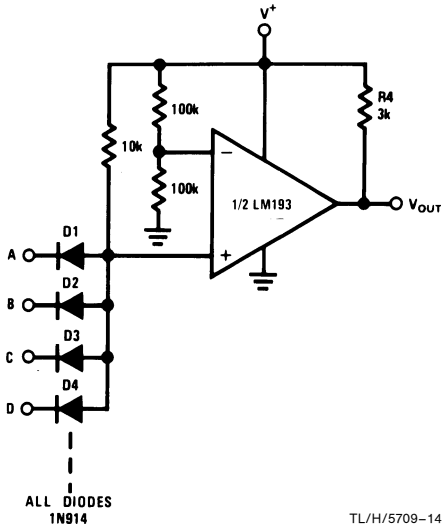
Typical Applications (Continued)

Output Strobing



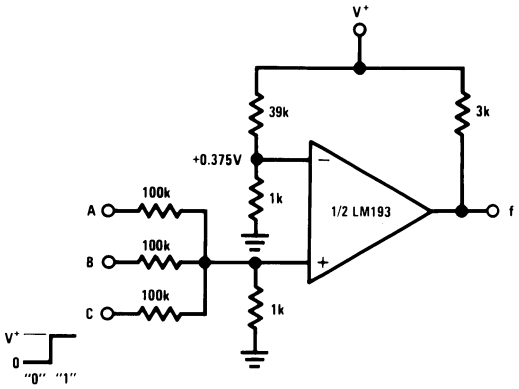
TL/H/5709–11

Large Fan-in AND Gate



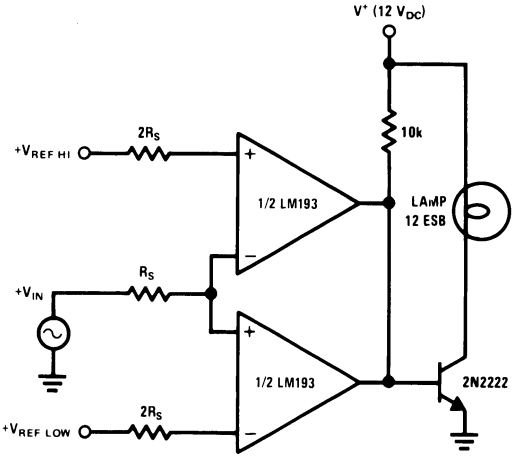
TL/H/5709–14

AND Gate



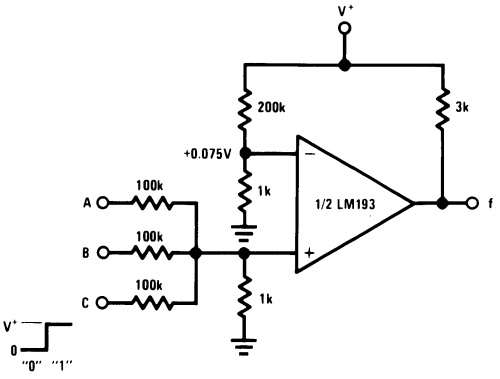
TL/H/5709–12

Limit Comparator



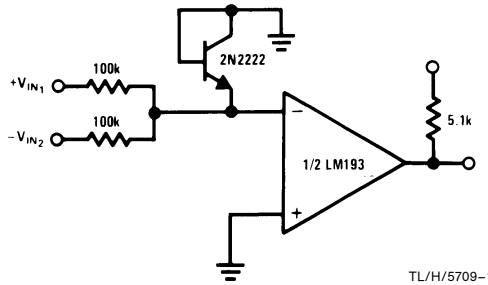
TL/H/5709–15

OR Gate



TL/H/5709–13

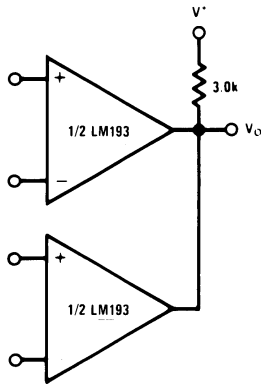
Comparing Input Voltages of Opposite Polarity



TL/H/5709–16

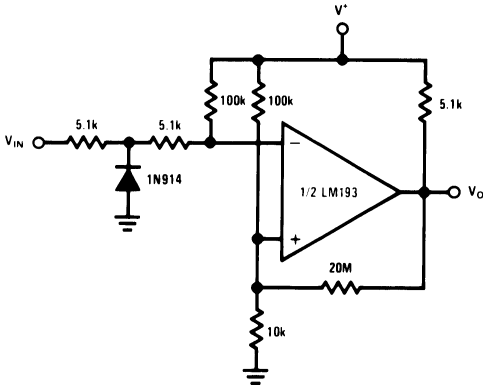
Typical Applications (Continued)

ORing the Outputs



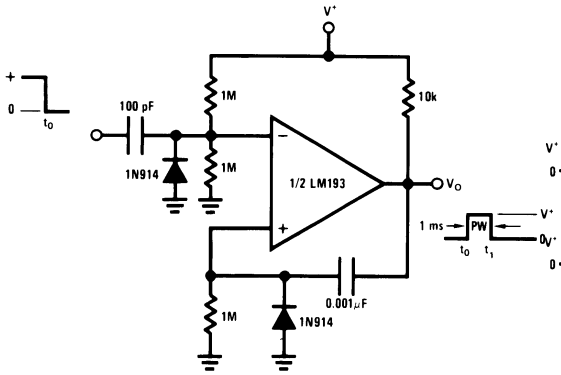
TL/H/5709–17

Zero Crossing Detector (Single Power Supply)

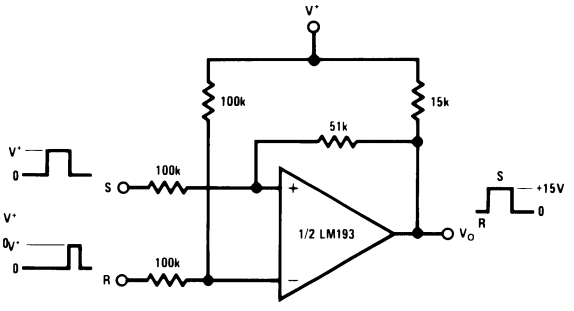


TL/H/5709–21

One-Shot Multivibrator



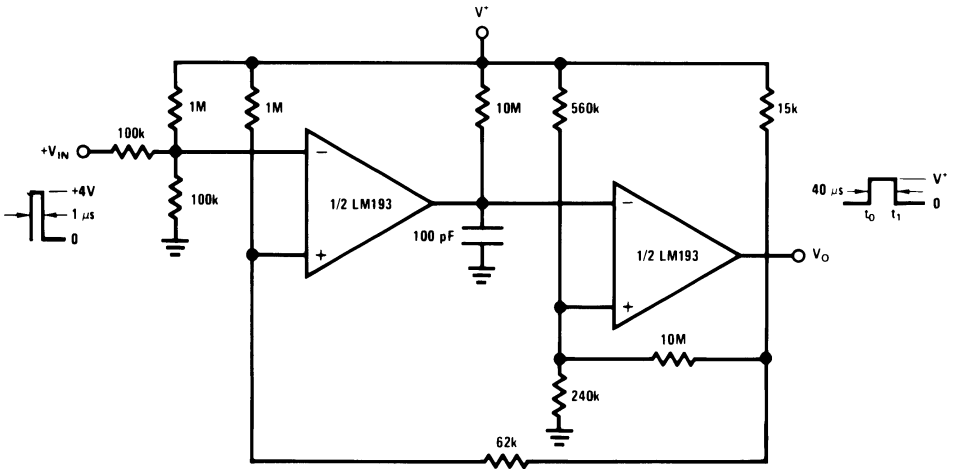
Bi-Stable Multivibrator



TL/H/5709–24

TL/H/5709–22

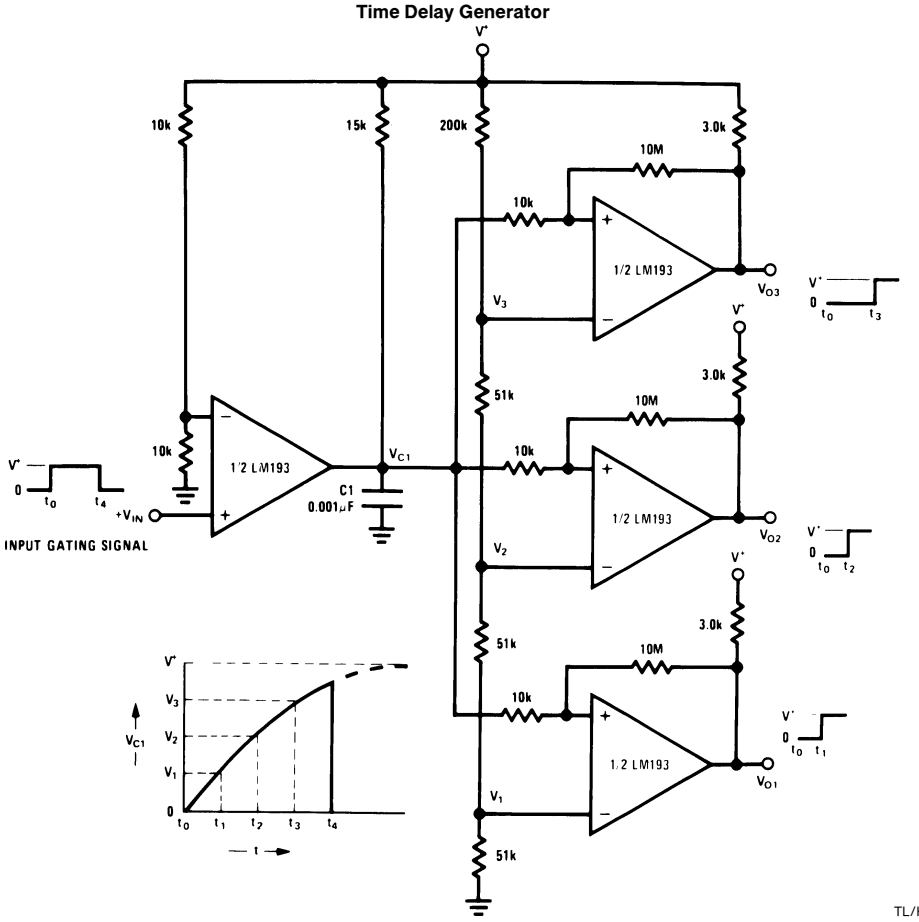
One-Shot Multivibrator with Input Lock Out



TL/H/5709–23

Typical Applications (Continued) ($V^+ = V_{DC}$)

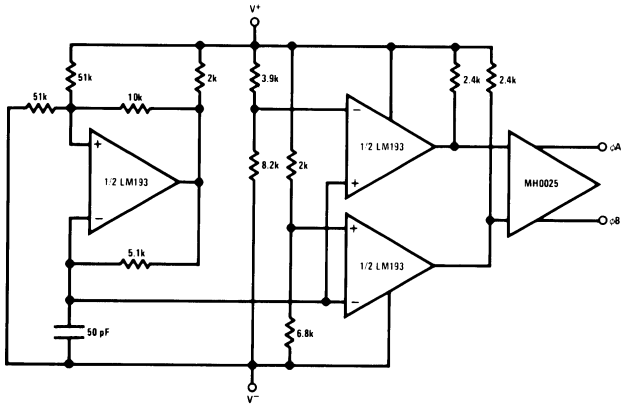
Time Delay Generator



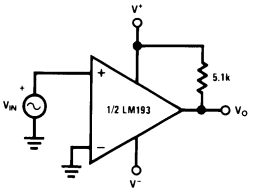
TL/H/5709–7

Split-Supply Applications ($V^+ = +15\ V_{DC}$ and $V^- = -15\ V_{DC}$)

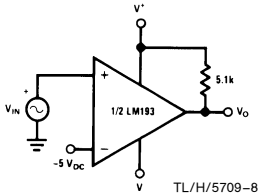
MOS Clock Driver



Zero Crossing Detector



Comparator With a Negative Reference

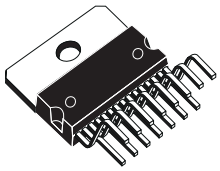


TL/H/5709–8

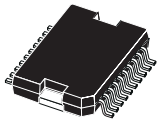
L298

DUAL FULL-BRIDGE DRIVER

- OPERATING SUPPLY VOLTAGE UP TO 46 V
- TOTAL DC CURRENT UP TO 4 A
- LOW SATURATION VOLTAGE
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VOLTAGE UP TO 1.5 V (HIGH NOISE IMMUNITY)



Multiwatt15



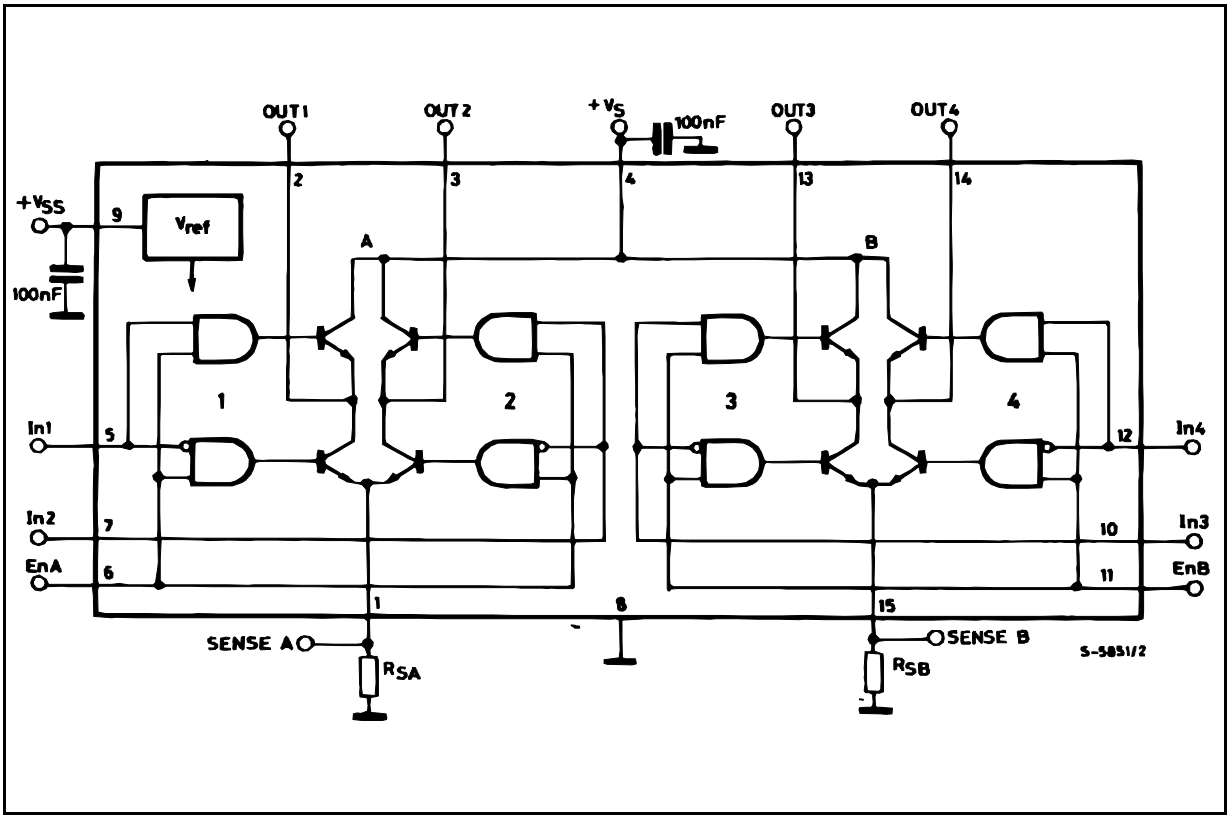
PowerSO20

ORDERING NUMBERS : L298N (Multiwatt Vert.)
L298HN (Multiwatt Horiz.)
L298P (PowerSO20)

DESCRIPTION

The L298 is an integrated monolithic circuit in a 15-lead Multiwatt and PowerSO20 packages. It is a high voltage, high current dual full-bridge driver designed to accept standard TTL logic levels and drive inductive loads such as relays, solenoids, DC and stepping motors. Two enable inputs are provided to enable or disable the device independently of the input signals. The emitters of the lower transistors of each bridge are connected together and the corresponding external terminal can be used for the connection of an external sensing resistor. An additional supply input is provided so that the logic works at a lower voltage.

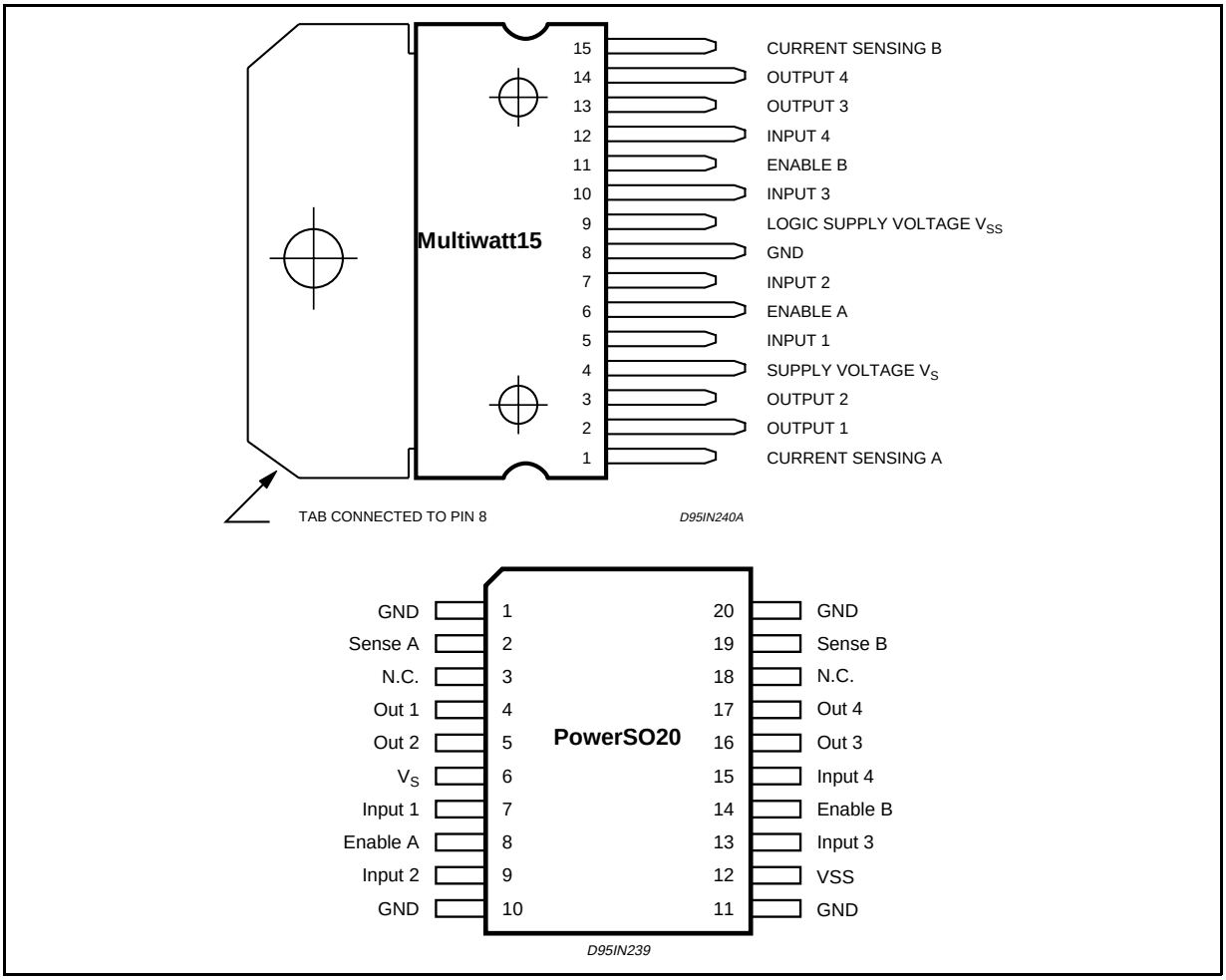
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Power Supply	50	V
V_{SS}	Logic Supply Voltage	7	V
V_I,V_{en}	Input and Enable Voltage	–0.3 to 7	V
I_O	Peak Output Current (each Channel) – Non Repetitive (t = 100µs) –Repetitive (80% on –20% off; t_{on} = 10ms) –DC Operation	 3 2.5 2	 A A A
V_{sens}	Sensing Voltage	–1 to 2.3	V
P_{tot}	Total Power Dissipation (T_{case} = 75°C)	25	W
T_{op}	Junction Operating Temperature	–25 to 130	°C
T_{stg}, T_j	Storage and Junction Temperature	–40 to 150	°C

PIN CONNECTIONS (top view)



THERMAL DATA

Symbol	Parameter		PowerSO20	Multiwatt15	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max.	–	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	13 (*)	35	°C/W

(*) Mounted on aluminum substrate

PIN FUNCTIONS (refer to the block diagram)

MW.15	PowerSO	Name	Function
1;15	2;19	Sense A; Sense B	Between this pin and ground is connected the sense resistor to control the current of the load.
2;3	4;5	Out 1; Out 2	Outputs of the Bridge A; the current that flows through the load connected between these two pins is monitored at pin 1.
4	6	V_S	Supply Voltage for the Power Output Stages. A non-inductive 100nF capacitor must be connected between this pin and ground.
5;7	7;9	Input 1; Input 2	TTL Compatible Inputs of the Bridge A.
6;11	8;14	Enable A; Enable B	TTL Compatible Enable Input: the L state disables the bridge A (enable A) and/or the bridge B (enable B).
8	1,10,11,20	GND	Ground.
9	12	VSS	Supply Voltage for the Logic Blocks. A100nF capacitor must be connected between this pin and ground.
10; 12	13;15	Input 3; Input 4	TTL Compatible Inputs of the Bridge B.
13; 14	16;17	Out 3; Out 4	Outputs of the Bridge B. The current that flows through the load connected between these two pins is monitored at pin 15.
–	3;18	N.C.	Not Connected

ELECTRICAL CHARACTERISTICS (V_S = 42V; V_{SS} = 5V, T_j = 25°C; unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage (pin 4)	Operative Condition	V_{IH} +2.5		46	V
V_{SS}	Logic Supply Voltage (pin 9)		4.5	5	7	V
I_S	Quiescent Supply Current (pin 4)	V_{en} = H; I_L = 0 V_i = L V_i = H		13 50	22 70	mA mA
		V_{en} = L V_i = X			4	mA
I_{SS}	Quiescent Current from V_{SS} (pin 9)	V_{en} = H; I_L = 0 V_i = L V_i = H		24 7	36 12	mA mA
		V_{en} = L V_i = X			6	mA
V_{iL}	Input Low Voltage (pins 5, 7, 10, 12)		–0.3		1.5	V
V_{iH}	Input High Voltage (pins 5, 7, 10, 12)		2.3		VSS	V
I_{iL}	Low Voltage Input Current (pins 5, 7, 10, 12)	V_i = L			–10	µA
I_{iH}	High Voltage Input Current (pins 5, 7, 10, 12)	Vi = H ≤ V_{SS} –0.6V		30	100	µA
V_{en} = L	Enable Low Voltage (pins 6, 11)		–0.3		1.5	V
V_{en} = H	Enable High Voltage (pins 6, 11)		2.3		V_{SS}	V
I_{en} = L	Low Voltage Enable Current (pins 6, 11)	V_{en} = L			–10	µA
I_{en} = H	High Voltage Enable Current (pins 6, 11)	V_{en} = H ≤ V_{SS} –0.6V		30	100	µA
$V_{CEsat\ (H)}$	Source Saturation Voltage	I_L = 1A I_L = 2A	0.95	1.35 2	1.7 2.7	V V
$V_{CEsat\ (L)}$	Sink Saturation Voltage	I_L = 1A (5) I_L = 2A (5)	0.85	1.2 1.7	1.6 2.3	V V
V_{CEsat}	Total Drop	I_L = 1A (5) I_L = 2A (5)	1.80		3.2 4.9	V V
V_{sens}	Sensing Voltage (pins 1, 15)		–1 (1)		2	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_1 (V_i)	Source Current Turn-off Delay	0.5 V_i to 0.9 I_L (2); (4)		1.5		µs
T_2 (V_i)	Source Current Fall Time	0.9 I_L to 0.1 I_L (2); (4)		0.2		µs
T_3 (V_i)	Source Current Turn-on Delay	0.5 V_i to 0.1 I_L (2); (4)		2		µs
T_4 (V_i)	Source Current Rise Time	0.1 I_L to 0.9 I_L (2); (4)		0.7		µs
T_5 (V_i)	Sink Current Turn-off Delay	0.5 V_i to 0.9 I_L (3); (4)		0.7		µs
T_6 (V_i)	Sink Current Fall Time	0.9 I_L to 0.1 I_L (3); (4)		0.25		µs
T_7 (V_i)	Sink Current Turn-on Delay	0.5 V_i to 0.9 I_L (3); (4)		1.6		µs
T_8 (V_i)	Sink Current Rise Time	0.1 I_L to 0.9 I_L (3); (4)		0.2		µs
fc (V_i)	Commutation Frequency	I_L = 2A		25	40	KHz
T_1 (V_{en})	Source Current Turn-off Delay	0.5 V_{en} to 0.9 I_L (2); (4)		3		µs
T_2 (V_{en})	Source Current Fall Time	0.9 I_L to 0.1 I_L (2); (4)		1		µs
T_3 (V_{en})	Source Current Turn-on Delay	0.5 V_{en} to 0.1 I_L (2); (4)		0.3		µs
T_4 (V_{en})	Source Current Rise Time	0.1 I_L to 0.9 I_L (2); (4)		0.4		µs
T_5 (V_{en})	Sink Current Turn-off Delay	0.5 V_{en} to 0.9 I_L (3); (4)		2.2		µs
T_6 (V_{en})	Sink Current Fall Time	0.9 I_L to 0.1 I_L (3); (4)		0.35		µs
T_7 (V_{en})	Sink Current Turn-on Delay	0.5 V_{en} to 0.9 I_L (3); (4)		0.25		µs
T_8 (V_{en})	Sink Current Rise Time	0.1 I_L to 0.9 I_L (3); (4)		0.1		µs

1) 1)Sensing voltage can be –1 V for t ≤ 50 µsec; in steady state V_{sens} min ≥ – 0.5 V.
2) See fig. 2.
3) See fig. 4.
4) The load must be a pure resistor.

Figure 1 : Typical Saturation Voltage vs. Output Current.

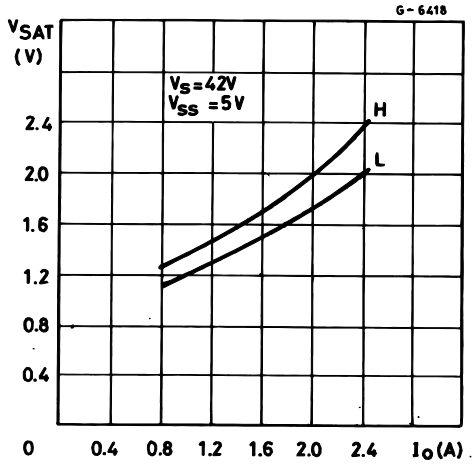
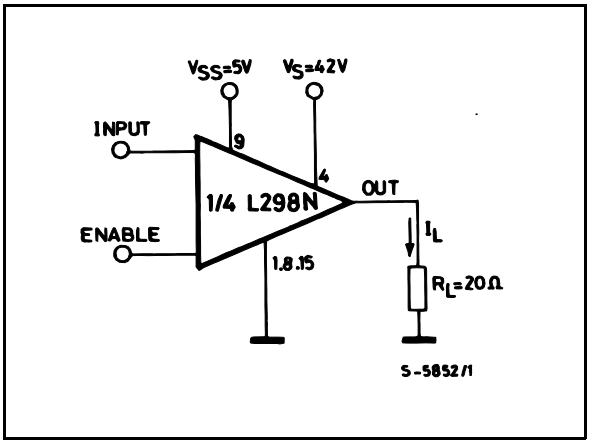


Figure 2 : Switching Times Test Circuits.



Note : For INPUT Switching, set EN = H
For ENABLE Switching, set IN = H

Figure 3 : Source Current Delay Times vs. Input or Enable Switching.

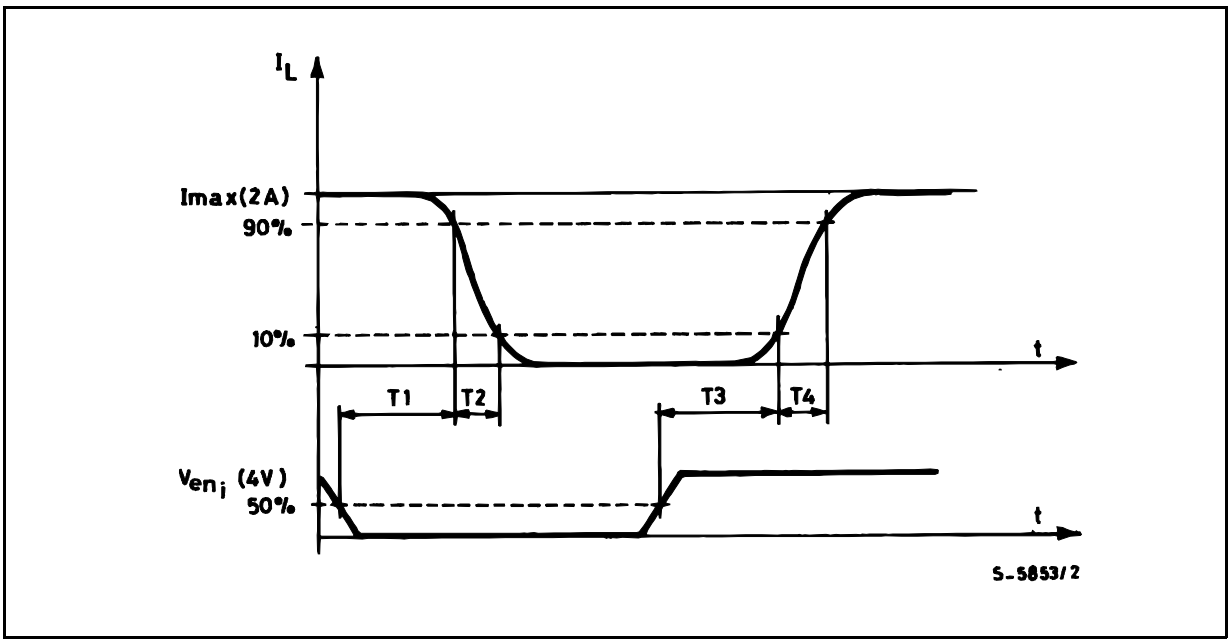
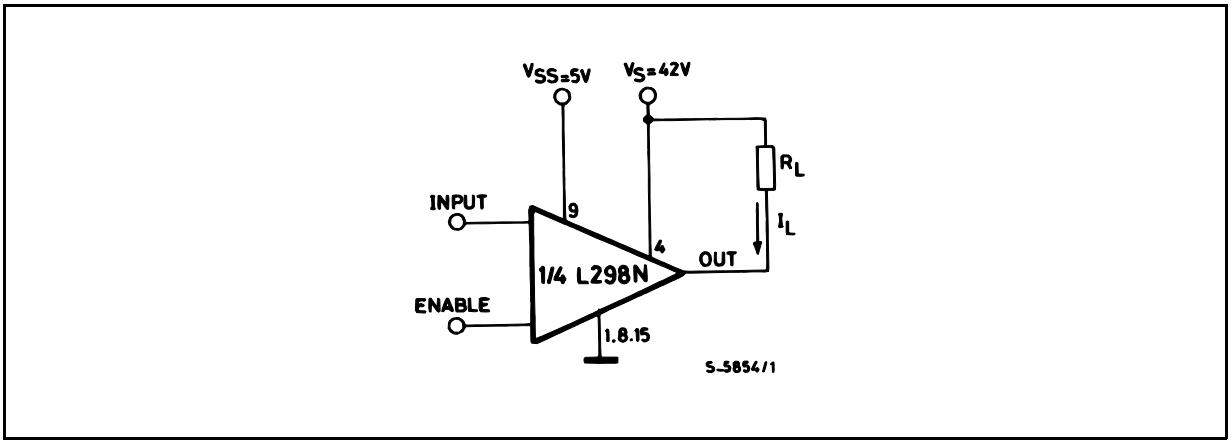


Figure 4 : Switching Times Test Circuits.



Note : For INPUT Switching, set EN = H
For ENABLE Switching, set IN = L

Figure 5 : Sink Current Delay Times vs. Input 0 V Enable Switching.

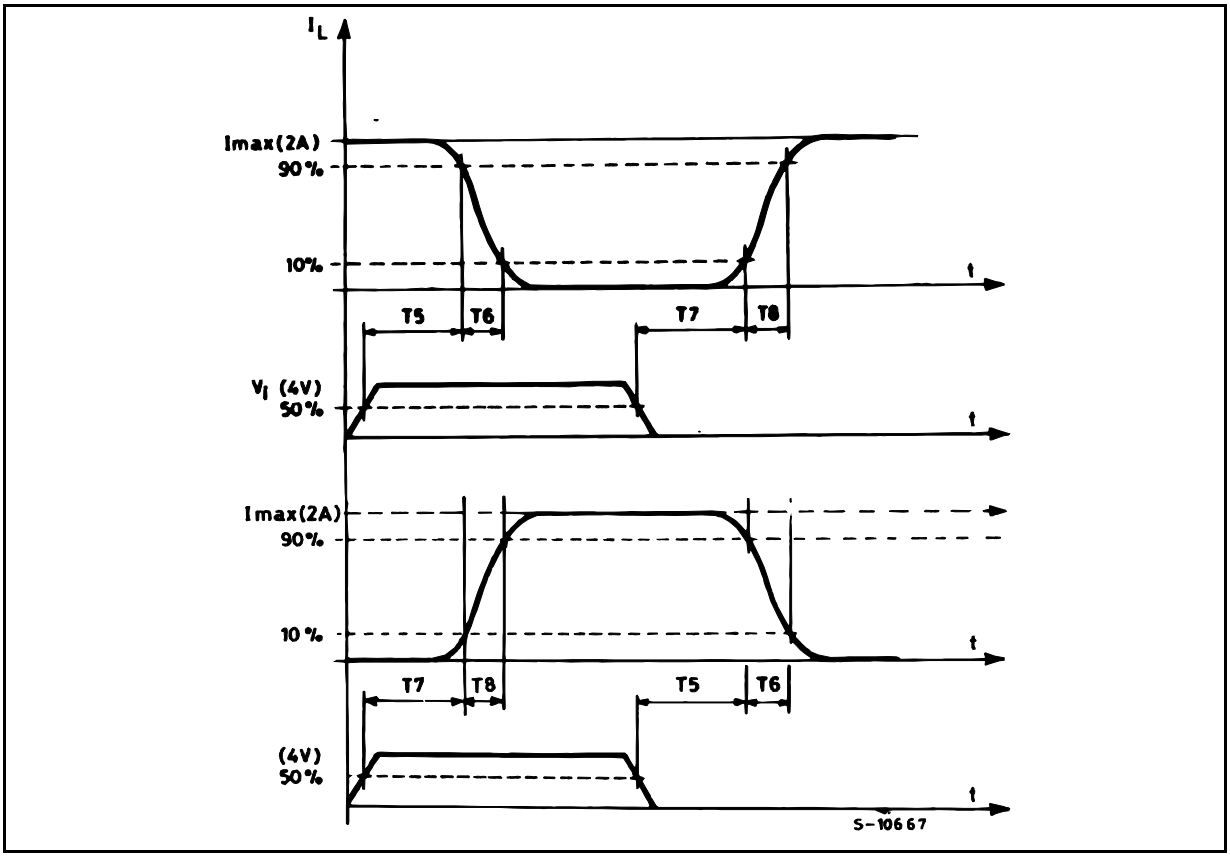
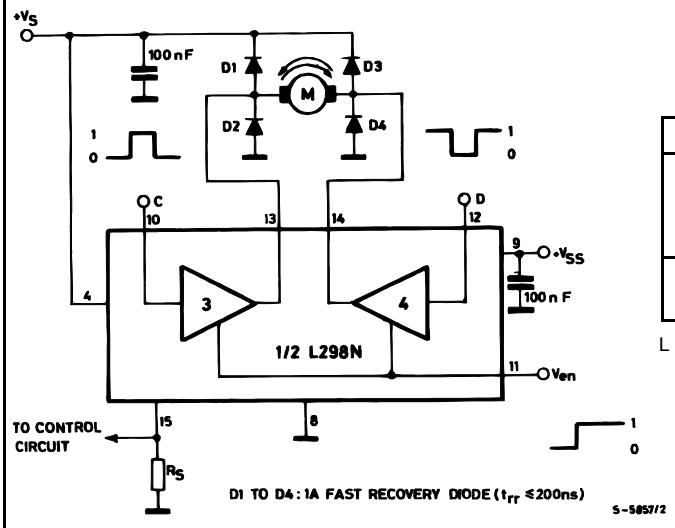


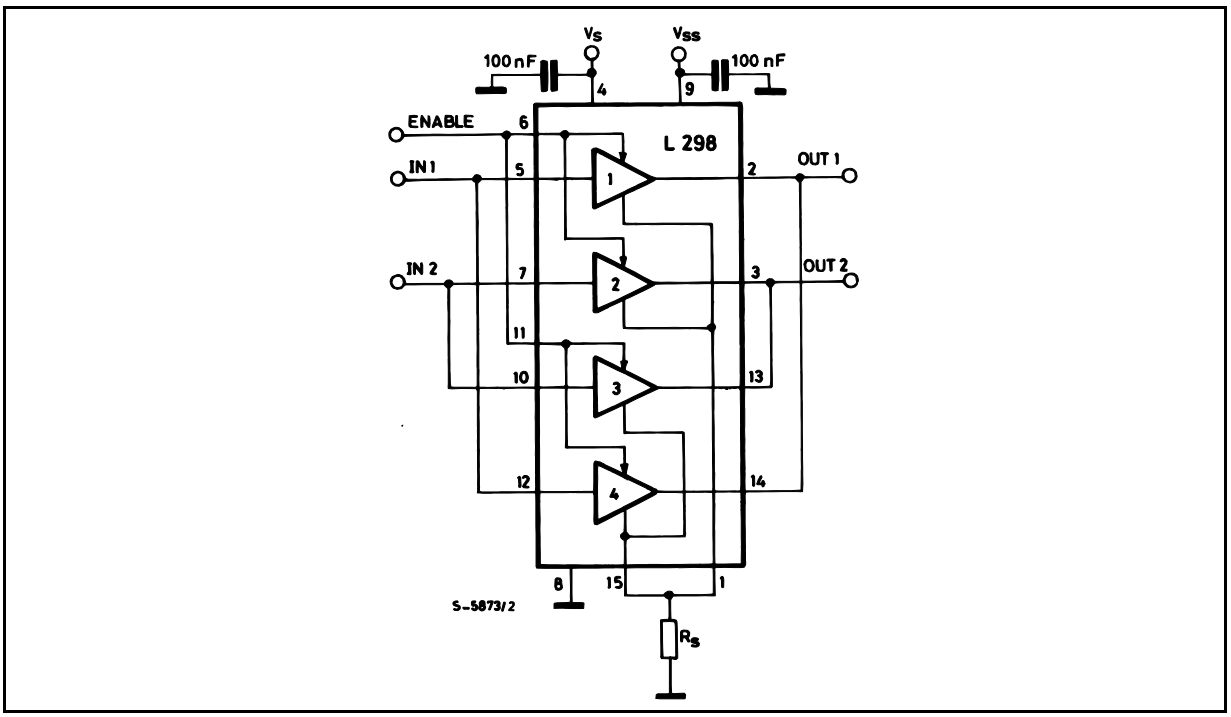
Figure 6 : Bidirectional DC Motor Control.



Inputs		Function
V_{en} = H	C = H ; D = L	Forward
	C = L ; D = H	Reverse
	C = D	Fast Motor Stop
V_{en} = L	C = X ; D = X	Free Running Motor Stop

L = Low H = High X = Don't care

Figure 7 : For higher currents, outputs can be paralleled. Take care to parallel channel 1 with channel 4 and channel 2 with channel 3.



APPLICATION INFORMATION (Refer to the block diagram)

1.1. POWER OUTPUT STAGE

The L298 integrates two power output stages (A ; B). The power output stage is a bridge configuration and its outputs can drive an inductive load in common or differenzial mode, depending on the state of the inputs. The current that flows through the load comes out from the bridge at the sense output : an external resistor (R_{SA} ; R_{SB}.) allows to detect the intensity of this current.

1.2. INPUT STAGE

Each bridge is driven by means of four gates the input of which are In1 ; In2 ; EnA and In3 ; In4 ; EnB. The In inputs set the bridge state when The En input is high ; a low state of the En input inhibits the bridge. All the inputs are TTL compatible.

2. SUGGESTIONS

A non inductive capacitor, usually of 100 nF, must be foreseen between both Vs and Vss, to ground, as near as possible to GND pin. When the large capacitor of the power supply is too far from the IC, a second smaller one must be foreseen near the L298.

The sense resistor, not of a wire wound type, must be grounded near the negative pole of Vs that must be near the GND pin of the I.C.

Each input must be connected to the source of the driving signals by means of a very short path.

Turn-On and Turn-Off : Before to Turn-ON the Supply Voltage and before to Turn it OFF, the Enable input must be driven to the Low state.

3. APPLICATIONS

Fig 6 shows a bidirectional DC motor control Schematic Diagram for which only one bridge is needed. The external bridge of diodes D1 to D4 is made by four fast recovery elements (trr $\leq$ 200 nsec) that must be chosen of a VF as low as possible at the worst case of the load current.

The sense output voltage can be used to control the current amplitude by chopping the inputs, or to provide overcurrent protection by switching low the enable input.

The brake function (Fast motor stop) requires that the Absolute Maximum Rating of 2 Amps must never be overcome.

When the repetitive peak current needed from the load is higher than 2 Amps, a paralleled configuration can be chosen (See Fig.7).

An external bridge of diodes are required when inductive loads are driven and when the inputs of the IC are chopped ; Shottky diodes would be preferred.

This solution can drive until 3 Amps In DC operation and until 3.5 Amps of a repetitive peak current.

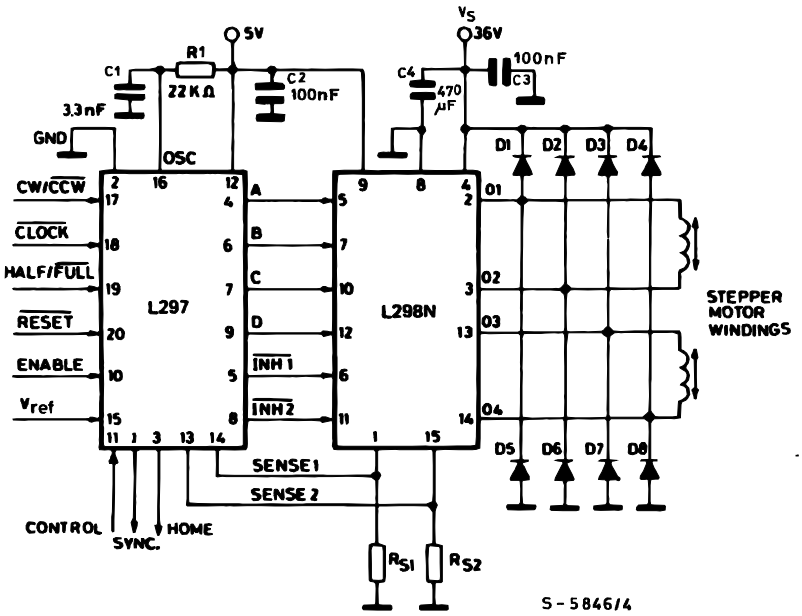
On Fig 8 it is shown the driving of a two phase bipolar stepper motor ; the needed signals to drive the inputs of the L298 are generated, in this example, from the IC L297.

Fig 9 shows an example of P.C.B. designed for the application of Fig 8.

Fig 10 shows a second two phase bipolar stepper motor control circuit where the current is controlled by the I.C. L6506.

Figure 8 : Two Phase Bipolar Stepper Motor Circuit.

This circuit drives bipolar stepper motors with winding currents up to 2 A. The diodes are fast 2 A types.



$R_{S1} = R_{S2} = 0.5\ \Omega$

D1 to D8 = 2 A Fast diodes { $V_F \leq 1.2$ V @ I = 2 A
trr ≤ 200 ns

ChipCorder®
TECHNOLOGY BY ISD

ISD1400 Series

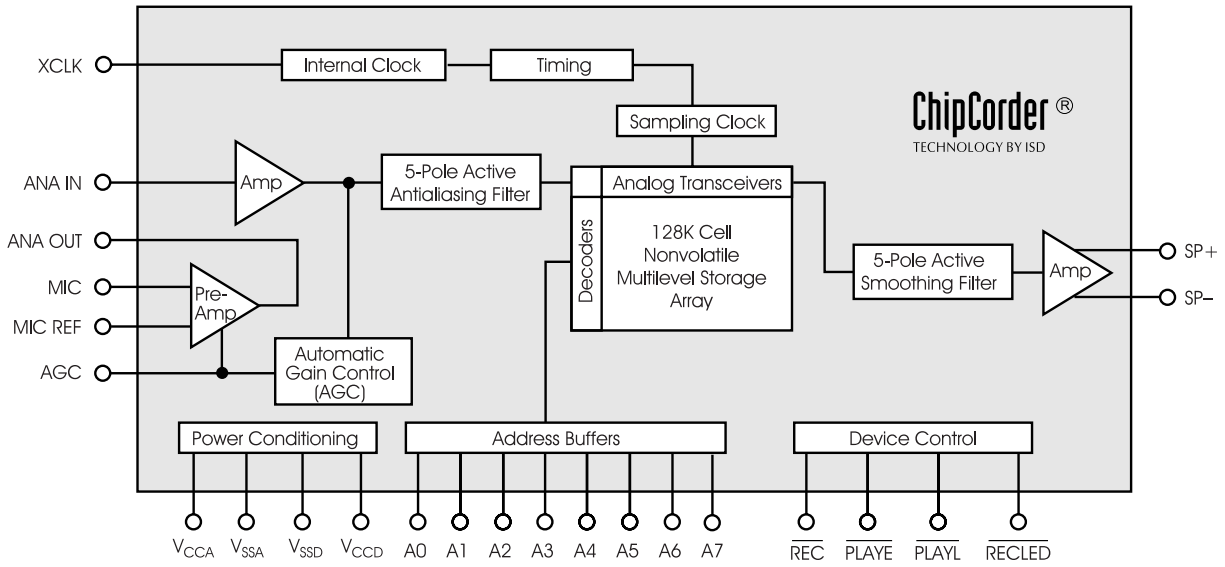
Single-Chip Voice Record/Playback Devices
16- and 20-Second Durations

GENERAL DESCRIPTION

Information Storage Devices' ISD1400 ChipCorder® series provides high-quality, single-chip record/playback solutions to short-duration messaging applications. The CMOS devices include an on-chip oscillator, microphone preamplifier, automatic gain control, antialiasing filter, smoothing filter, and speaker amplifier. A minimum record/playback subsystem can be configured with a microphone, a speaker, several passives, two push-buttons, and a power source.

Recordings are stored in on-chip nonvolatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through ISD's patented multilevel storage technology. Voice and audio signals are stored directly into memory in their natural form, providing high-quality, solid-state voice reproduction.

Figure: ISD1400 Series Block Diagram



FEATURES

- Easy-to-use single-chip voice record/playback solution
- High-quality, natural voice/audio reproduction
- Push-button interface
  - Playback can be edge- or level-activated
- Single-chip durations of 16 and 20 seconds
- Automatic power-down mode
  - Enters standby mode immediately following a record or playback cycle
  - Standby current 0.5 μA (typical)
- Zero-power message storage
  - Eliminates battery backup circuits
- Fully addressable to handle multiple messages
- 100-year message retention (typical)
- 100,000 record cycles (typical)
- On-chip clock source
- No programmer or development system needed
- Single +5 volt power supply
- Available in die form, DIP, and SOIC packaging
- Industrial temperature (–40°C to +85°C) versions available

Table: ISD1400 Series Summary

Part Number	Minimum Duration (Seconds)	Input Sample Rate (KHz)	Typical Filter Pass Band (KHz)
ISD1416	16	8.0	3.3
ISD1420	20	6.4	2.6

Table of Contents

ISD1400 Series

Single-Chip Voice Record/Playback Devices
16- and 20-Second Durations

FIGURES, CHARTS, AND TABLES IN THE ISD1400 SERIES DATASHEET

DETAILED DESCRIPTION

SPEECH/SOUND QUALITY

The ISD1400 series includes devices offered at 6.4 and 8.0 KHz sampling frequencies, allowing the user a choice of speech quality options. The speech samples are stored directly into on-chip nonvolatile memory without the digitization and compression associated with other solutions. Direct analog storage provides a very true, natural sounding reproduction of voice, music, tones, and sound effects not available with most solid-state digital solutions.

DURATION

To meet end system requirements, the ISD1400 series offers single-chip solutions at 16 and 20 seconds.

EEPROM STORAGE

One of the benefits of ISD's ChipCorder technology is the use of on-chip nonvolatile memory, providing zero-power message storage. The message is retained for up to 100 years typically without power. In addition, the device can be re-recorded typically over 100,000 times.

BASIC OPERATION

The ISD1400 ChipCorder series devices are controlled by a single record signal, $\overline{\text{REC}}$, and either of two push-button control playback signals, $\overline{\text{PLAYE}}$ (edge-activated playback), and $\overline{\text{PLAYL}}$ (level-activated playback). The ISD1400 parts are configured for simplicity of design in a single-message application. Using the address lines will allow multiple message applications. Device operation is explained on page 15.

AUTOMATIC POWER-DOWN MODE

At the end of a playback or record cycle, the ISD1400 series devices automatically return to a low-power standby mode, consuming typically 0.5 μA. During a playback cycle, the device powers down automatically at the end of the message. During a record cycle, the device powers down immediately after $\overline{\text{REC}}$ is released HIGH.

ADDRESSING (OPTIONAL)

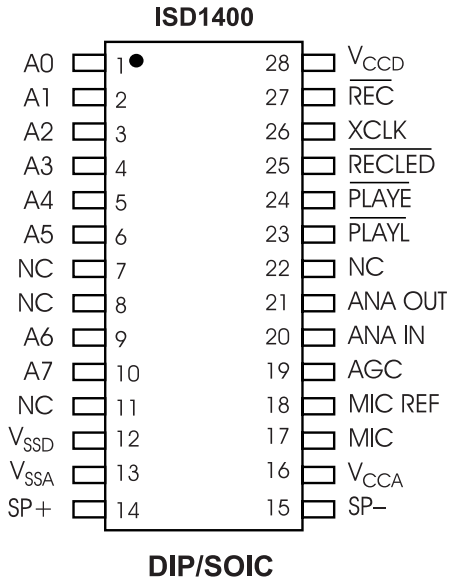
In addition to providing simple message playback, the ISD1400 series provides a full addressing capability.

The ISD1400 series storage array has 160 distinct addressable segments, providing the following resolutions. See Application Information for ISD1400 address tables.

Table 1: Device Playback/Record Durations

Part Number	Minimum Duration (Seconds)
ISD1416	100 ms
ISD1420	125 ms

Figure 1: ISD1400 Series Pinouts



NOTE: *NC means must Not Connect.*

PIN DESCRIPTION

NOTE *The $\overline{REC}$ signal is debounced for 50 ms on the rising edge to prevent a false retriggering from a push-button switch.*

VOLTAGE INPUTS (V_{CCA} , V_{CCD})

Analog and digital circuits internal to the ISD1400 series use separate power buses to minimize noise on the chip. These power buses are brought out to separate pins on the package and should be tied together as close to the supply as possible. It is important that the power supply be decoupled as close as possible to the package.

GROUND INPUTS (V_{SSA} , V_{SSD})

Similar to V_{CCA} and V_{CCD}, the analog and digital circuits internal to the ISD1400 series use separate ground buses to minimize noise. These pins should be tied together as close as possible to the device.

RECORD (REC)

The $\overline{REC}$ input is an active-LOW record signal. The device records whenever $\overline{REC}$ is LOW. This signal must remain LOW for the duration of the recording. $\overline{REC}$ takes precedence over either playback ($\overline{PLAYE}$ or $\overline{PLAYL}$) signal. If $\overline{REC}$ is pulled LOW during a playback cycle, the playback immediately ceases and recording begins.

A record cycle is completed when $\overline{REC}$ is pulled HIGH or the memory space is filled.

An end-of-message marker (EOM) is internally recorded, enabling a subsequent playback cycle to terminate appropriately. The device automatically powers down to standby mode when $\overline{REC}$ goes HIGH.

PLAYBACK, EDGE-ACTIVATED (PLAYE)

When a LOW-going transition is detected on this input signal, a playback cycle begins. Playback continues until an EOM is encountered or the end of the memory space is reached. Upon completion of the playback cycle, the device automatically powers down into standby mode. Taking $\overline{PLAYE}$ HIGH during a playback cycle will not terminate the current cycle.

PLAYBACK, LEVEL-ACTIVATED (PLAYL)

When this input signal transitions from HIGH to LOW, a playback cycle is initiated. Playback continues until $\overline{PLAYL}$ is pulled HIGH, an EOM marker is detected, or the end of the memory space is reached. The device automatically powers down to standby mode upon completion of the playback cycle.

NOTE *In playback, if either $\overline{PLAYE}$ or $\overline{PLAYL}$ is held LOW during EOM or OVF, the device will still enter standby and the internal oscillator and timing generator will stop. However, the rising edge of $\overline{PLAYE}$ and $\overline{PLAYL}$ are not debounced and any subsequent falling edge (particularly switch bounce) present on the input pins will initiate another playback.*

RECORD LED OUTPUT ($\overline{\text{RECLED}}$)

The output $\overline{\text{RECLED}}$ is LOW during a record cycle. It can be used to drive an LED to provide feedback that a record cycle is in progress. In addition, $\overline{\text{RECLED}}$ pulses LOW momentarily when an EOM is encountered in a playback cycle.

MICROPHONE INPUT (MIC)

The microphone input transfers its signal to the on-chip preamplifier. An on-chip Automatic Gain Control (AGC) circuit controls the gain of this preamplifier from –15 to 24 dB. An external microphone should be AC coupled to this pin via a series capacitor. The capacitor value, together with the internal 10 KΩ resistance on this pin, determine the low-frequency cutoff for the ISD1400 series passband. See Application Information for additional information on low-frequency cutoff calculations.

MICROPHONE REFERENCE (MIC REF)

The MIC REF input is the inverting input to the microphone preamplifier. This provides a noise-canceling or common-mode rejection input to the device when connected differentially to a microphone.

AUTOMATIC GAIN CONTROL (AGC)

The AGC dynamically adjusts the gain of the preamplifier to compensate for the wide range of microphone input levels. The AGC allows the full range of sound, from whispers to loud sounds, to be recorded with minimal distortion. The "attack" time is determined by the time constant of a 5 KΩ internal resistance and an external capacitor (C6 on the schematic in Figure 4) connected from the AGC pin to V_{SSA} analog ground. The "release" time is determined by the time constant of an external resistor (R5) and an external capacitor (C6) connected in parallel between the AGC Pin and V_{SSA} analog ground. Nominal values of 470 KΩ and 4.7 µF give satisfactory results in most cases.

ANALOG OUTPUT (ANA OUT)

This pin provides the preamplifier output to the user. The voltage gain of the preamplifier is determined by the voltage level at the AGC pin.

ANALOG INPUT (ANA IN)

The ANA IN pin transfers the input signal to the chip for recording. For microphone inputs, the ANA OUT pin should be connected via an external capacitor to the ANA IN pin. This capacitor value, together with the 3.0 KΩ input impedance of ANA IN, is selected to give additional cutoff at the low-frequency end of the voice passband. If the desired input is derived from a source other than a microphone, the signal can be fed, capacitively coupled, into the ANA IN pin directly.

EXTERNAL CLOCK INPUT (XCLK)

The external clock input for the ISD1400 devices has an internal pull-down device. The ISD1400 is configured at the factory with an internal sampling clock frequency that guarantees its minimum nominal record/playback time. For instance, an ISD1420 operating within specification will be observed to always have a minimum of 20 seconds of recording time. The sampling frequency is then maintained to a variation of ±2.25 percent over the commercial temperature and operating voltage ranges, while still maintaining the minimum specified recording duration. This will result in some devices having a few percent more than nominal recording time.

The internal clock has a ±5 percent tolerance over the industrial temperature and voltage range. A regulated power supply is recommended for industrial temperature parts. If greater precision is required, the device can be clocked through the XCLK pin as follows:

Table 2: External Clock Sample Rates

Part Number	Sample Rate	Required Clock
ISD1416	8.0 KHz	1024 KHz
ISD1420	6.4 KHz	819.2 KHz

These recommended clock rates should not be varied because the antialiasing and smoothing filters are fixed, and aliasing problems can occur if the sample rate differs from the one recommended. The duty cycle on the input clock is not critical, as the clock is immediately divided by two internally. **If the XCLK is not used, this input should be connected to ground.**

SPEAKER OUTPUTS (SP+, SP–)

The SP+ and SP– pins provide direct drive for loudspeakers with impedances as low as 16 Ω. A single output may be used, but, for direct-drive loudspeakers, the two opposite-polarity outputs provide an improvement in output power of up to four times over a single-ended connection. Furthermore, when SP+ and SP– are used, a speaker-coupling capacitor is not required. A single-ended connection will require an AC-coupling capacitor between the SP pin and the speaker. The speaker outputs are in a high-impedance state during a record cycle, and held at V_{SSA} during power down.

ADDRESS INPUTS (A0–A7)

The Address Inputs have two functions, depending upon the level of the two Most Significant Bits (MSB) of the address.

If either of the two MSBs is LOW, the inputs are all interpreted as address bits and are used as the start address for the current record or playback cycle. The address pins are inputs only and do not output internal address information as the operation progresses. Address inputs are latched by the falling edge of $\overline{\text{PLAYE}}$, $\overline{\text{PLAYL}}$, or $\overline{\text{REC}}$.

OPERATIONAL MODES

The ISD1400 series is designed with several built-in operational modes provided to allow maximum functionality with a minimum of additional components, described in detail below. The operational modes use the address pins on the ISD1400 devices, but are mapped outside the valid address range. When the two Most Significant Bits (MSBs) are HIGH (A6 and A7), the remaining address signals are interpreted as mode bits and not as address bits. Therefore, operational modes and direct addressing are not compatible and cannot be used simultaneously.

There are two important considerations for using operational modes. First, all operations begin initially at address 0, which is the beginning of the ISD1400 address space. Later operations can begin at other address locations, depending on the operational mode(s) chosen. In addition, the address pointer is reset to 0 when the device is changed from record to playback but not from playback to record when A4 is HIGH in Operational Mode.

Second, an Operational Mode is executed when any of the control inputs, $\overline{\text{PLAYE}}$, $\overline{\text{PLAYL}}$, or $\overline{\text{REC}}$, go LOW and the two MSBs are HIGH. This Operational Mode remains in effect until the next LOW-going control input signal, at which point the current address/mode levels are sampled and executed.

NOTE *The two MSBs are on pins 9 and 10 for each ISD1400 series device.*

OPERATIONAL MODES DESCRIPTION

The Operational Modes can be used in conjunction with a microcontroller, or they can be hardwired to provide the desired system operation.

A0 — MESSAGE CUEING

Message Cueing allows the user to skip through messages, without knowing the actual physical addresses of each message. Each control input LOW pulse causes the internal address pointer to skip to the next message. This mode should be used for playback only, and is typically used with the A4 Operational Mode.

A1 — DELETE $\overline{\text{EOM}}$ MARKERS

The A1 Operational Mode allows sequentially recorded messages to be combined into a single message with only one EOM marker set at the end of the final message. When this operational mode is configured, messages recorded sequentially are played back as one continuous message.

A2 — UNUSED

A3 — MESSAGE LOOPING

The A3 Operational Mode allows for the automatic, continuously repeated playback of the message located at the beginning of the address space.

A message can completely fill the ISD1400 device and will loop from beginning to end. Pulsing $\overline{\text{PLAYE}}$ will start the playback and pulsing $\overline{\text{PLAYL}}$ will end the playback.

A4 — CONSECUTIVE ADDRESSING

During normal operations, the address pointer will reset when a message is played through to an EOM marker. The A4 Operational Mode inhibits the address pointer reset, allowing messages to be recorded or played back consecutively. When the device is in a static state; i.e., not recording or playing back, momentarily taking this pin LOW will reset the address counter to zero.

A5 — UNUSED

Table 3: Operational Modes Table

Address Crtl. (HIGH)	Function	Typical Use	Jointly Compatible[1]
A0	Message cueing	Fast-forward through messages	A4
A1	Delete EOM markers	Position EOM marker at the end of the last message	A3, A4
A2	Unused		
A3	Looping	Continuous playback from Address 0	A1
A4	Consecutive addressing	Record/play multiple consecutive messages	A0, A1
A5	Unused		

1. *Additional operational modes can be used simultaneously with the given mode.*

TIMING DIAGRAMS

Figure 2: Record

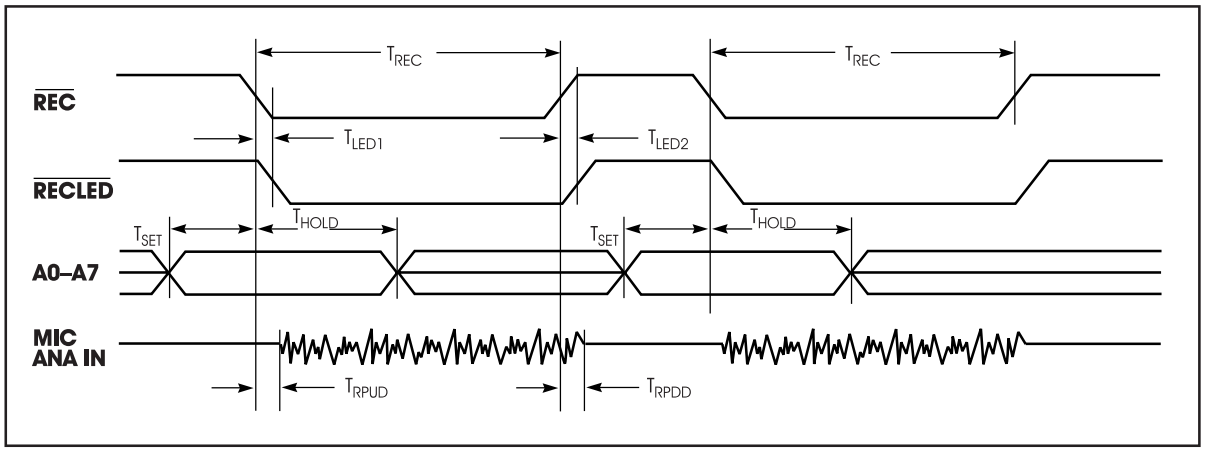
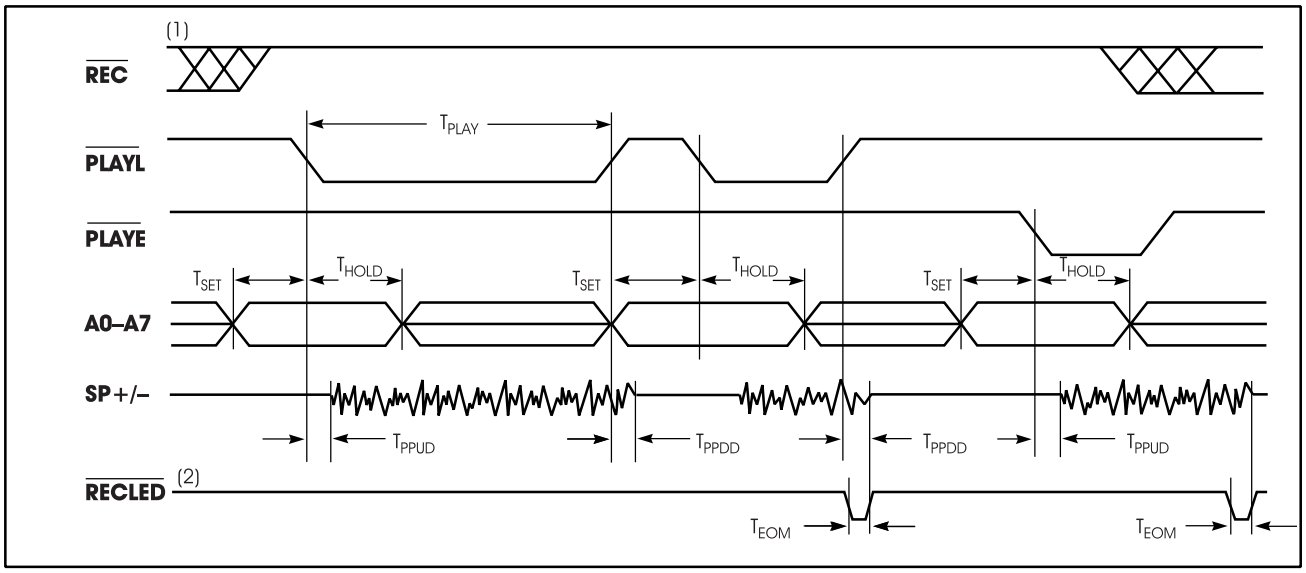


Figure 3: Playback



1. *$\overline{REC}$ must be HIGH for the entire duration of a playback cycle.*
2. *$\overline{RECLED}$ functions as an EOM during playback.*

Table 4: Absolute Maximum Ratings (Packaged Parts)[1]

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to any pin	(V_{SS} – 0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pin (Input current limited to ±20 mA)	(V_{SS} – 1.0 V) to (V_{CC} + 1.0 V)
Lead temperature (soldering – 10 seconds)	300°C
V_{CC} – V_{SS}	–0.3 V to +7.0 V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

Table 5: Operating Conditions (Packaged Parts)

Condition	Value
Commercial operating temperature range[1]	0°C to +70°C
Industrial operating temperature[1]	–40°C to +85°C
Supply voltage (V_{CC})[2]	+4.5 V to +5.5 V
Ground voltage (V_{SS})[3]	0 V

1. *Case temperature.*
2. $V_{CC} = V_{CCA} = V_{CCD}$.
3. $V_{SS} = V_{SSA} = V_{SSD}$.

Table 6: DC Parameters (Packaged Parts)

Symbol	Parameters	Min[2]	Typ [1]	Max[2]	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.4			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –1.6 mA
I_{CC}	V_{CC} Current (Operating)		15	30	mA	V_{CC} = 5.5 V [3], R_{EXT} = ∞
I_{SB}	V_{CC} Current (Standby)		0.5	10	µA	[3] [4]
I_{IL}	Input Leakage Current			±1	µA	
I_{ILPD}	Input Current HIGH w/Pull Down			130	µA	Force V_{CC} [5]
R_{EXT}	Output Load Impedance	16			Ω	Speaker Load
R_{MIC}	Preamp In Input Resistance	4	9	17	KΩ	Pins 17, 18
$R_{ANA\ IN}$	ANA IN Input Resistance	2.5	3	5	KΩ	
A_{PRE1}	Preamp Gain 1	20	23	26	dB	AGC = 0.0 V
A_{PRE2}	Preamp Gain 2		–45	–15	dB	AGC = 2.5 V

Table 6: DC Parameters (Packaged Parts)

Symbol	Parameters	Min(2)	Typ (1)	Max(2)	Units	Conditions
A_{ARP}	ANA IN to SP+/– Gain	20	22	25	dB	
R_{AGC}	AGC Output Resistance	2.5	5	9.5	KΩ	
I_{PREH}	Preamp Out Source		–2		mA	@ V_{OUT} = 1.0 V
I_{PREL}	Preamp In Sink		0.5		mA	@ V_{OUT} = 2.0 V

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *V_{CCA} and V_{CCD} connected together.*
4. *$\overline{REC}$, $\overline{PLAYL}$, and $\overline{PLAYE}$ must be at V_{CCD}.*
5. *XCLK pin.*

Table 7: AC Parameters (Packaged Parts)

Symbol	Characteristic		Min(2)	Typ (1)	Max(2)	Units	Conditions
F_S	Sampling Frequency	ISD1416 ISD1420			8 6.4	KHz KHz	(5) (5)
F_{CF}	Filter Pass Band	ISD1416 ISD1420		3.3 2.6		KHz KHz	3 dB Roll-Off Point (3)(6) 3 dB Roll-Off Point (3)(6)
T_{REC}	Record Duration	ISD1416 ISD1420	16 20			sec sec	
T_{PLAY}	Playback Duration	ISD1416 ISD1420	16 20			sec sec	(5) (5)
T_{LED1}	$\overline{RECLED}$ ON Delay			5		msec	
T_{LED2}	$\overline{RECLED}$ OFF Delay	ISD1416 ISD1420	30 40	38.9 48.6	95 110	msec msec	
T_{SET}	Address Setup Time		300			nsec	
T_{HOLD}	Address Hold Time		0			nsec	
T_{RPUD}	Record Power-Up Delay	ISD1416 ISD1420		26 32		msec msec	
T_{RPDD}	Record Power-Down Delay	ISD1416 ISD1420		26 32		msec msec	
T_{PPUD}	Play Power-Up Delay	ISD1416 ISD1420		26 32		msec msec	

Table 7: AC Parameters (Packaged Parts)

Symbol	Characteristic		Min(2)	Typ (1)	Max(2)	Units	Conditions
T_{PPDD}	Play Power-Down Delay	ISD1416 ISD1420		6.5 8.1		msec msec	
T_{EOM}	EOM Pulse Width	ISD1416 ISD1420		12.5 15.625		msec msec	
THD	Total Harmonic Distortion			1	3	%	@ 1 KHz
P_{OUT}	Speaker Output Power			12.2		mW	R_{EXT} = 16 Ω
V_{OUT}	Voltage Across Speaker Pins			1.25	2.5	V p–p	R_{EXT} = 600 Ω
V_{IN1}	MIC Input Voltage				20	mV	Peak-to-Peak (4)
V_{IN2}	ANA IN Input Voltage				50	mV	Peak-to-Peak

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *Low-frequency cutoff depends upon value of external capacitors (see Pin Descriptions).*
4. *With 5.1 KΩ series resistor at ANA IN.*
5. *Sampling frequency and playback duration will vary as much as ±2.25 percent over the commercial temperature and voltage ranges. It may vary as much as ±5 percent over the industrial temperature and voltage ranges. All devices will meet the maximum sampling frequency and minimum playback duration parameters. For greater stability, an external clock can be utilized (see Pin Descriptions).*
6. *Filter specification applies to the antialiasing filter and to the smoothing filter.*

TYPICAL PARAMETER VARIATION WITH VOLTAGE AND TEMPERATURE (PACKAGED PARTS)

Chart 1: Record Mode Operating Current (I_{CC})

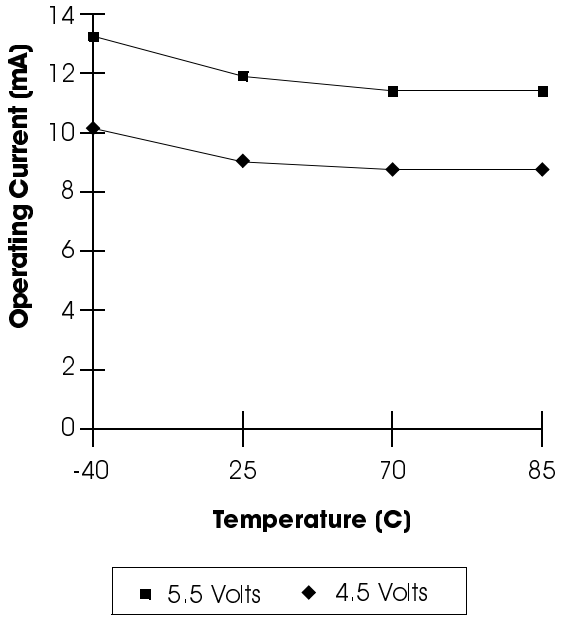


Chart 2: Total Harmonic Distortion

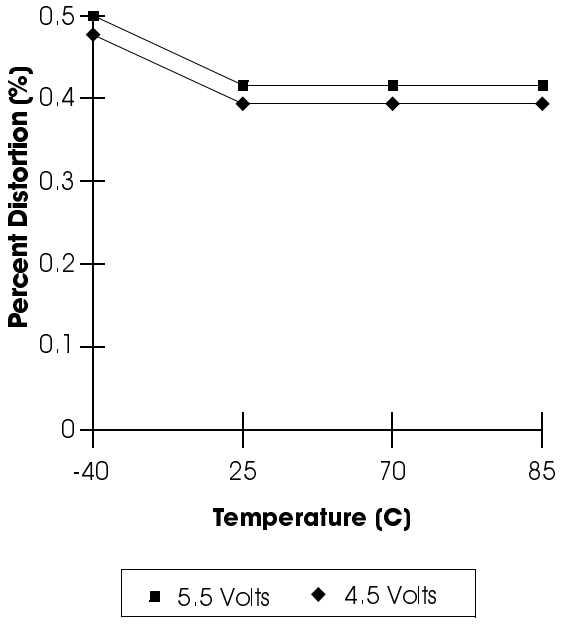


Chart 3: Standby Current (I_{SB})

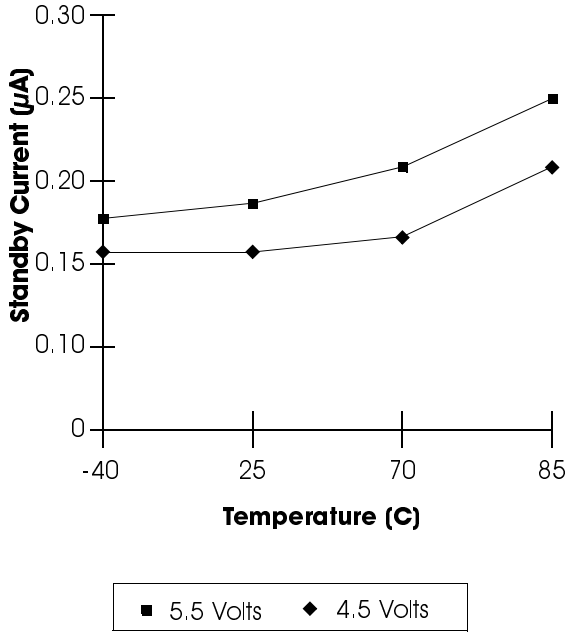


Chart 4: Oscillator Stability

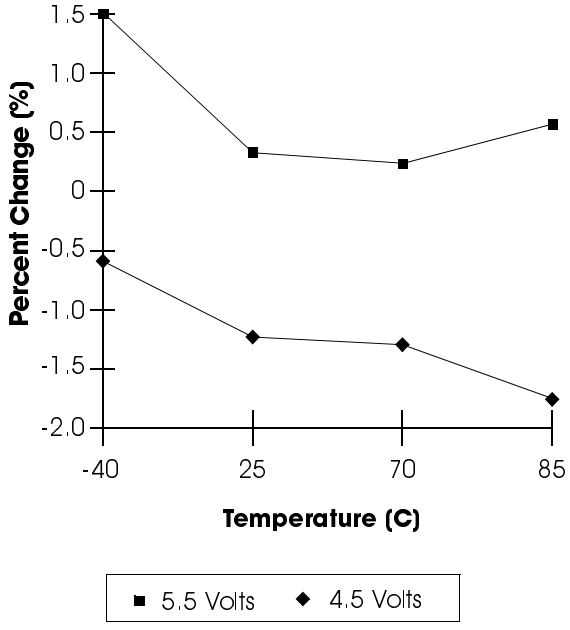


Table 8: Absolute Maximum Ratings (Die)[1]

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to any pad	(V_{SS} – 0.3V) to (V_{CC} + 0.3V)
Voltage applied to any pad (Input current limited to ±20 mA)	(V_{SS} – 1.0 V) to (V_{CC} + 1.0 V)
V_{CC} – V_{SS}	–0.3 V to +7.0 V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

Table 9: Operating Conditions (Die)

Condition	Value
Commercial operating temperature range	0°C to +50°C
Supply voltage (V_{CC})[1]	+4.5 V to +6.5 V
Ground voltage (V_{SS})[2]	0 V

1. $V_{CC} = V_{CCA} = V_{CCD}$.
2. $V_{SS} = V_{SSA} = V_{SSD}$.

Table 10: DC Parameters (Die)

Symbol	Parameters	Min[2]	Typ [1]	Max[2]	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.4			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –1.6 mA
I_{CC}	V_{CC} Current (Operating)		15	30	mA	V_{CC} = 5.5 V [3], R_{EXT} = ∞
I_{SB}	V_{CC} Current (Standby)		0.5	10	µA	[3] [4]
I_{IL}	Input Leakage Current			±1	µA	
I_{ILPD}	Input Current HIGH w/Pull Down			130	µA	Force V_{CC} [5]
R_{EXT}	Output Load Impedance	16			Ω	Speaker Load
R_{MIC}	Preamp In Input Resistance	4	9	17	KΩ	Pins 17, 18
$R_{ANA\ IN}$	ANA IN Input Resistance	2.5	3	5	KΩ	
A_{PRE1}	Preamp Gain 1	20	23	26	dB	AGC = 0.0 V
A_{PRE2}	Preamp Gain 2		–45	–15	dB	AGC = 2.5 V
A_{ARP}	ANA IN to SP+/– Gain	20	22	25	dB	

Table 10: DC Parameters (Die)

Symbol	Parameters	Min(2)	Typ (1)	Max(2)	Units	Conditions
R_{AGC}	AGC Output Resistance	2.5	5	9.5	KΩ	
I_{PREH}	Preamp Out Source		–2		mA	@ V_{OUT} = 1.0 V
I_{PREL}	Preamp In Sink		0.5		mA	@ V_{OUT} = 2.0 V

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *V_{CCA} and V_{CCD} connected together.*
4. *$\overline{REC}$, $\overline{PLAYL}$, and $\overline{PLAYE}$ must be at V_{CCD} .*
5. *XCLK pin.*

Table 11: AC Parameters (Die)

Symbol	Characteristic		Min(2)	Typ (1)	Max(2)	Units	Conditions
F_S	Sampling Frequency	ISD1416 ISD1420			8 6.4	KHz KHz	(5) (5)
F_{CF}	Filter Pass Band	ISD1416 ISD1420		3.3 2.6		KHz KHz	3 dB Roll-Off Point (3)(6) 3 dB Roll-Off Point (3)(6)
T_{REC}	Record Duration	ISD1416 ISD1420	16 20			sec sec	
T_{PLAY}	Playback Duration	ISD1416 ISD1420	16 20			sec sec	(5) (5)
T_{LED1}	$\overline{RECLED}$ ON Delay			5		msec	
T_{LED2}	$\overline{RECLED}$ OFF Delay	ISD1416 ISD1420	30 40	38.9 48.6	95 110	msec msec	
T_{SET}	Address Setup Time		300			nsec	
T_{HOLD}	Address Hold Time		0			nsec	
T_{RPUD}	Record Power-Up Delay	ISD1416 ISD1420		26 32		msec msec	
T_{RPDD}	Record Power-Down Delay	ISD1416 ISD1420		26 32		msec msec	
T_{PPUD}	Play Power-Up Delay	ISD1416 ISD1420		26 32		msec msec	

Table 11: AC Parameters (Die)

Symbol	Characteristic		Min(2)	Typ (1)	Max(2)	Units	Conditions
T_{PPDD}	Play Power-Down Delay	ISD1416 ISD1420		6.5 8.1		msec msec	
T_{EOM}	EOM Pulse Width	ISD1416 ISD1420		12.5 15.625		msec msec	
THD	Total Harmonic Distortion			1	3	%	@ 1 KHz
P_{OUT}	Speaker Output Power			12.2		mW	R_{EXT} = 16 Ω
V_{OUT}	Voltage Across Speaker Pins			1.25	2.5	V p–p	R_{EXT} = 600 Ω
V_{IN1}	MIC Input Voltage				20	mV	Peak-to-Peak (4)
V_{IN2}	ANA IN Input Voltage				50	mV	Peak-to-Peak

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *Low-frequency cutoff depends upon value of external capacitors (see Pin Descriptions).*
4. *With 5.1 KΩ series resistor at ANA IN.*
5. *Sampling frequency and playback duration will vary as much as ±2.25 percent over the commercial temperature and voltage ranges. All devices will meet the maximum sampling frequency and minimum playback duration parameters. For greater stability, an external clock can be utilized (see Pin Descriptions).*
6. *Filter specification applies to the antialiasing filter and to the smoothing filter.Typical Parameter Variation with Voltage and Temperature (Die).*

TYPICAL PARAMETER VARIATION WITH VOLTAGE AND TEMPERATURE (DIE)

Chart 5: Record Mode Operating Current (I_{CC})

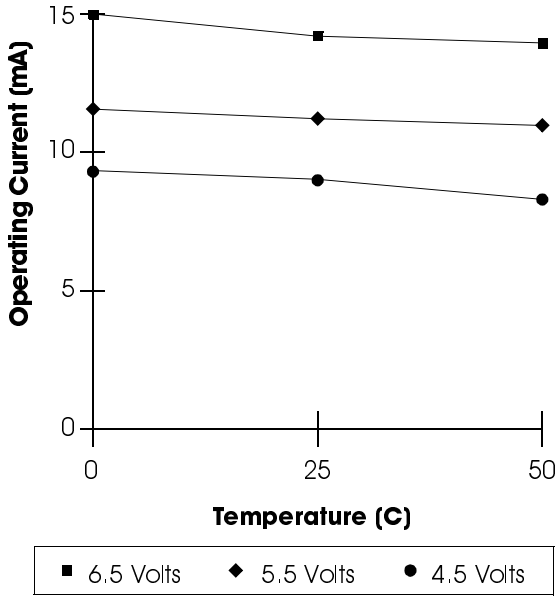


Chart 6: Total Harmonic Distortion

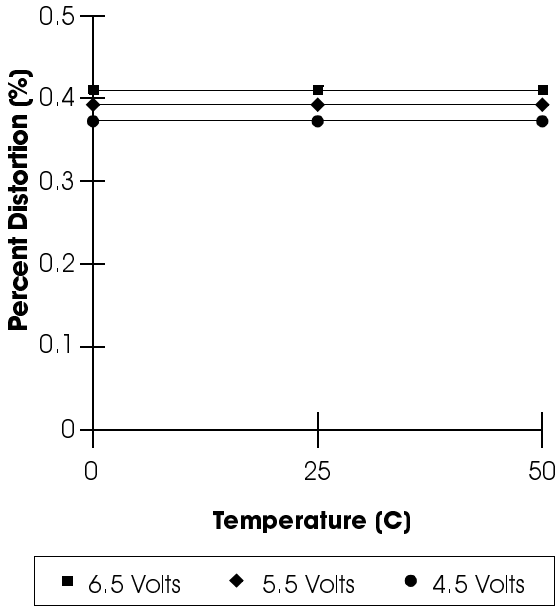


Chart 7: Standby Current (I_{SB})

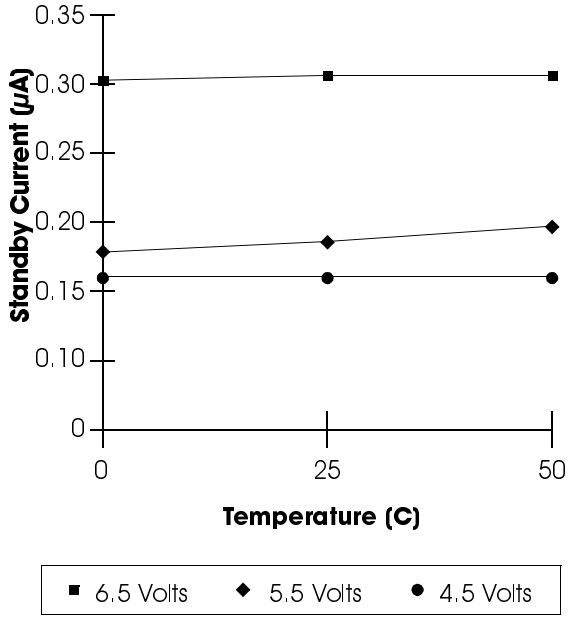


Chart 8: Oscillator Stability

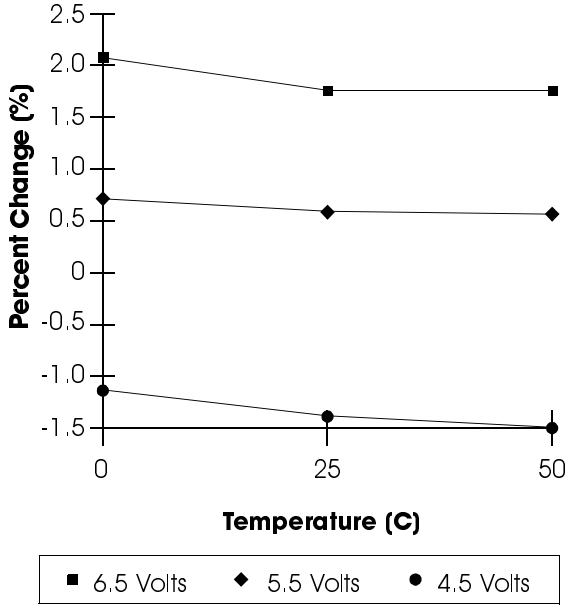
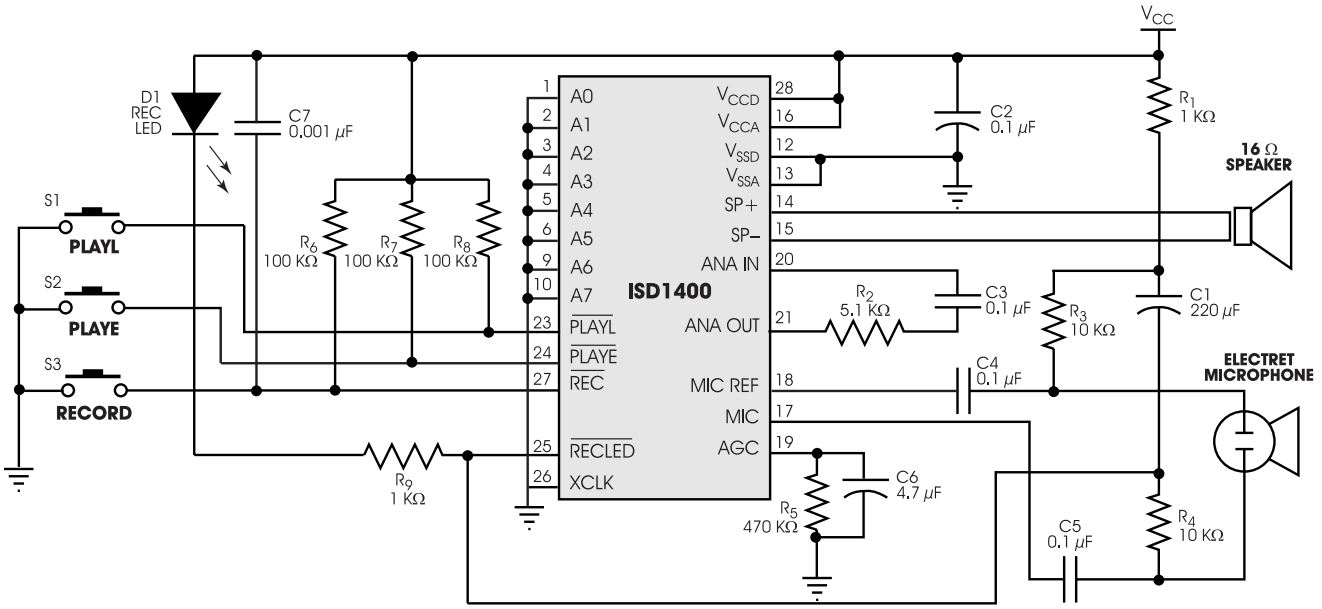


Figure 4: Application Example



FUNCTIONAL DESCRIPTION EXAMPLE

The following example operating sequence demonstrates the functionality of the ISD1400 series devices.

1. Record a message filling the address space.

   Pulling the $\overline{\text{REC}}$ signal LOW initiates a record cycle from the beginning of the message space. If $\overline{\text{REC}}$ is held LOW, the recording continues until the message space has been filled. Once the message space is filled, recording ceases. The device will automatically power down after $\overline{\text{REC}}$ is pulled HIGH.

2. Edge-activated playback.

   Pulling the $\overline{\text{PLAYE}}$ signal LOW initiates a playback cycle from the beginning of the message space or at a selected location. The rising edge of $\overline{\text{PLAYE}}$ has no effect on operation. If a recording has filled the message space, the entire message is played. When the device reaches the EOM marker, it automatically powers down. A subsequent falling edge on $\overline{\text{PLAYE}}$ initiates a new play cycle from the start address.

3. Level-activated playback.

   Pulling the $\overline{\text{PLAYL}}$ signal LOW initiates a playback cycle from the beginning of the message space or a selected location. If recording has filled the message space, the entire message is played. When the device reaches the EOM marker, it automatically powers down. A subsequent falling edge on $\overline{\text{PLAYL}}$ initiates a new play cycle from the starting address.

4. Level-activated playback (truncated).

   If $\overline{\text{PLAYL}}$ is pulled HIGH any time during the playback cycle, the device stops playing and enters the power-down mode. A subsequent falling edge on $\overline{\text{PLAYL}}$ initiates a new play cycle from the start address.

5. Record (interrupting playback).

   The $\overline{\text{REC}}$ signal takes precedence over other operations. Any LOW-going transition

on $\overline{REC}$ initiates a new record operation from the beginning of the start address or at a selected location, regardless of any current operation in progress.

6. Record a message, partially filling the address space.

   A record operation need not fill the entire message space. Releasing the $\overline{REC}$ signal HIGH before filling the message space causes the recording to stop and an EOM to be placed. The device powers down automatically.

7. Play back a message, partially filling the address space.

   Pulling the $\overline{PLAYE}$ or $\overline{PLAYL}$ signal LOW initiates a playback cycle which is then completed when the EOM marker is encountered. Playback ceases and the device powers down.

8. $\overline{RECLED}$ operation.

   The $\overline{RECLED}$ output pin provides an active-LOW signal which can be used to drive an LED as a "record-in-progress" indicator. It returns to a HIGH state when the $\overline{REC}$ pin is released HIGH or when the recording is completed due to the message space being filled. This pin also pulses LOW to indicate an EOM at the end of a message being played.

APPLICATIONS NOTE

Some users may experience an unexpected recording taking place when their circuit is powered up, or the batteries are changed and V_{CC} rises faster than $\overline{REC}$. This undesired recording prevents playback of the previously recorded message. A spurious End Of Message (EOM) marker appears at the very beginning of the memory, preventing access to the original message, and nothing is played.

To prevent this occurrence, place a capacitor (approx. 0.001 μF) between the control pin ($\overline{REC}$) and V_{CC}. This pulls the control pin voltage up with V_{CC} as it rises. Once the voltage is HIGH, the pull-up device will keep the pin HIGH until intentionally pulled LOW, preventing the false EOM marker.

Since this anomaly depends on factors such as the capacitance of the user's printed circuit board, not all circuit designs will exhibit the spurious marker. However, it is recommended that the capacitor is included for design reliability. A more detailed explanation and resolution of this occurrence is described in Application Information.

ISD1400 SERIES PHYSICAL DIMENSIONS

Figure 5: 28-Lead 0.600-Inch Plastic Dual Inline Package (PDIP) (P)

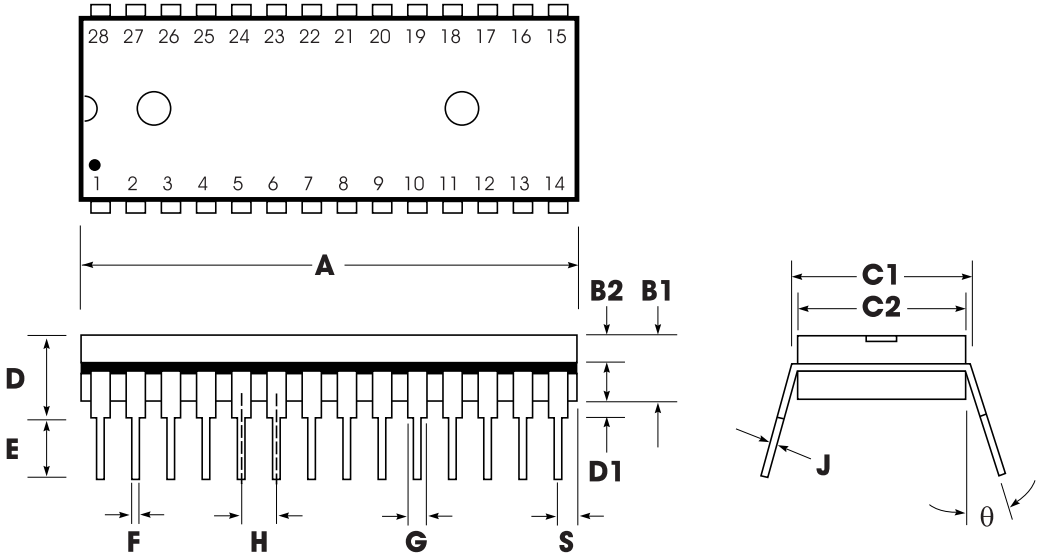


Table 12: Plastic Dual Inline Package (PDIP) (P) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	1.445	1.450	1.455	36.70	36.83	36.96
B1		0.150			3.81	
B2	0.065	0.070	0.075	1.65	1.78	1.91
C1	0.600		0.625	15.24		15.88
C2	0.530	0.540	0.550	13.46	13.72	13.97
D			0.19			4.83
D1	0.015			0.38		
E	0.125		0.135	3.18		3.43
F	0.015	0.018	0.022	0.38	0.46	0.56
G	0.055	0.060	0.065	1.40	1.52	1.65
H		0.100			2.54	
J	0.008	0.010	0.012	0.20	0.25	0.30
S	0.070	0.075	0.080	1.78	1.91	2.03
q	0°		15°	0°		15°

NOTE: *Lead coplanarity to be within 0.005 inches.*

Figure 6: 28-Lead 0.300-Inch Plastic Small Outline Integrated Circuit (SOIC) (S)

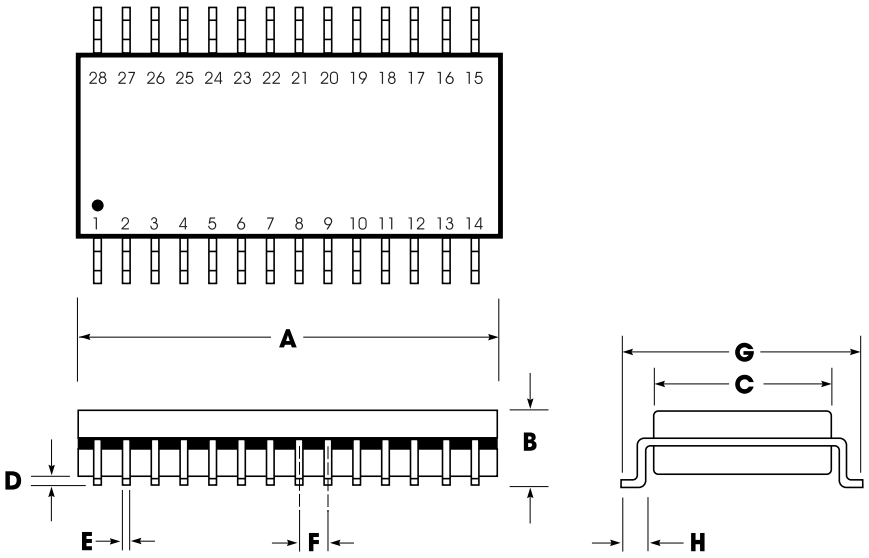


Table 13: Plastic Small Outline Integrated Circuit (SOIC) (S) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.701	0.706	0.711	17.81	17.93	18.06
B	0.097	0.101	0.104	2.46	2.56	2.64
C	0.292	0.296	0.299	7.42	7.52	7.59
D	0.005	0.009	0.0115	0.127	0.22	0.29
E	0.014	0.016	0.019	0.35	0.41	0.48
F		0.050			1.27	
G	0.400	0.406	0.410	10.16	10.31	10.41
H	0.024	0.032	0.040	0.61	0.81	1.02

NOTE: *Lead coplanarity to be within 0.004 inches.*

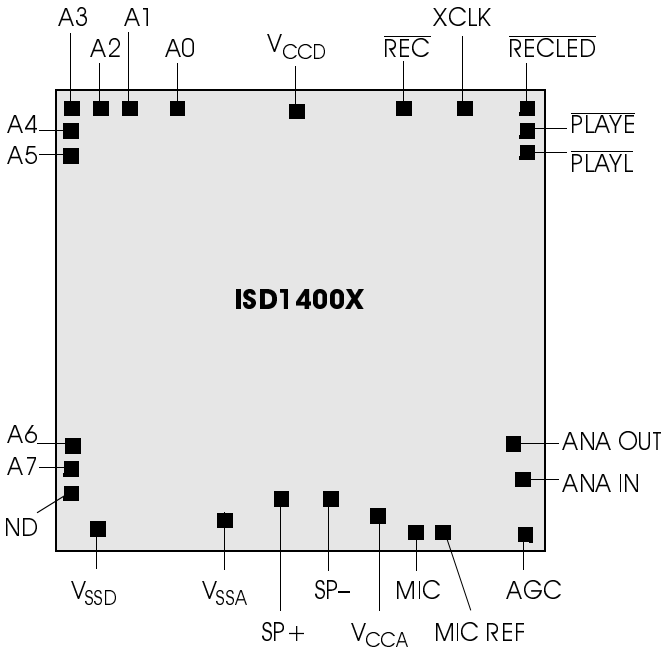
Figure 7: ISD1400 Series Bonding Physical Layout[1]

ISD1400X

I. Die Dimensions
X: 172.2 ±1 mils
Y: 168.5 ±1 mils

II. Die Thickness[(2)]
17.5 ±1 mils

III. Pad Opening
100 x 112 microns
3.9 x 4.4 mils



*1. The backside of die is internally connected to V_{SS}. It **MUST NOT** be connected to any other potential or damage may occur.*

2. Die thickness is subject to change, please contact ISD factory for status.

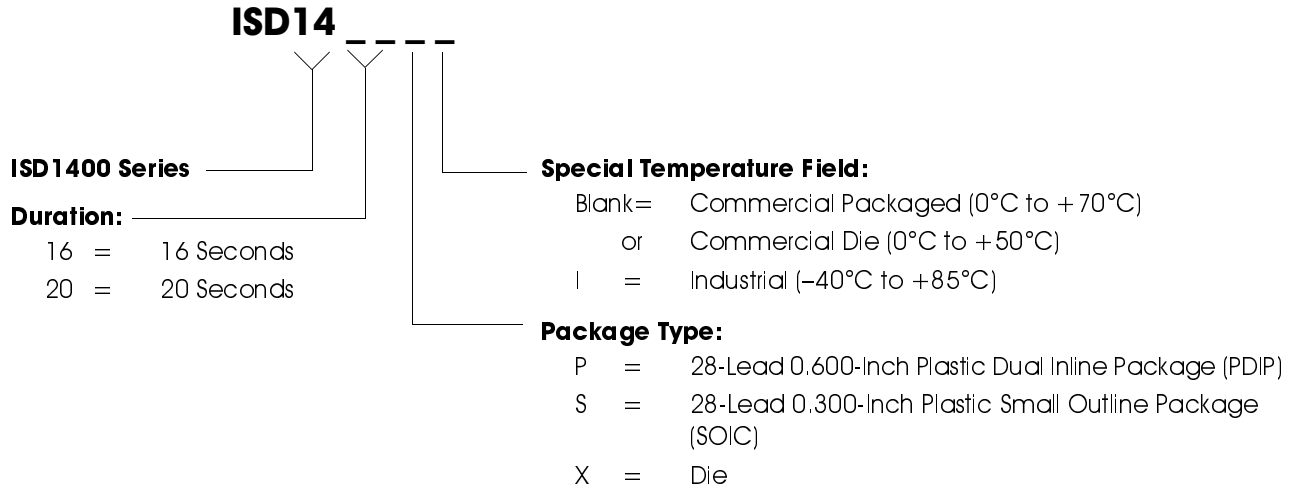
Table 14: ISD1400 Series PIN/PAD Designations, with Respect to Die Center (µm)

Pin	Pin Name	X Axis	Y Axis
A0	Address 0	–1332.5	1973.8
A1	Address 1	–1628.9	1973.8
A2	Address 2	–1808.9	1973.8
A3	Address 3	–2014.1	1910.2
A4	Address 4	–2014.1	1722.6
A5	Address 5	–2014.1	1519.8
A6	Address 6	–2014.1	–1214.6
A7	Address 7	–2014.1	–1399.8
NC	No Connect	–2014.1	–1745.4
V_{SSD}	V_{SS} Digital Power Supply	–1894.1	–1971.8
V_{SSA}	V_{SS} Analog Power Supply	–358.1	–1971.8
SP+	Speaker Output +	–17.7	–1896.6
SP–	Speaker Output –	411.9	–1896.6
V_{CCA}	V_{CC} Analog Power Supply	779.5	–1936.2
MIC	Microphone Input	991.5	–1973.8
MIC REF	Microphone Reference	1168.7	–1973.8
AGC	Automatic Gain Control	1977.9	–1910.6
ANA IN	Analog Input	2005.1	–1580.2
ANA OUT	Analog Output	1990.7	–1379.0
$\overline{\text{PLAYL}}$	Level-Activated Playback	2013.9	1608.6
$\overline{\text{PLAYE}}$	Edge-Activated Playback	2013.9	1777.0
$\overline{\text{RECLED}}$	Record LED Output	2011.9	1971.8
XCLK	No Connect (optional)	1580.7	1973.8
$\overline{\text{REC}}$	Record	752.3	1973.8
V_{CCD}	V_{CC} Digital Power Supply	–48.5	1929.4

NOTE: *Die dimensions and pin/pad positions may be subject to change. Please contact ISD Sales Offices or Representatives to verify current or future specifications.*

ORDERING INFORMATION

Product Number Descriptor Key



When ordering ISD1400 Series devices, please refer to the following valid part numbers.

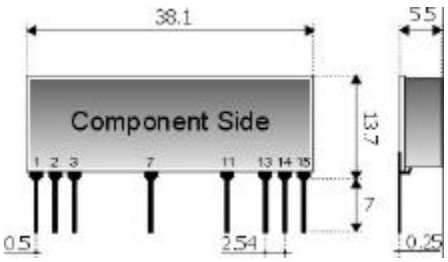
Part Number	Part Number
ISD1416P	ISD1420P
ISD1416PI	ISD1420PI
ISD1416S	ISD1420S
ISD1416SI	ISD1420SI
ISD1416X	ISD1420X

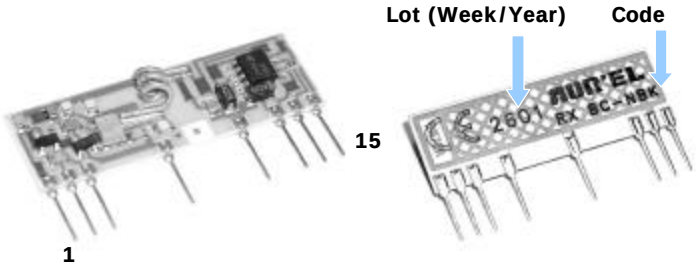
For the latest product information, access ISD's worldwide website at http://www.isd.com.

BC-NBK Receiver

Digital RF receiver, thick-film technology, with high sensitivity, low consumption and low antenna radiation.

Pin-out





Connections

Pin 2-7-11	**Ground**	GND Connections: Internally connected to a single ground plate.
Pin 3	**Antenna**	50Ω impedence, antenna connection
Pin 1-15	**+V**	Connection to the positive pole of supply (+5V ±10%)
Pin 13	**Test Point**	Analog output of the demodulated signal. By connecting an oscillograph, the entity and quality of the received RF signal can be seen.
Pin 14	**Data Out.**	Receiver digital output. Apply loads over 1 KΩ

Technical Features

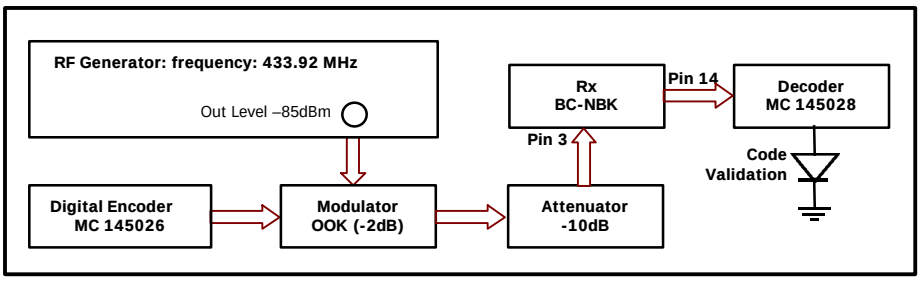
	Min	Typical	Max	Unity	Remarks
Working centre frequency		433.92		MHz	
Voltage supply	4.5	5	5.5	V	
Absorbed current		2,7	3	mA	
RF sensitivity		-97		dBm	See note 1
RF passband at –3dB		2.4		MHz	
Output square wave		2		KHz	
Output low logic level			0.1	V	See note 4
Output high logic level	3.8			V	See note 4
RF spurious emissions in antenna		-65	-60	dBm	See note 2
Switch-on time			2	s	See note 3
Working temperature	-20		+80	°C	See Fig. 5
Dimensions	38.1 x 13.7 x 5.5 mm				

Note1: *Values have been obtained by applying the test system as per Fig. 1.*
Note2: *The R.F. emission measure has been obtained by connecting the spectrum analyser directly to RX's Pin 3.*
Note3: *By switch-on time is meant the time required by the receiver to acquire the declared characteristics from the very moment the power supply is applied.*
Note4: *Values obtained with 10KW maximum load applied.*

BC-NBK module was previously BZT approved by mean of Test Report obtained c/o the laboratory:
ISPT LAB RADIO – viale Europa 190, 00144 Roma.

The declared technical features have been obtained by applying the following test system:

Fig. 1



Device usage

In order to obtain the performances described in the technical specifications and to comply with the operating conditions which characterize the Certification, the receiver has to be fitted on a printed circuit, considering what follows:

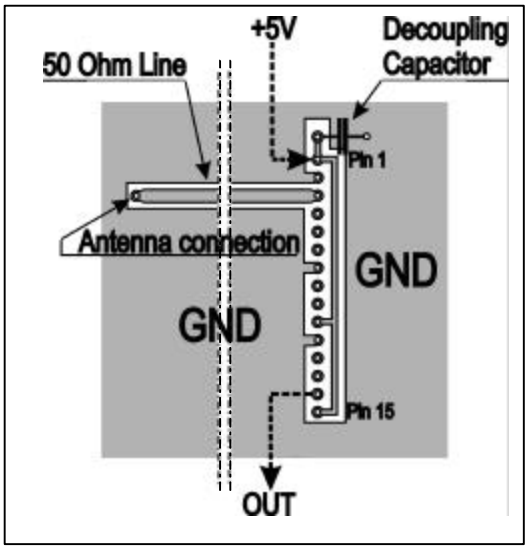
5 V dc supply:

1. The receiver must be supplied by a very low voltage source, safety protected against short circuits.
2. Maximum voltage variations allowed: ± 0,5 V.
3. De-coupling, next to the receiver, by means of a minimum 100.000 pF ceramic capacitor.

Ground:

1. It must surround at the best the welding area of the receiver. The circuit must be double layer, with throughout vias to the ground planes, approximately each 15 mm.
2. It must be properly dimensioned, specially in the antenna connection area, in case a radiating whip antenna is fitted, in it (an area of approximately 50 mm radius is suggested).

Fig. 3 Suggested lay-out for the device correct usage.



50 Ohm line:

1. It must be the shortest as possible.
2. 1,8 mm wide for 1 mm thick FR4 printed circuits and 2,9 mm wide for 1,6 mm thick FR4 printed circuits. On the same side, it must be kept 2 mm away from the ground circuit.
3. On the opposite side a ground circuit area must be present.

Antenna connection:

1. It may be utilized as the direct connection point for the radiating whip antenna.
2. It can bear the connection of the central wire of a 50 Ω coaxial cable. Be sure that the braid is welded to the ground in a close point.

Antenna

1. A **whip** antenna, 16,5 mm long and approximately 1 mm dia, brass or copper wire made, must be connected to the RF input of the receiver.
2. The antenna body must be keep straight as much as possible and it must be free from other circuits or metal parts (5 cm minimum suggested distance.)
3. It can be utilized both vertically or horizontally, provided that the connection point between antenna and receiver input, is surrounded by a good ground plane.

N.B: As an alternative to the a.m. antenna it is possible to utilize the whip model manufactured by **AUR°EL** (see related Data Sheet and Application Notes).
By fitting whips too different from the described ones, the EEC Certification is not assured.

Other components:

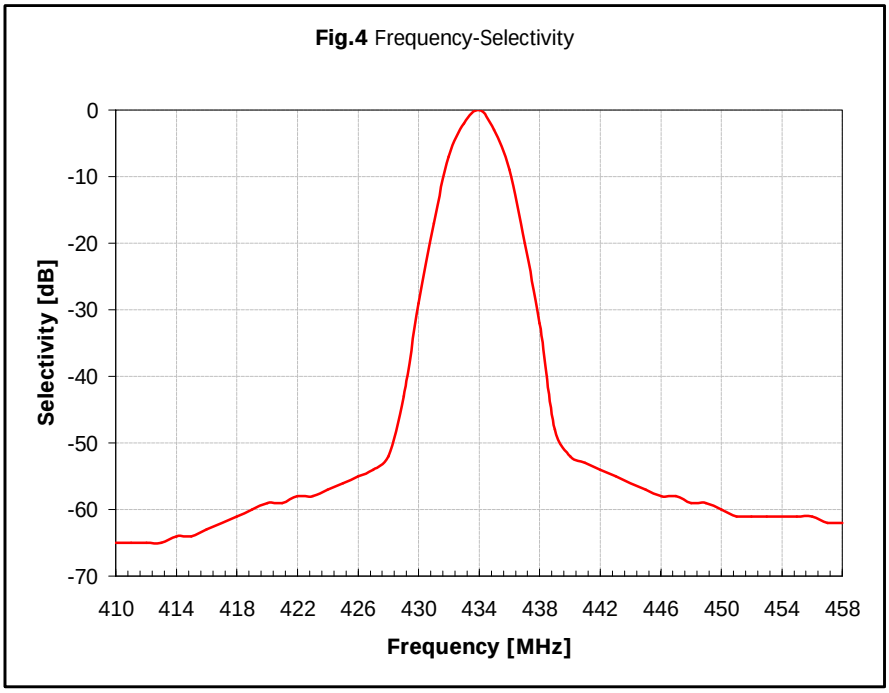
1. Keep the receiver separate from all other components of the circuit (more than 5 mm).
2. Keep particularly far away and shielded all microprocessors and their clock circuits.
3. Do not fit components around the 50 Ohm line. At least keep them at 5 mm distance.
4. If the Antenna Connection is directly used for a radiating whip connection, keep at least a 5 cm radius free area. In case of coaxial cable connection, then 5 mm radius will suffice.

Reference Rules

The **BC-NBK** receiver is EEC certified and in particular it complies with the European Rules **EN 300 220-3,** and **EN 301 489-3 for class 3.** The equipment has been tested according to rule **EN 60950** and it can be utilized inside a special insulated housing that assures the compliance with the above mentioned rule. The receiver must be supplied by a very low voltage source, safety protected against short circuits. The use of the receiver module is foreseen inside housings that assure the overcoming of the rule **EN 61000-4-2** not directly applicable to the module itself. In particular, it is at the user's care the insulation of the external antenna connection, and of the antenna itself since the RF output of the receiver is not built to directly bear the electrostatic charges foreseen by the a.m. rules.

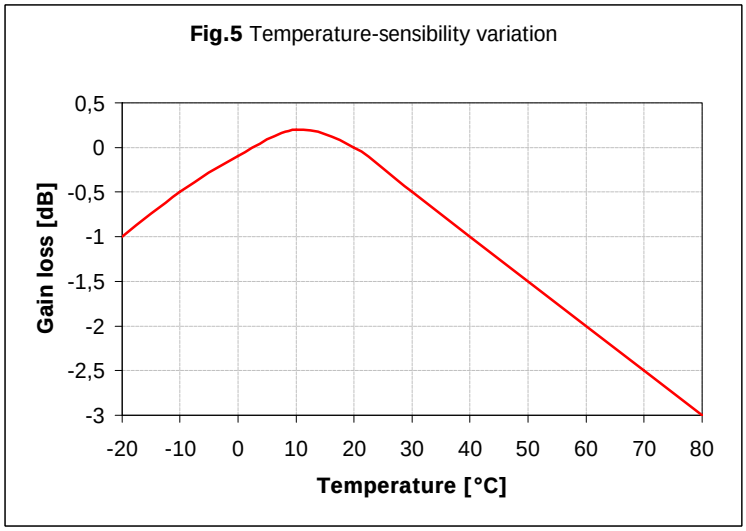
Reference curves

Fig.4 Frequency-Selectivity



The curve has been obtained by the test system shown in Fig.1

Fig.5 Temperature-sensibility variation



5V supply, RF input 433,92MHz, -95dBm

8-INPUT PRIORITY ENCODER

The HEF4532B is an 8-input priority encoder with eight active HIGH priority inputs (I_0 to I_7), three active HIGH outputs (O_0 to O_2), an active HIGH enable input (E_{in}), an active HIGH enable output (E_{out}) and an active HIGH group select output (GS).
Data is accepted on inputs I_0 to I_7. The binary code corresponding to the highest priority input (I_0 to I_7) which is HIGH, is generated on O_0 to O_2 if E_{in} is HIGH. Input I_7 is assigned the highest priority. GS is HIGH when one or more priority inputs and E_{in} are HIGH. E_{out} is HIGH when I_0 to I_7 are LOW and E_{in} is HIGH. E_{in}, when LOW, forces all outputs (O_0 to O_2, GS, E_{out}) LOW.

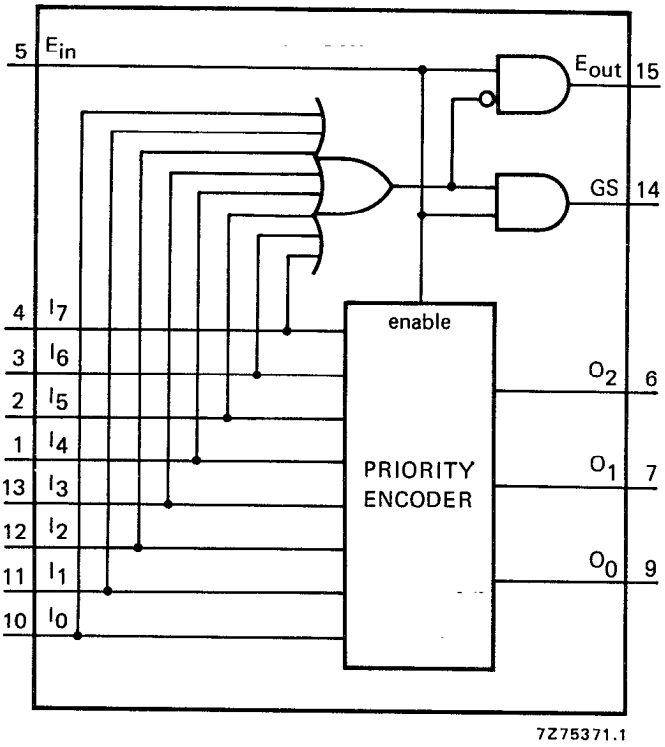


Fig. 1 Functional diagram.

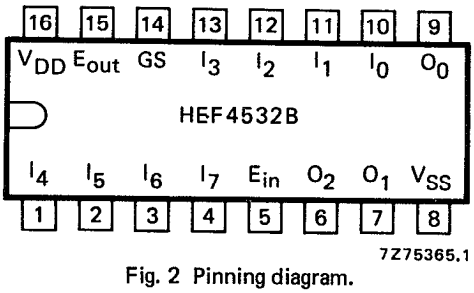


Fig. 2 Pinning diagram.

HEF4532BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4532BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4532BT(D): 16-lead SO; plastic (SOT109-1)
( ): Package Designator North America

PINNING

I_0 to I_7	priority inputs
E_{in}	enable input
E_{out}	enable output
GS	group select output
O_0 to O_2	outputs

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

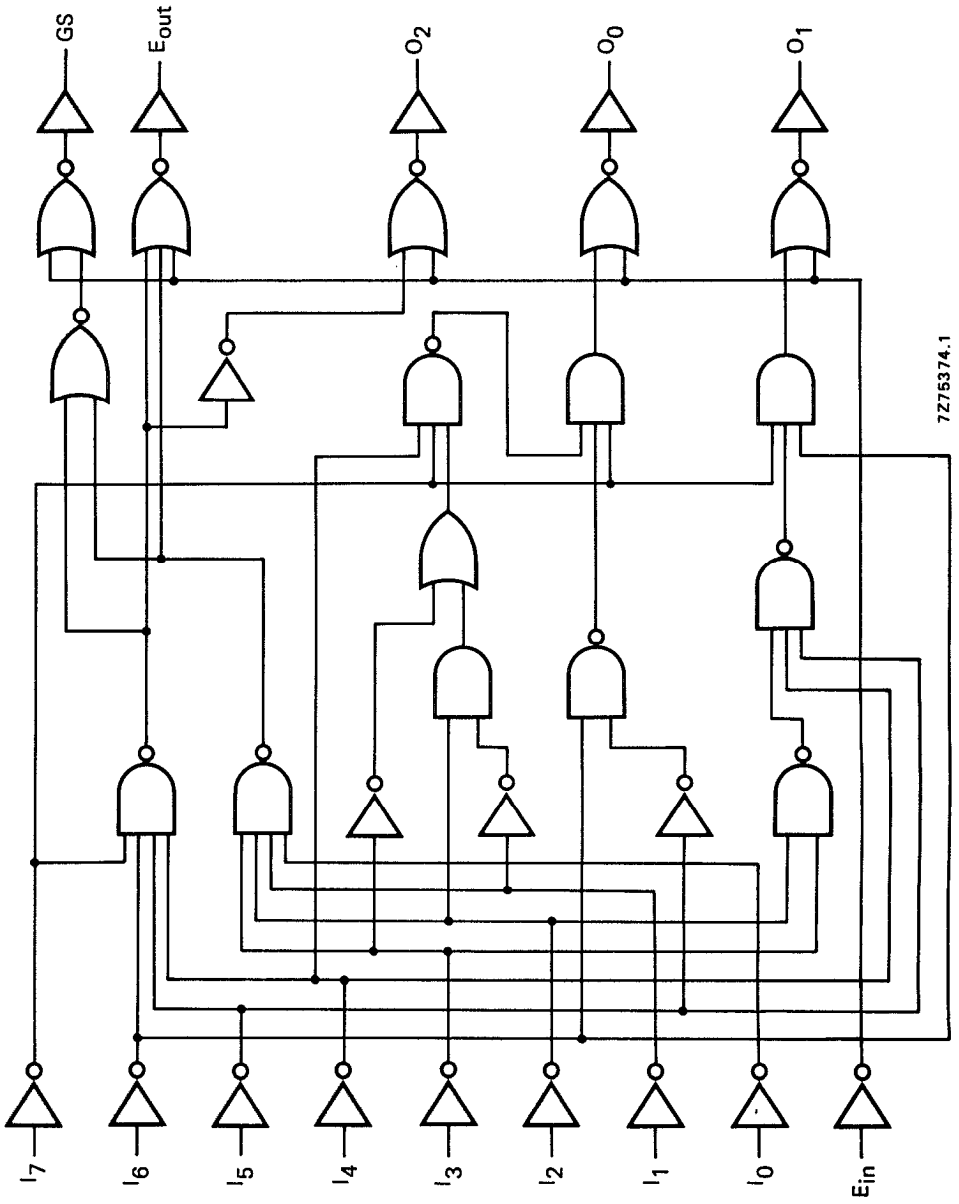


Fig. 3 Logic diagram.

TRUTH TABLE

inputs									outputs				
E_{in}	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	GS	O_2	O_1	O_0	E_{out}
L	X	X	X	X	X	X	X	X	L	L	L	L	L
H	L	L	L	L	L	L	L	L	L	L	L	L	H
H	H	X	X	X	X	X	X	X	H	H	H	H	L
H	L	H	X	X	X	X	X	X	H	H	H	L	L
H	L	L	H	X	X	X	X	X	H	H	L	H	L
H	L	L	L	H	X	X	X	X	H	H	L	L	L
H	L	L	L	L	H	X	X	X	H	L	H	H	L
H	L	L	L	L	L	H	X	X	H	L	H	L	L
H	L	L	L	L	L	L	H	X	H	L	L	H	L
H	L	L	L	L	L	L	L	H	H	L	L	L	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

LOGIC EQUATIONS

$O_2 = E_{in} \cdot (I_4 + I_5 + I_6 + I_7)$
$O_1 = E_{in} \cdot (I_2 \cdot \overline{I}_4 \cdot \overline{I}_5 + I_3 \cdot \overline{I}_4 \cdot \overline{I}_5 + I_6 + I_7)$
$O_0 = E_{in} \cdot (I_1 \cdot \overline{I}_2 \cdot \overline{I}_4 \cdot \overline{I}_6 + I_3 \cdot \overline{I}_4 \cdot \overline{I}_6 + I_5 \cdot \overline{I}_6 + I_7)$
$E_{out} = E_{in} \cdot \overline{I}_0 \cdot \overline{I}_1 \cdot \overline{I}_2 \cdot \overline{I}_3 \cdot \overline{I}_4 \cdot \overline{I}_5 \cdot \overline{I}_6 \cdot \overline{I}_7$
$GS = E_{in} \cdot (I_0 + I_1 + I_2 + I_3 + I_4 + I_5 + I_6 + I_7)$

A.C. CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times $\leqslant 20$ ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1\,620\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$6\,600\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$15\,970\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns; see also waveforms Fig. 4

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
E_{in} → E_{out}	5			95	190	ns	68 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
	5			80	160	ns	53 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
E_{in} → GS	5			85	170	ns	58 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
	5			80	160	ns	53 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
E_{in} → O_n	5			80	160	ns	53 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
	5			85	170	ns	58 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
I_n → O_n	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
I_n → GS	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
HIGH to LOW	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

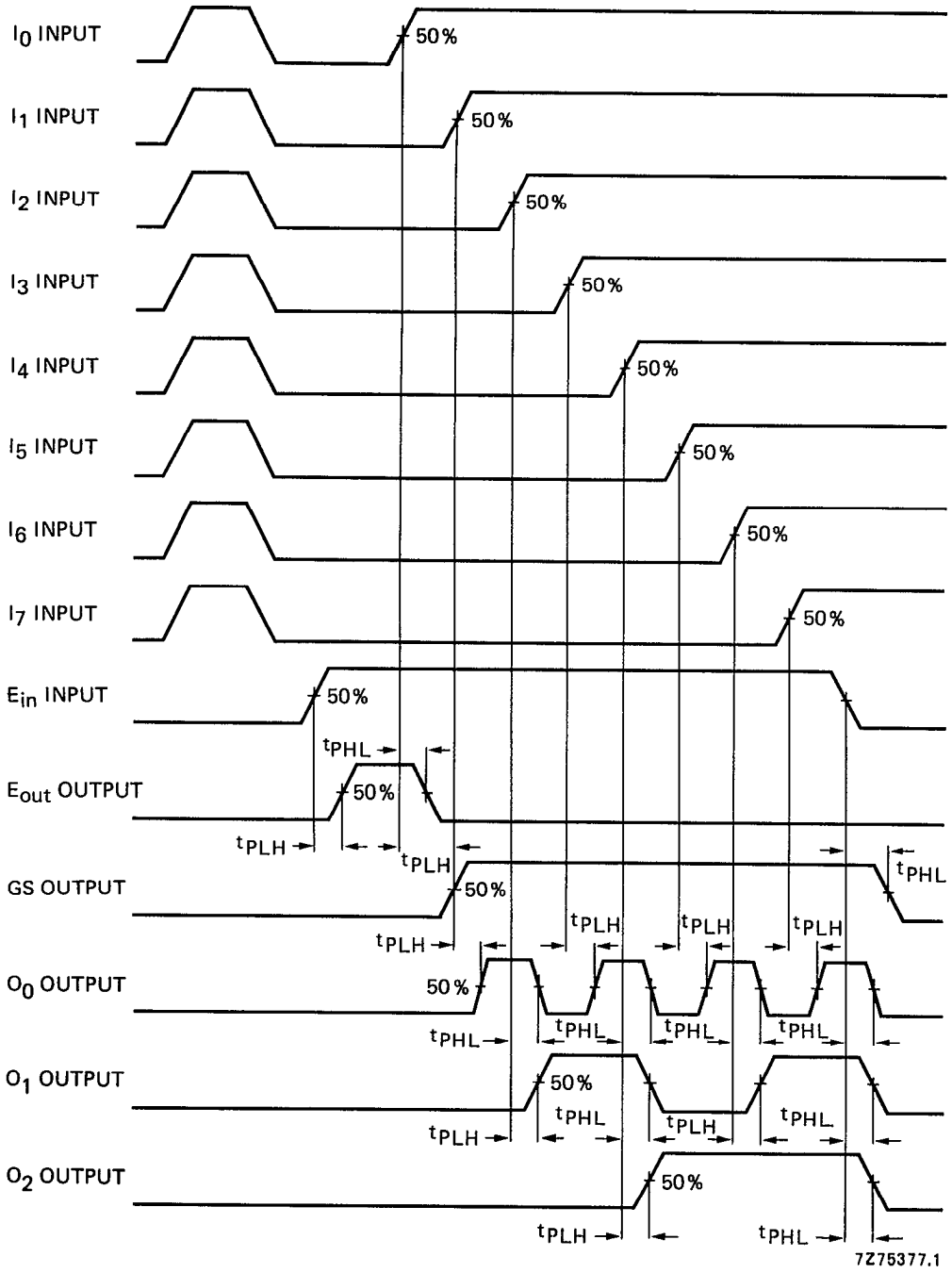


Fig. 4 Waveforms showing propagation delays from inputs to outputs.

APPLICATION INFORMATION

Some examples of applications for the HEF4532B are:

- Priority encoder
- Keyboard encoder

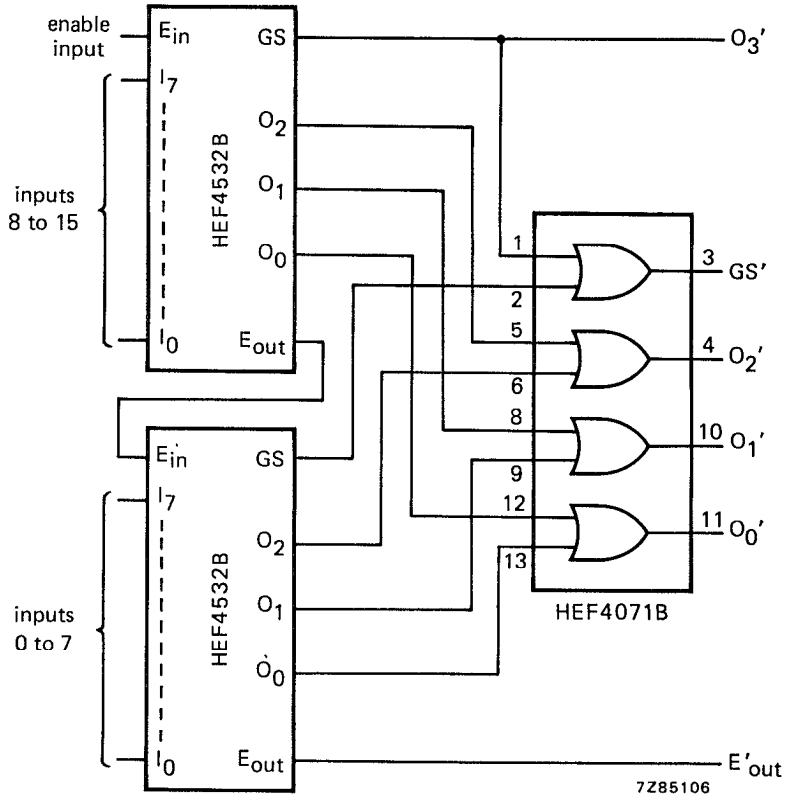


Fig. 5 16-level priority encoder.

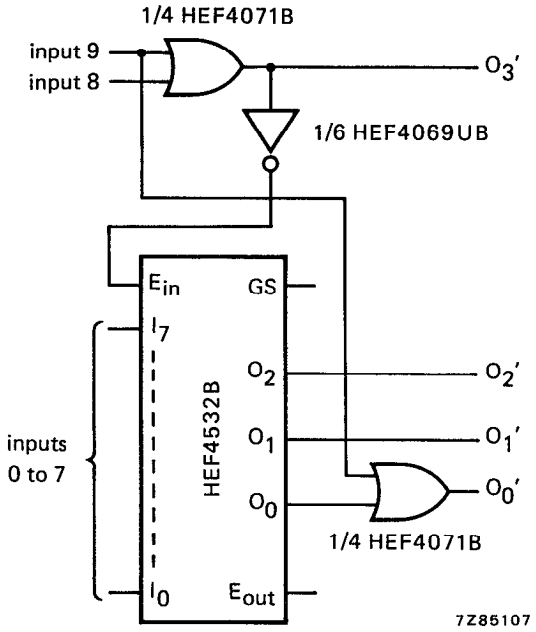


Fig. 6 0-to-9 keyboard encoder.

TRUTH TABLE (for Fig. 6)

inputs										outputs				
9	8	7	6	5	4	3	2	1	0	GS	O_3'	O_2'	O_1'	O_0'
H	X	X	X	X	X	X	X	X	X	L	H	L	L	H
L	H	X	X	X	X	X	X	X	X	L	H	L	L	L
L	L	H	X	X	X	X	X	X	X	H	L	H	H	H
L	L	L	H	X	X	X	X	X	X	H	L	H	H	L
L	L	L	L	H	X	X	X	X	X	H	L	H	L	H
L	L	L	L	L	H	X	X	X	X	H	L	H	L	L
L	L	L	L	L	L	H	X	X	X	H	L	L	H	H
L	L	L	L	L	L	L	H	X	X	H	L	L	H	L
L	L	L	L	L	L	L	L	H	X	H	L	L	L	H
L	L	L	L	L	L	L	L	L	H	H	L	L	L	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

National Semiconductor

February 1988

CD4020BM/CD4020BC 14-Stage Ripple Carry Binary Counters CD4040BM/CD4040BC 12-Stage Ripple Carry Binary Counters CD4060BM/CD4060BC 14-Stage Ripple Carry Binary Counters

General Description

The CD4020BM/CD4020BC, CD4060BM/CD4060BC are 14-stage ripple carry binary counters, and the CD4040BM/CD4040BC is a 12-stage ripple carry binary counter. The counters are advanced one count on the negative transition of each clock pulse. The counters are reset to the zero state by a logical "1" at the reset input independent of clock.

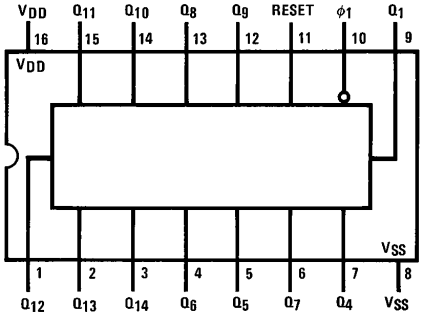
Features

■ Wide supply voltage range	1.0V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	Fan out of 2 driving 74L or 1 driving 74LS
■ Medium speed operation	8 MHz typ. at V_{DD} = 10V
■ Schmitt trigger clock input	

Connection Diagrams

Dual-In-Line Package

CD4020BM/CD4020BC



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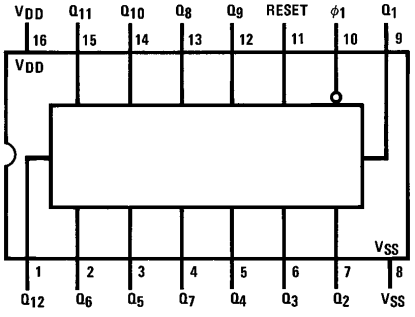
Top View

Order Number CD4020B, CD4040B or CD4060B

Dual-In-Line Package

CD4040BM/CD4040BC



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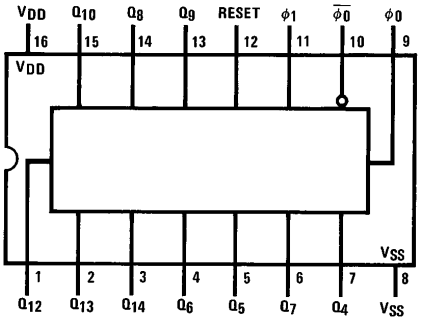
Top View

Dual-In-Line Package

CD4060BM/CD4060BC



TL/F/5953–3

Top View

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to V_{DD} +0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Package Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions

Supply Voltage (V_{DD})	+3V to +15V
Input Voltage (V_{IN})	0V to V_{DD}
Operating Temperature Range (T_A)	
CD40XXBM	−55°C to +125°C
CD40XXBC	−40°C to +85°C

DC Electrical Characteristics CD40XXBM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5			5		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10			10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20			20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
	(See Note 3)	V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
	(See Note 3)	V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Data does not apply to oscillator points ϕ_0 and $\overline{\phi_0}$ of CD4060BM/CD4060BC. I_{OH} and I_{OL} are tested one output at a time.

DC Electrical Characteristics 40XXBC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20			20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40			40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80			80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V

DC Electrical Characteristics 40XXBC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (See Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (See Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics* CD4020BM/CD4020BC, CD4040BM/CD4040BC

T_A = 25°C, C_L = 50 pF, R_L = 200k, t_r = t_f = 20 ns, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL1}, t_{PLH1}	Propagation Delay Time to Q_1	V_{DD} = 5V		250	550	ns
		V_{DD} = 10V		100	210	ns
		V_{DD} = 15V		75	150	ns
t_{PHL}, t_{PLH}	Interstage Propagation Delay Time from Q_n to Q_{n+1}	V_{DD} = 5V		150	330	ns
		V_{DD} = 10V		60	125	ns
		V_{DD} = 15V		45	90	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5V		125	335	ns
		V_{DD} = 10V		50	125	ns
		V_{DD} = 15V		40	100	ns
t_{rCL}, t_{fCL}	Maximum Clock Rise and Fall Time	V_{DD} = 5V			No Limit	ns
		V_{DD} = 10V			No Limit	ns
		V_{DD} = 15V			No Limit	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	1.5	4		MHz
		V_{DD} = 10V	4	10		MHz
		V_{DD} = 15V	5	12		MHz
$t_{PHL(R)}$	Reset Propagation Delay	V_{DD} = 5V		200	450	ns
		V_{DD} = 10V		100	210	ns
		V_{DD} = 15V		80	170	ns
$t_{WH(R)}$	Minimum Reset Pulse Width	V_{DD} = 5V		200	450	ns
		V_{DD} = 10V		100	210	ns
		V_{DD} = 15V		80	170	ns
C_{in}	Average Input Capacitance	Any Input		5	7.5	pF
C_{pd}	Power Dissipation Capacitance			50		pF

*AC Parameters are guaranteed by DC correlated testing.

AC Electrical Characteristics* CD4060BM/CD4060BC

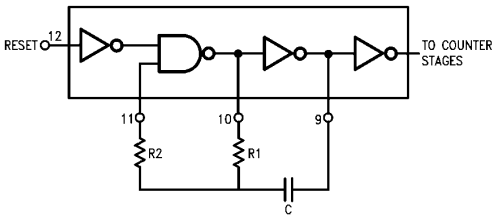
$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, $t_r = t_f = 20$ ns, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL4}, t_{PLH4}	Propagation Delay Time to Q_4	$V_{DD} = 5V$		550	1300	ns
		$V_{DD} = 10V$		250	525	ns
		$V_{DD} = 15V$		200	400	ns
t_{PHL}, t_{PLH}	Interstage Propagation Delay Time from Q_n to Q_{n+1}	$V_{DD} = 5V$		150	330	ns
		$V_{DD} = 10V$		60	125	ns
		$V_{DD} = 15V$		45	90	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5V$		170	500	ns
		$V_{DD} = 10V$		65	170	ns
		$V_{DD} = 15V$		50	125	ns
t_{rCL}, t_{fCL}	Maximum Clock Rise and Fall Time	$V_{DD} = 5V$			No Limit	ns
		$V_{DD} = 10V$			No Limit	ns
		$V_{DD} = 15V$			No Limit	ns
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	1	3		MHz
		$V_{DD} = 10V$	3	8		MHz
		$V_{DD} = 15V$	4	10		MHz
$t_{PHL(R)}$	Reset Propagation Delay	$V_{DD} = 5V$		200	450	ns
		$V_{DD} = 10V$		100	210	ns
		$V_{DD} = 15V$		80	170	ns
$t_{WH(R)}$	Minimum Reset Pulse Width	$V_{DD} = 5V$		200	450	ns
		$V_{DD} = 10V$		100	210	ns
		$V_{DD} = 15V$		80	170	ns
C_{in}	Average Input Capacitance	Any Input		5	7.5	pF
C_{pd}	Power Dissipation Capacitance			50		pF

*AC Parameters are guaranteed by DC correlated testing.

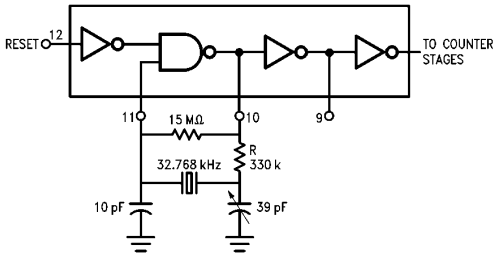
CD4060B Typical Oscillator Connections

RC Oscillator



TL/F/5953–4

Crystal Oscillator



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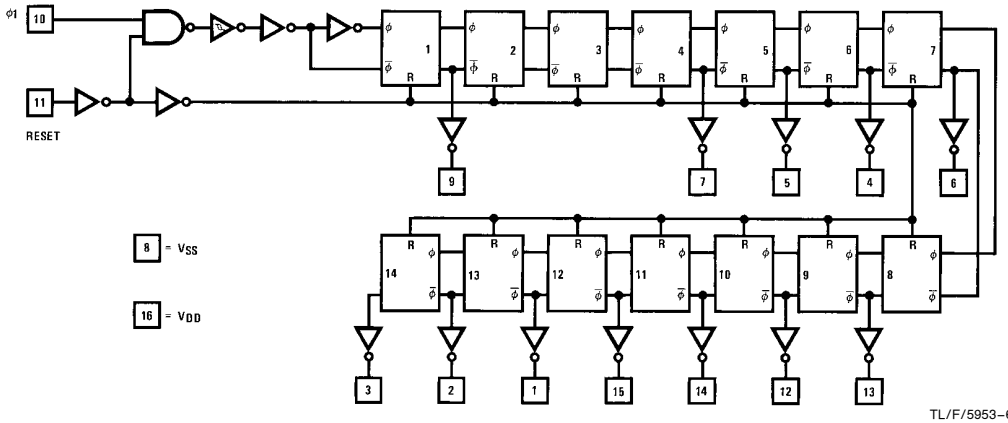
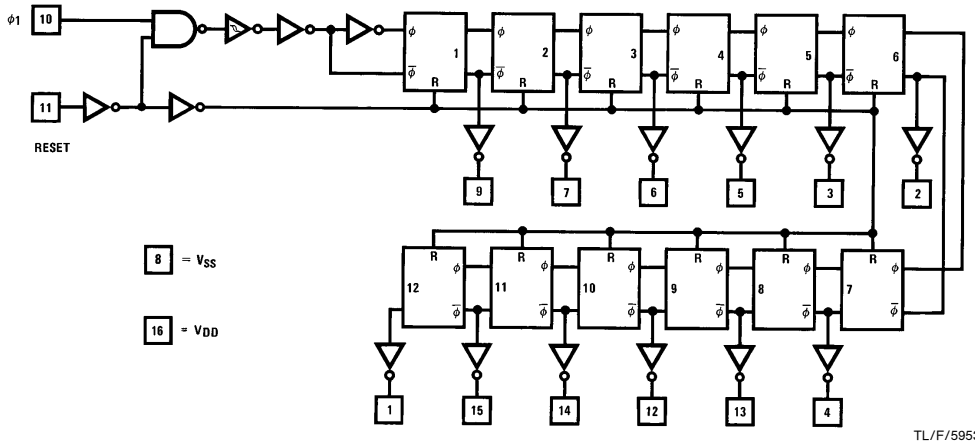
Schematic Diagrams

CD4020BM/CD4020BC Schematic Diagram



TL/F/5953–6

CD4040BM/CD4040BC Schematic Diagram



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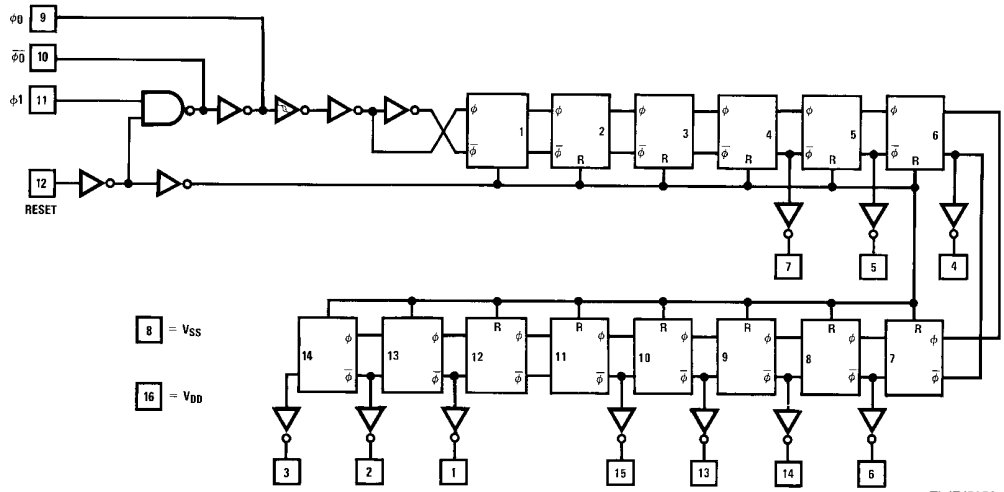
CD4060BM/CD4060BC Schematic Diagram



TL/F/5953–8

National Semiconductor

February 1988

CD4013BM/CD4013BC Dual D Flip-Flop

General Description

The CD4013B dual D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement mode transistors. Each flip-flop has independent data, set, reset, and clock inputs and "Q" and "$\overline{Q}$" outputs. These devices can be used for shift register applications, and by connecting "$\overline{Q}$" output to the data input, for counter and toggle applications. The logic level present at the "D" input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line respectively.

Features

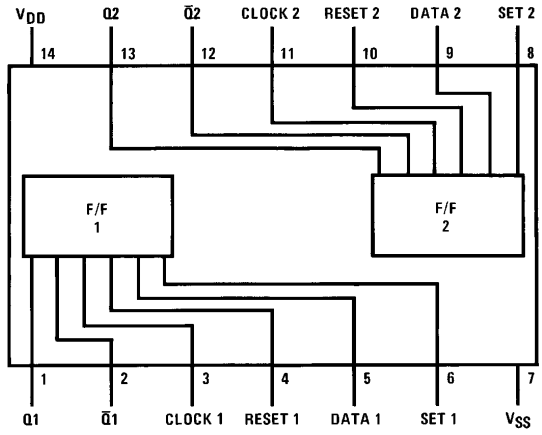
■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial electronics
- Remote metering
- Computers

Connection Diagram

Dual-In-Line Package



TL/F/5946–1

Top View

Order Number CD4013B

Truth Table

CL†	D	R	S	Q	$\overline{Q}$
⌐⌐	0	0	0	0	1
⌐⌐	1	0	0	1	0
⌐⌐	x	0	0	Q	$\overline{Q}$
x	x	1	0	0	1
x	x	0	1	1	0
x	x	1	1	1	1

No change
† = Level change
x = Don't care case

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
Input Voltage (V_{IN})	$-0.5\ V_{DC}$ to $V_{DD} + 0.5\ V_{DC}$
Storage Temp. Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	$+3\ V_{DC}$ to $+15\ V_{DC}$
Input Voltage (V_{IN})	$0\ V_{DC}$ to $V_{DD}\ V_{DC}$
Operating Temperature Range (T_A)	
CD4013BM	$-55°C$ to $+125°C$
CD4013BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4013BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$, $V_{IN} = V_{DD}$ or V_{SS}		1.0			1.0		30	μA
		$V_{DD} = 10V$, $V_{IN} = V_{DD}$ or V_{SS}		2.0			2.0		60	μA
		$V_{DD} = 15V$, $V_{IN} = V_{DD}$ or V_{SS}		4.0			4.0		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V$		0.05			0.05		0.05	V
		$V_{DD} = 10V$		0.05			0.05		0.05	V
		$V_{DD} = 15V$		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V$	4.95		4.95			4.95		V
		$V_{DD} = 10V$	9.95		9.95			9.95		V
		$V_{DD} = 15V$	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5			1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$		3.0			3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$	7.0		7.0			7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 4.6V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.6		−1.3	−2.25		−0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4013BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$, $V_{IN} = V_{DD}$ or V_{SS}		4.0			4.0		30	μA
		$V_{DD} = 10V$, $V_{IN} = V_{DD}$ or V_{SS}		8.0			8.0		60	μA
		$V_{DD} = 15V$, $V_{IN} = V_{DD}$ or V_{SS}		16.0			16.0		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V$		0.05			0.05		0.05	V
		$V_{DD} = 10V$		0.05			0.05		0.05	V
		$V_{DD} = 15V$		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V$	4.95		4.95			4.95		V
		$V_{DD} = 10V$	9.95		9.95			9.95		V
		$V_{DD} = 15V$	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5			1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$		3.0			3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0			4.0		4.0	V

DC Electrical Characteristics CD4013BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
V_{IH}	High Level Input Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$	7.0		7.0			7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 4.6V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.3		−1.1	−2.25		−0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

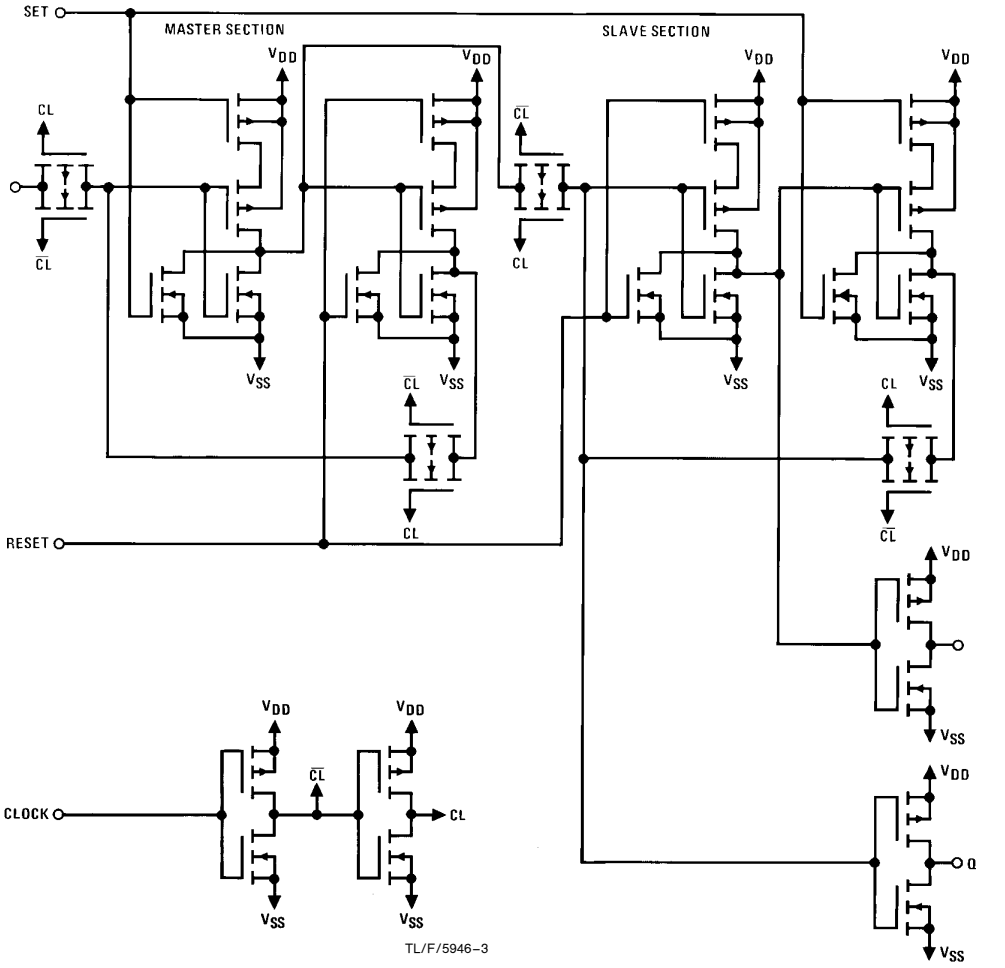
Note 3: I_{OH} and I_{OL} are measured one output at a time.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CLOCK OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		200	350	ns
		$V_{DD} = 10V$		80	160	ns
		$V_{DD} = 15V$		65	120	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		32	65	ns
t_{RCL}, t_{FCL}	Maximum Clock Rise and Fall Time	$V_{DD} = 5V$			15	μs
		$V_{DD} = 10V$			10	μs
		$V_{DD} = 15V$			5	μs
t_{SU}	Minimum Set-Up Time	$V_{DD} = 5V$		20	40	ns
		$V_{DD} = 10V$		15	30	ns
		$V_{DD} = 15V$		12	25	ns
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	2.5	5		MHz
		$V_{DD} = 10V$	6.2	12.5		MHz
		$V_{DD} = 15V$	7.6	15.5		MHz
SET AND RESET OPERATION						
$t_{PHL(R)}$, $t_{PLH(S)}$	Propagation Delay Time	$V_{DD} = 5V$		150	300	ns
		$V_{DD} = 10V$		65	130	ns
		$V_{DD} = 15V$		45	90	ns
$t_{WH(R)}$, $t_{WH(S)}$	Minimum Set and Reset Pulse Width	$V_{DD} = 5V$		90	180	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		25	50	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF

*AC Parameters are guaranteed by DC correlated testing.

Schematic Diagram



TL/F/5946–3

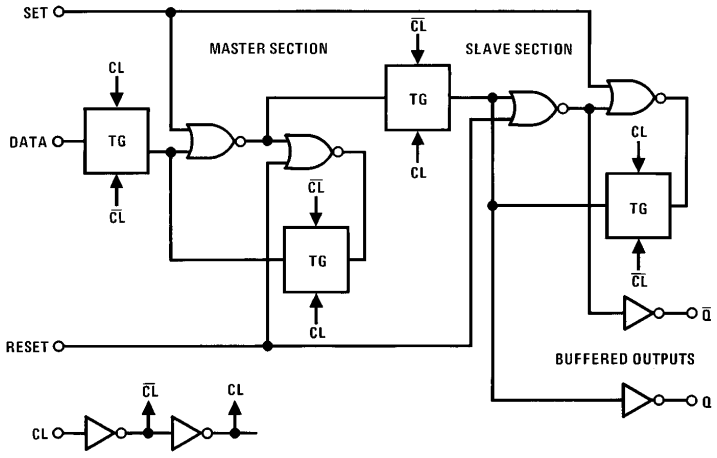
TL/F/5946–2

ALL P-SUBSTRATES ( ) CONNECTED TO V_{DD}

ALL N-SUBSTRATES ( ) CONNECTED TO V_{SS}

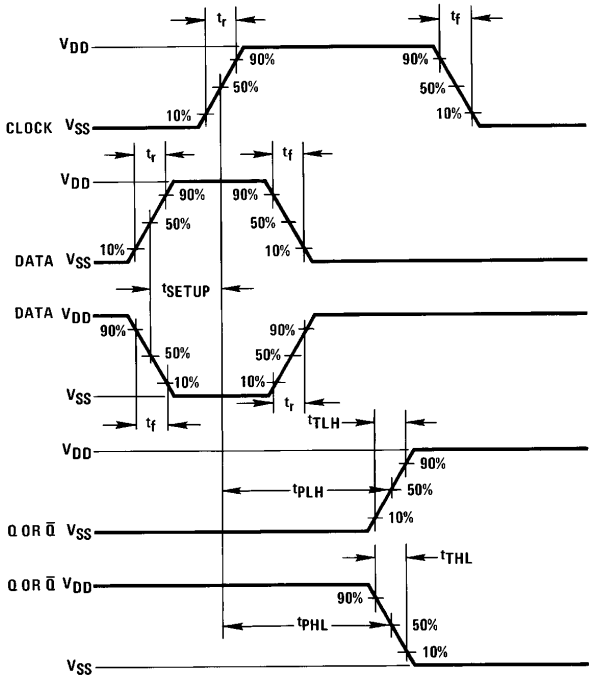
TL/F/5946–4

Logic Diagram



TL/F/5946–5

Switching Time Waveforms



TL/F/5946–6

National Semiconductor

June 1989

54LS164/DM54LS164/DM74LS164
8-Bit Serial In/Parallel Out Shift Registers

General Description

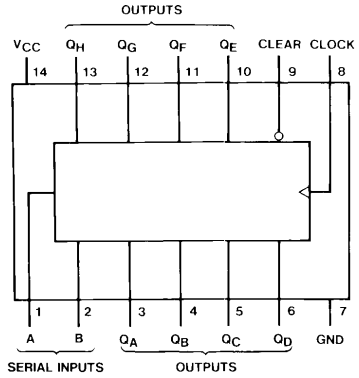
These 8-bit shift registers feature gated serial inputs and an asynchronous clear. A low logic level at either input inhibits entry of the new data, and resets the first flip-flop to the low level at the next clock pulse, thus providing complete control over incoming data. A high logic level on either input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

Features

- Gated (enable/disable) serial inputs
- Fully buffered clock and serial inputs
- Asynchronous clear
- Typical clock frequency 36 MHz
- Typical power dissipation 80 mW
- Alternate Military/Aerospace device (54LS164) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6398–1

Order Number 54LS164DMQB, 54LS164FMQB, 54LS164LMQB, DM54LS164J, DM54LS164W, DM74LS164M or DM74LS164N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

Inputs				Outputs			
Clear	Clock	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L	...	L
H	L	X	X	Q_{A0}	Q_{B0}	...	Q_{H0}
H	↑	H	H	H	Q_{An}	...	Q_{Gn}
H	↑	L	X	L	Q_{An}	...	Q_{Gn}
H	↑	X	L	L	Q_{An}	...	Q_{Gn}

H = High Level (steady state), L = Low Level (steady state)

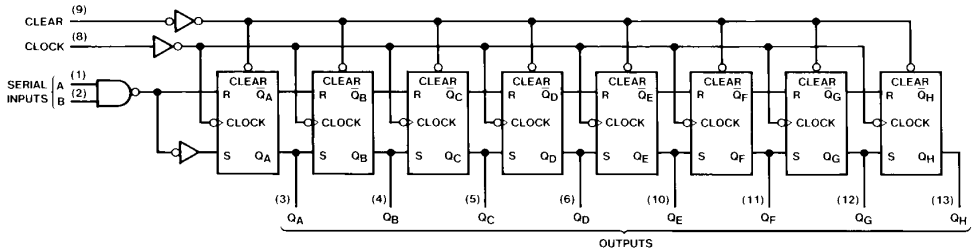
X = Don't Care (any input, including transitions)

↑ = Transition from low to high level

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

Logic Diagram



TL/F/6398–2

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" tables will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS164			DM74LS164			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 4)		0		25	0		25	MHz
t_W	Pulse Width (Note 4)	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Data Setup Time (Note 4)		17			17			ns
t_H	Data Hold Time (Note 4)		5			5			ns
t_{REL}	Clear Release Time (Note 4)		30			30			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			16	27	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

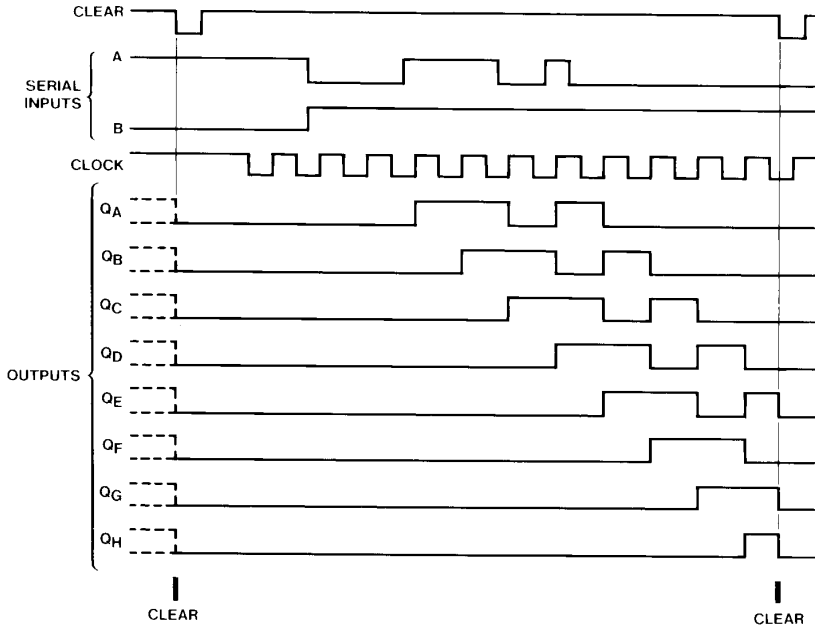
Note 3: I_{CC} is measured with all outputs open, the SERIAL input grounded, the CLOCK input at 2.4V, and a momentary ground, then 4.5V, applied to the CLEAR input.

Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$				Units
			$C_L = 15$ pF		$C_L = 50$ pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25				MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		27		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		32		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		36		45	ns

Timing Diagram



TL/F/6398–3

National Semiconductor

June 1989

54LS153/DM54LS153/DM74LS153
Dual 4-Line to 1-Line Data Selectors/Multiplexers

General Description

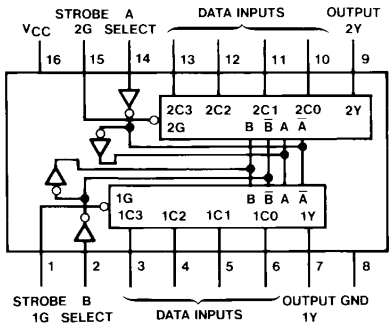
Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

Features

- Permits multiplexing from N lines to 1 line
- Performs at parallel-to-serial conversion
- Strobe (enable) line provided for cascading (N lines to n lines)
- High fan-out, low impedance, totem pole outputs
- Typical average propagation delay times
  - — From data 14 ns
  - — From strobe 19 ns
  - — From select 22 ns
- Typical power dissipation 31 mW
- Alternate Military/Aerospace device (54LS153) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

Connection Diagram

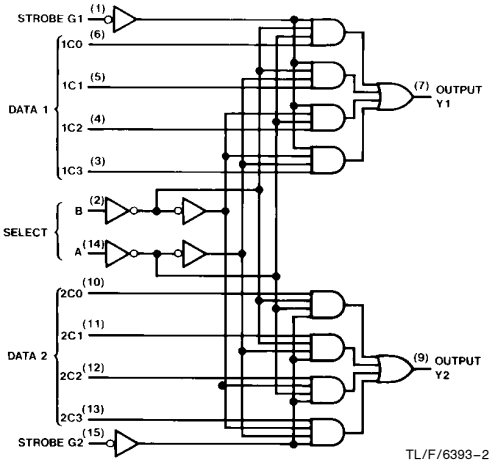
Dual-In-Line Package



TL/F/6393–1

Order Number 54LS153DMQB, 54LS153FMQB, 54LS153LMQB, DM54LS153J, DM54LS153W, DM74LS153M or DM74LS153N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Logic Diagram



TL/F/6393–2

Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

H = High Level, L = Low Level, X = Don't Care

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150° C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS153			DM74LS153			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6.2	10	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25° C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all other inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) to (Output)	$R_L = 2\ k\Omega$				Units
			$C_L = 15\ pF$		$C_L = 50\ pF$		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		15		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		26		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		29		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		38		45	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		24		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		32		40	ns

National Semiconductor

June 1989

54LS138/DM54LS138/DM74LS138, 54LS139/DM54LS139/DM74LS139 Decoders/Demultiplexers

General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The LS138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The LS139 comprises two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

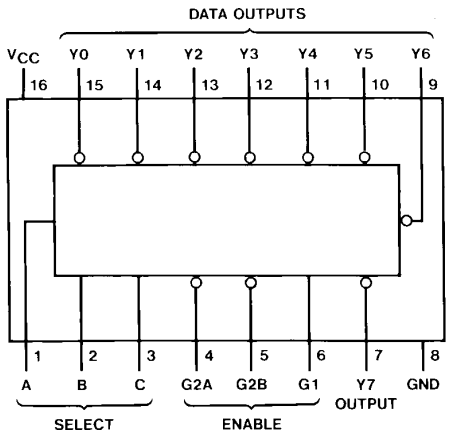
All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

Features

- Designed specifically for high speed:
  - Memory decoders
  - Data transmission systems
- LS138 3-to-8-line decoders incorporates 3 enable inputs to simplify cascading and/or data reception
- LS139 contains two fully independent 2-to-4-line decoders/demultiplexers
- Schottky clamped for high performance
- Typical propagation delay (3 levels of logic)
  - LS138 21 ns
  - LS139 21 ns
- Typical power dissipation
  - LS138 32 mW
  - LS139 34 mW
- Alternate Military/Aerospace devices (54LS138, 54LS139) are available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagrams

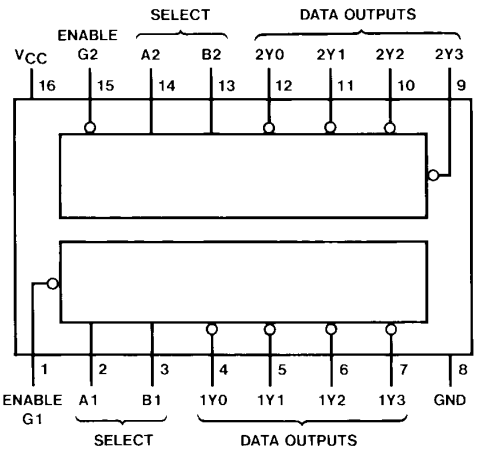
Dual-in-Line Package



TL/F/6391–1

Order Number 54LS138DMQB, 54LS138FMQB, 54LS138LMQB, DM54LS138J, DM54LS138W, DM74LS138M or DM74LS138N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Dual-in-Line Package



TL/F/6391–2

Order Number 54LS139DMQB, 54LS139FMQB, 54LS139LMQB, DM54LS139J, DM54LS139W, DM74LS139M or DM74LS139N
See NS Package Number E20A, J16A, M16A, N16E or W16A

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS138			DM74LS138			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS138 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6.3	10	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs enabled and open.

'LS138 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	Levels of Delay	R_L = 2 kΩ				Units
				C_L = 15 pF		C_L = 50 pF		
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output	2		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output	2		27		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output	3		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output	3		27		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output	2		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output	2		24		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output	3		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output	3		28		40	ns

Recommended Operating Conditions

Symbol	Parameter	DM54LS139			DM74LS139			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

’LS139 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6.8	11	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs enabled and open.

’LS139 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output		27		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output		24		40	ns

Function Tables

LS138

Inputs					Outputs							
Enable		Select										
G1	G2*	C	B	A	YO	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

* G2 = G2A + G2B

H = High Level, L = Low Level, X = Don’t Care

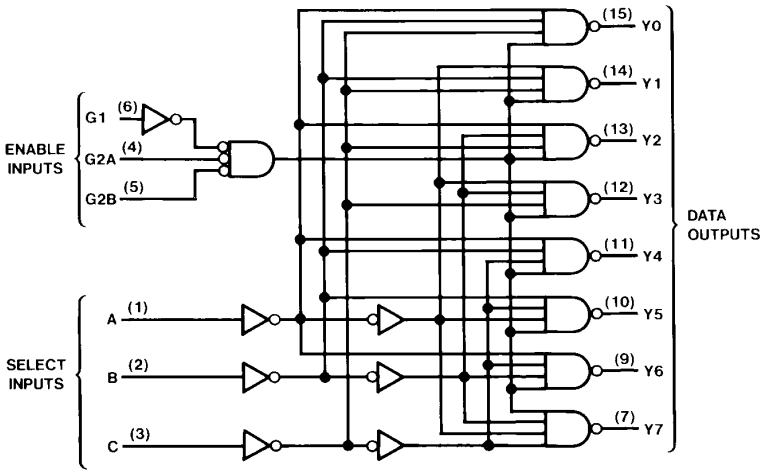
LS139

Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = High Level, L = Low Level, X = Don’t Care

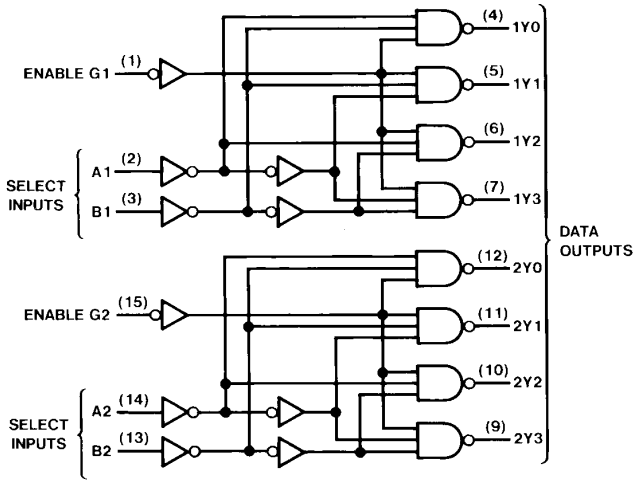
Logic Diagrams

LS138



TL/F/6391–3

LS139



TL/F/6391–4

National Semiconductor

June 1989

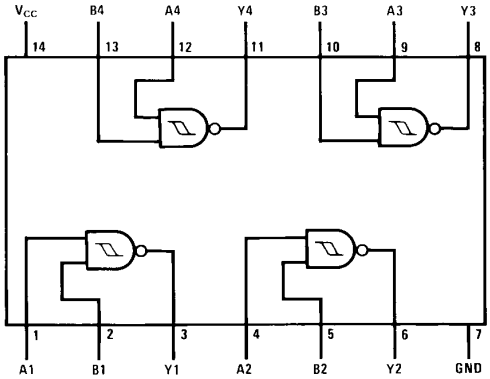
DM54LS132/DM74LS132 Quad 2-Input NAND Gates with Schmitt Trigger Inputs

General Description

This device contains four independent gates each of which performs the logic NAND function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.

Connection Diagram

Dual-In-Line Package



TL/F/6389–1

Order Number DM54LS132J, DM54LS132W, DM74LS132M or DM74LS132N
See NS Package Number J14A, M14A, N14A or W14B

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

DM54LS132/DM74LS132 Quad 2-Input NAND Gates with Schmitt Trigger Inputs

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS132			DM74LS132			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 1)	1.4	1.6	1.9	1.4	1.6	1.9	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 1)	0.5	0.8	1	0.5	0.8	1	V
HYS	Input Hysteresis (Note 1)	0.4	0.8		0.4	0.8		V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_I = V_{T-} Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_I = V_{T+} Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, V_I = V_{T+}			−0.14		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = 5V, V_I = V_{T-}			−0.18		mA
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			5.9	11	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			8.2	14	mA

Note 1: V_{CC} = 5V

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

June 1989

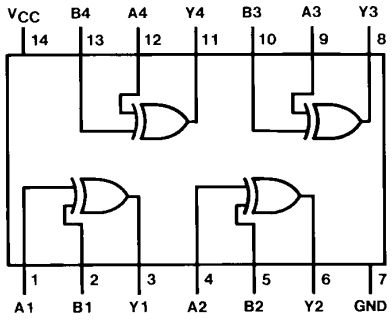
DM54LS86/DM74LS86
Quad 2-Input Exclusive-OR Gates

General Description

This device contains four independent gates each of which performs the logic exclusive-OR function.

Connection Diagram

Dual-In-Line Package



TL/F/6380–1

Order Number DM54LS86J, DM54LS86W, DM74LS86M or DM74LS86N
See NS Package Number J14A, M14A, N14A or W14B

Function Table

$$Y = A \oplus B = \overline{A}B + A\overline{B}$$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS86			DM74LS86			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.2	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)			6.1	10	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 4)			9	15	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CCH} is measured with all outputs open, one input at each gate at 4.5V, and the other inputs grounded.

Note 4: I_{CCL} is measured with all outputs open and all inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	$R_L = 2\ k\Omega$				Units
			$C_L = 15$ pF		$C_L = 50$ pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Other Input Low		18		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			17		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Other Input High		10		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			12		15	ns

National Semiconductor

June 1989

54LS85/DM54LS85/DM74LS85 4-Bit Magnitude Comparators

General Description

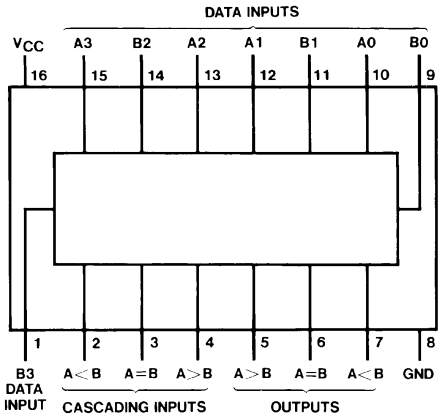
These 4-bit magnitude comparators perform comparison of straight binary or BCD codes. Three fully-decoded decisions about two, 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A = B input. The cascading path is implemented with only a two-gate-level delay to reduce overall comparison times for long words.

Features

- Typical power dissipation 52 mW
- Typical delay (4-bit words) 24 ns
- Alternate Military/Aerospace device (54LS85) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6379–1

Order Number 54LS85DMQB, 54LS85FMQB, 54LS85LMQB, DM54LS85J, DM54LS85W, DM74LS85M or DM74LS85N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Function Table

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	**A2, B2**	**A1, B1**	**A0, B0**	**A > B**	**A < B**	**A = B**	**A > B**	**A < B**	**A = B**
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

H = High Level, L = Low Level, X = Don't Care

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS85			DM74LS85			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	A < B			0.1	mA
			A > B			0.1	
			Others			0.3	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	A < B			20	μA
			A > B			20	
			Others			60	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	A < B			−0.4	mA
			A > B			−0.4	
			Others			−1.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			10	20	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

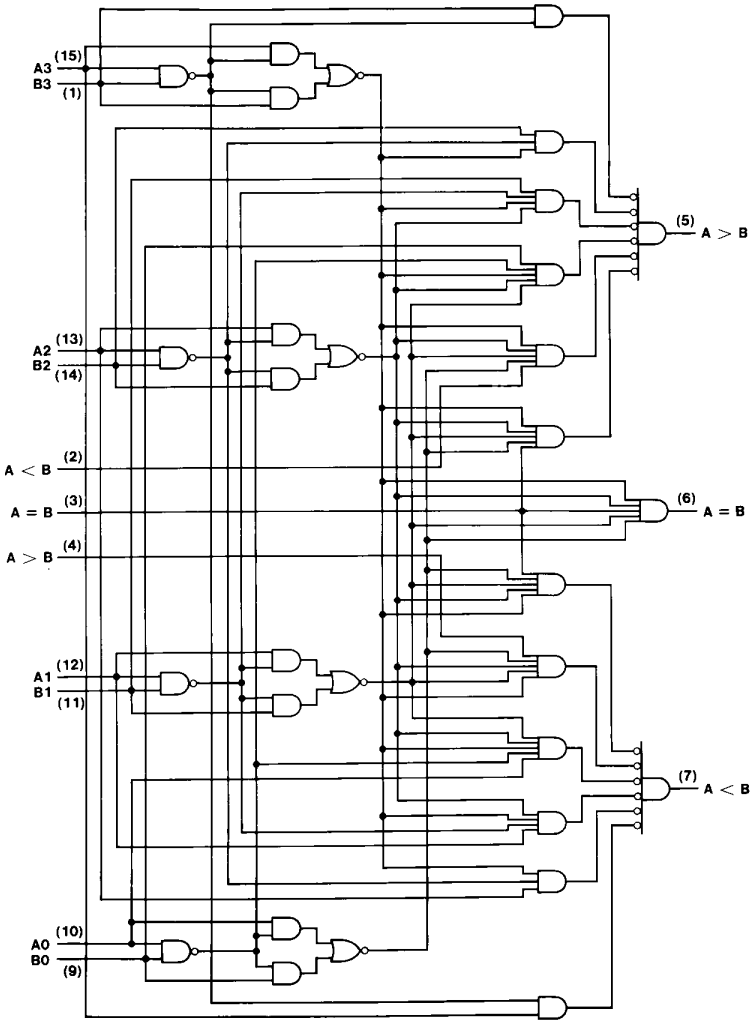
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open, A = B grounded and all other inputs at 4.5V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From Input	To Output	Number of Gate Levels	$R_L = 2\ k\Omega$				Units
					$C_L = 15\ pF$		$C_L = 50\ pF$		
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low-to-High Level Output	Any A or B Data Input	A < B, A > B	3		36		42	ns
			A = B	4		40		40	
t_{PHL}	Propagation Delay Time High-to-Low Level Output	Any A or B Data Input	A < B, A > B	3		30		40	ns
			A = B	4		30		40	
t_{PLH}	Propagation Delay Time Low-to-High Level Output	A < B or A = B	A > B	1		22		26	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output	A < B or A = B	A > B	1		17		26	ns
t_{PLH}	Propagation Delay Time Low-to-High Level Output	A =B	A = B	2		20		25	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output	A = B	A = B	2		17		26	ns
t_{PLH}	Propagation Delay Time Low-to-High Level Output	A > B or A = B	A < B	1		22		26	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output	A > B or A = B	A < B	1		17		26	ns

Logic Diagram



TL/F/6379–2

National Semiconductor

June 1989

54LS74/DM54LS74A/DM74LS74A Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear and Complementary Outputs

General Description

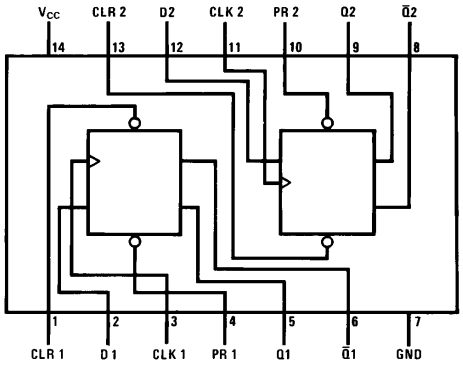
This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is low or high without affecting the outputs as long as the data setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Features

- Alternate military/aerospace device (54LS74) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6373–1

Order Number 54LS74DMQB, 54LS74FMQB, 54LS74LMQB, DM54LS74AJ, DM54LS74AW, DM74LS74AM or DM74LS74AN
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

↑ = Positive-going Transition

* = This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (high) level.

Q_0 = The output logic level of Q before the indicated input conditions were established.

54LS74/DM54LS74A/DM74LS74A Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear and Complementary Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS74A			DM74LS74A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		25	0		25	MHz
f_{CLK}	Clock Frequency (Note 3)		0		20	0		20	MHz
t_W	Pulse Width (Note 2)	Clock High	18			18			ns
		Preset Low	15			15			
		Clear Low	15			15			
t_W	Pulse Width (Note 3)	Clock High	25			25			ns
		Preset Low	20			20			
		Clear Low	20			20			
t_{SU}	Setup Time (Notes 1 and 2)		20 ↑			20 ↑			ns
t_{SU}	Setup Time (Notes 1 and 3)		25 ↑			25 ↑			ns
t_H	Hold Time (Note 1 and 4)		0 ↑			0 ↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: $C_L = 15$ pF, $R_L = 2$ kΩ, $T_A = 25°C$, and $V_{CC} = 5V$.

Note 3: $C_L = 50$ pF, $R_L = 2$ kΩ, $T_A = 25°C$, and $V_{CC} = 5V$.

Note 4: $T_A = 25°C$ and $V_{CC} = 5V$.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @Max Input Voltage	V_{CC} = Max, V_I = 7V	Data			0.1	mA
			Clock			0.1	
			Preset			0.2	
			Clear			0.2	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Data			20	μA
			Clock			20	
			Clear			40	
			Preset			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Data			−0.4	mA
			Clock			−0.4	
			Preset			−0.8	
			Clear			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			4	8	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where V_O = 2.25V and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 3: With all outputs open, I_{CC} is measured with CLOCK grounded after setting the Q and $\overline{Q}$ outputs high in turn.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		25		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		30		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		25		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		30		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		25		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		30		35	ns

FAIRCHILD SEMICONDUCTOR™

March 1998

DM74LS47
BCD to 7-Segment Decoder/Driver with Open-Collector Outputs

General Description

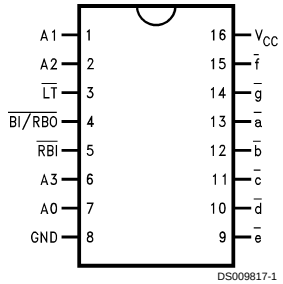
The 'LS47 accepts four lines of BCD (8421) input data, generates their complements internally and decodes the data with seven AND/OR gates having open-collector outputs to drive indicator segments directly. Each segment output is guaranteed to sink 24 mA in the ON (LOW) state and withstand 15V in the OFF (HIGH) state with a maximum leakage current of 250 µA. Auxiliary inputs provided blanking, lamp test and cascadable zero-suppression functions.

Features

- Open-collector outputs
- Drive indicator segments directly
- Cascadable zero-suppression capability
- Lamp test input

Connection Diagram

Dual-In-Line Package



DS009817-1

Order Number DM54LS47J, DM54LS47W, DM74LS47M or DM74LS47N
See Package Number J16A, M16A, N16E or W16A

Pin Names	Description
A0–A3	BCD Inputs
$\overline{RBI}$	Ripple Blanking Input (Active LOW)
$\overline{LT}$	Lamp Test Input (Active LOW)
$\overline{BI/RBO}$	Blanking Input (Active LOW) or Ripple Blanking Output (Active LOW)
$\overline{a}$ –$\overline{g}$	*Segment Outputs (Active LOW)

Note 1: *OC—Open Collector

Absolute Maximum Ratings (Note 2)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	DM54LS47			DM74LS47			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current $\overline{a} - \overline{g}$ @ 15V = V_{OH} (Note 3)			−50			−250	µA
I_{OH}	High Level Output Current $\overline{BI}$ /$\overline{RBO}$						−50	µA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

Note 2: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 3: OFF state at $\overline{a}$–$\overline{g}$.

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, $\overline{BI}$ /$\overline{RBO}$	DM54	2.4			V
			DM74	2.7	3.4		
I_{OFF}	Output High Current Segment Outputs	V_{CC} = 5.5V, V_O = 15V $\overline{a} - \overline{g}$				250	µA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, $\overline{a} - \overline{g}$	DM54			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 3.2 mA, $\overline{BI}$ /$\overline{RBO}$	DM74			0.5	
		I_{OL} = 12 mA, $\overline{a} - \overline{g}$	DM74		0.25	0.4	
		I_{OL} = 1.6 mA, $\overline{BI}$ /$\overline{RBO}$	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	DM74			100	µA
		V_{CC} = Max, V_I = 10V	DM54				
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5) , I_{OS} at $\overline{BI/RBO}$	DM54	−0.3		−2.0	mA
			DM74	−0.3		−2.0	
I_{CC}	Supply Current	V_{CC} = Max				13	mA

Note 4: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = +5.0V, T_A = +25˚C

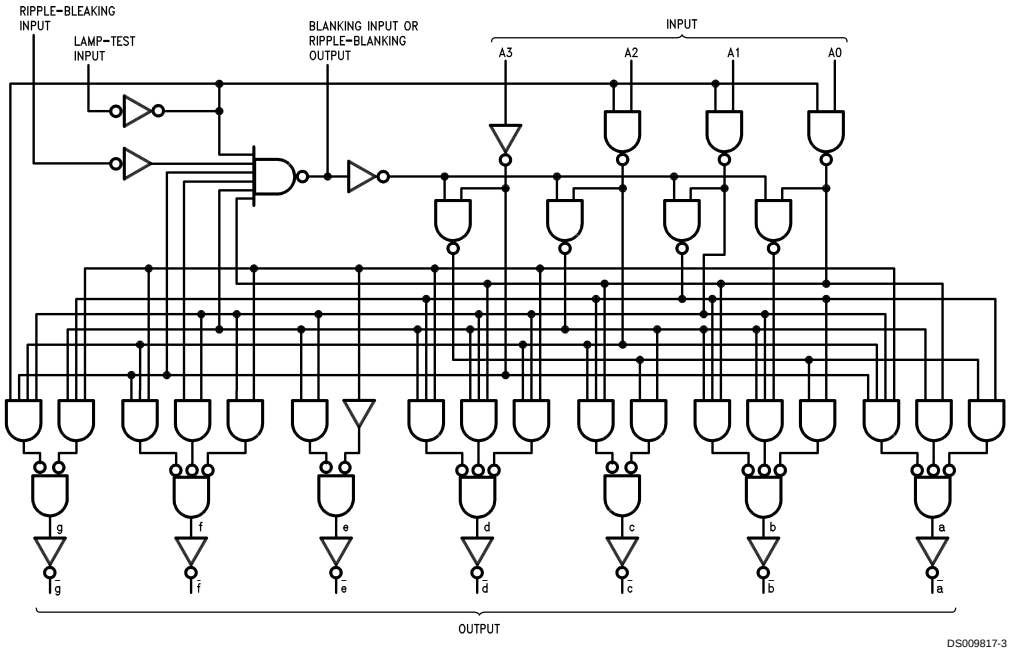
Symbol	Parameter	Conditions	R_L = 665Ω, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay			100	ns
t_{PHL}	An to $\overline{a}$ –$\overline{g}$			100	
t_{PLH}	Propagation Delay			100	ns
t_{PHL}	$\overline{RBI}$ to $\overline{a}$ –$\overline{g}$ (Note 6)			100	

Note 6: $\overline{LT}$ = HIGH, A0–A3 = LOW

Functional Description

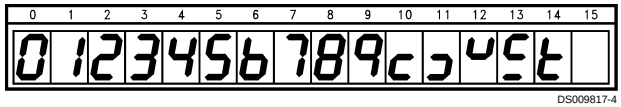
The 'LS47 decodes the input data in the pattern indicated in the Truth Table and the segment identification illustration. If the input data is decimal zero, a LOW signal applied to the $\overline{RBI}$ blanks the display and causes a multidigit display. For example, by grounding the $\overline{RBI}$ of the highest order decoder and connecting its $\overline{BI/RBO}$ to $\overline{RBI}$ of the next lowest order decoder, etc., leading zeros will be suppressed. Similarly, by grounding $\overline{RBI}$ of the lowest order decoder and connecting its $\overline{BI/RBO}$ to $\overline{RBI}$ of the next highest order decoder, etc., trailing zeros will be suppressed. Leading and trailing zeros can be suppressed simultaneously by using external gates, i.e.: by driving $\overline{RBI}$ of a intermediate decoder from an OR gate whose inputs are $\overline{BI/RBO}$ of the next highest and lowest order decoders. $\overline{BI/RBO}$ also serves as an unconditional blanking input. The internal NAND gate that generates the $\overline{RBO}$ signal has a resistive pull-up, as opposed to a totem pole, and thus $\overline{BI/RBO}$ can be forced LOW by external means, using wired-collector logic. A LOW signal thus applied to $\overline{BI/RBO}$ turns off all segment outputs. This blanking feature can be used to control display intensity by varying the duty cycle of the blanking signal. A LOW signal applied to $\overline{LT}$ turns on all segment outputs, provided that $\overline{BI/RBO}$ is not forced LOW.

Logic Diagram



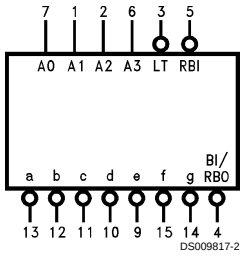
DS009817-3

Numerical Designations—Resultant Displays



DS009817-4

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Truth Table

Decimal or Function	Inputs							Outputs							Note
	$\overline{LT}$	$\overline{RBI}$	A3	A2	A1	A0	$\overline{BI/RBO}$	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	(Note 7)
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	(Note 7)
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
$\overline{BI}$	X	X	X	X	X	X	L	H	H	H	H	H	H	H	(Note 8)
$\overline{RBI}$	H	L	L	L	L	L	L	H	H	H	H	H	H	H	(Note 9)
$\overline{LT}$	L	X	X	X	X	X	H	L	L	L	L	L	L	L	(Note 10)

Note 7: $\overline{BI/RBO}$ is wire-AND logic serving as blanking input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBO}$). The blanking out ($\overline{BI}$) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking or a decimal 0 is not desired. X = input may be HIGH or LOW.

Note 8: When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a HIGH level regardless of the state of any other input condition.

Note 9: When ripple-blanking input ($\overline{RBI}$) and inputs A0, A1, A2 and A3 are LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output ($\overline{RBO}$) goes to a LOW level (response condition).

Note 10: When the blanking input/ripple-blanking output ($\overline{BI/RBO}$) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

National Semiconductor

May 1989

54LS32/DM54LS32/DM74LS32 Quad 2-Input OR Gates

General Description

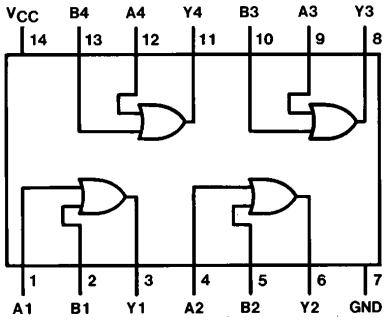
This device contains four independent gates each of which performs the logic OR function.

Features

- Alternate Military/Aerospace device (54LS32) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6361–1

Order Number 54LS32DMQB, 54LS32FMQB, 54LS32LMQB, DM54LS32J, DM54LS32W, DM74LS32M or DM74LS32N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$Y = A + B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = High Logic Level
L = Low Logic Level

  RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS32			DM74LS32			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			3.1	6.2	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			4.9	9.8	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	11	4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	11	4	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

June 1989

54LS08/DM54LS08/DM74LS08 Quad 2-Input AND Gates

General Description

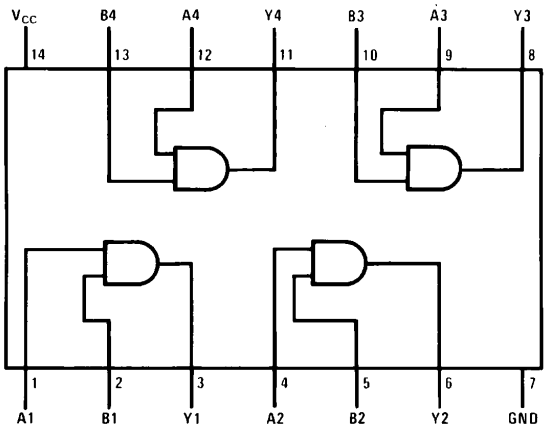
This device contains four independent gates each of which performs the logic AND function.

Features

- Alternate Military/Aerospace device (54LS08) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6347–1

Order Number 54LS08DMQB, 54LS08FMQB, 54LS08LMQB, DM54LS08J, DM54LS08W, DM74LS08M or DM74LS08N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$Y = AB$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level
L = Low Logic Level

  RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS08			DM74LS08			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			2.4	4.8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			4.4	8.8	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	4	13	6	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	11	5	18	ns

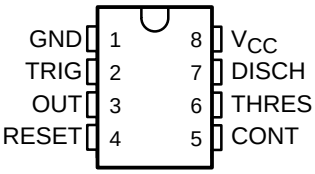
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

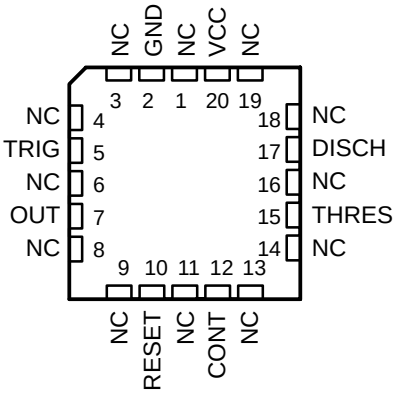
- **Timing From Microseconds to Hours**
- **Astable or Monostable Operation**
- **Adjustable Duty Cycle**
- **TTL-Compatible Output Can Sink or Source up to 200 mA**
- **Functionally Interchangeable With the Signetics NE555, SA555, SE555, SE555C; Have Same Pinout**

SE555C FROM TI IS NOT RECOMMENDED FOR NEW DESIGNS

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC–No internal connection

description

These devices are precision monolithic timing circuits capable of producing accurate time delays or oscillation. In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle may be independently controlled with two external resistors and a single external capacitor.

The threshold and trigger levels are normally two-thirds and one-third, respectively, of V_{CC}. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. RESET can override all other inputs and can be used to initiate a new timing cycle. When RESET goes low, the flip-flop is reset and the output goes low. Whenever the output is low, a low-impedance path is provided between DISCH and ground.

The output circuit is capable of sinking or sourcing current up to 200 mA. Operation is specified for supplies of 5 V to 15 V. With a 5-V supply, output levels are compatible with TTL inputs.

The NE555 is characterized for operation from 0°C to 70°C. The SA555 is characterized for operation from –40°C to 85°C. The SE555 and SE555C are characterized for operation over the full military range of –55°C to 125°C.

AVAILABLE OPTIONS

T_A	PACKAGE					CHIP FORM (Y)
	V_{THRES} max V_{CC} = 15 V	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (P)	
0°C to 70°C	11.2 V	NE555D			NE555P	NE555Y
–40°C to 85°C	11.2 V	SA555D			SA555P	
–55°C to 125°C	10.6 V 11.2 V	SE555D SE555CD	SE555FK SE555CFK	SE555JG SE555CJG	SE555P SE555CP	

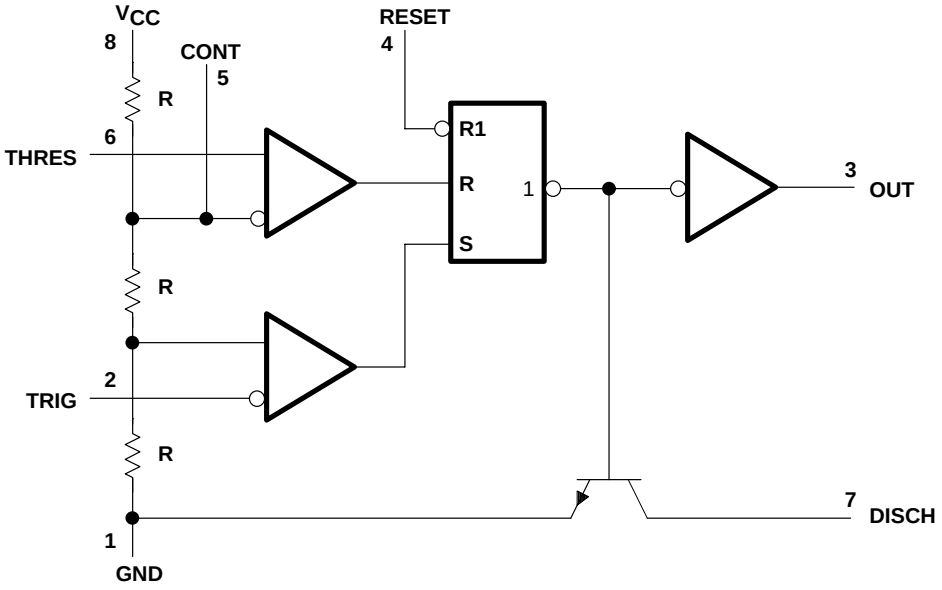
The D package is available taped and reeled. Add the suffix R to the device type (e.g., NE555DR).

FUNCTION TABLE

RESET	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	< 1/3 V_{DD}	Irrelevant	High	Off
High	> 1/3 V_{DD}	> 2/3 V_{DD}	Low	On
High	> 1/3 V_{DD}	< 2/3 V_{DD}	As previously established	

† Voltage levels shown are nominal.

functional block diagram

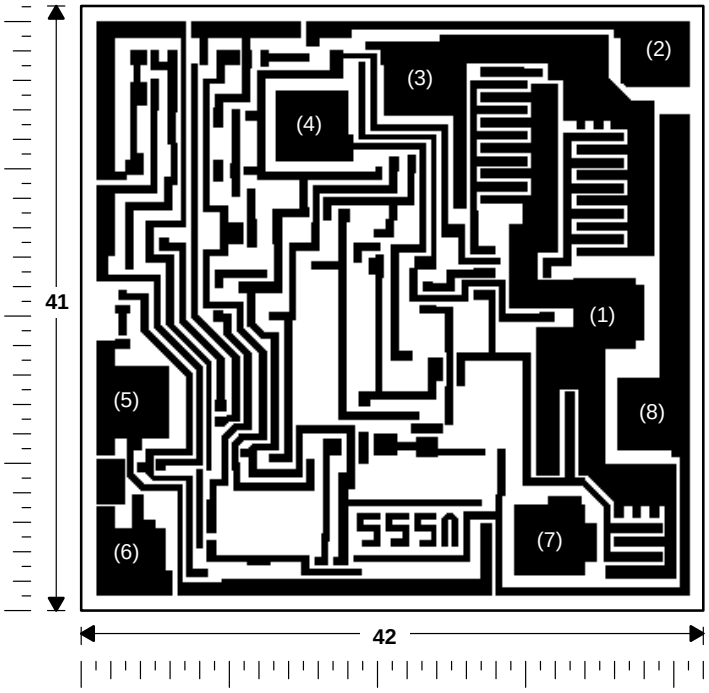


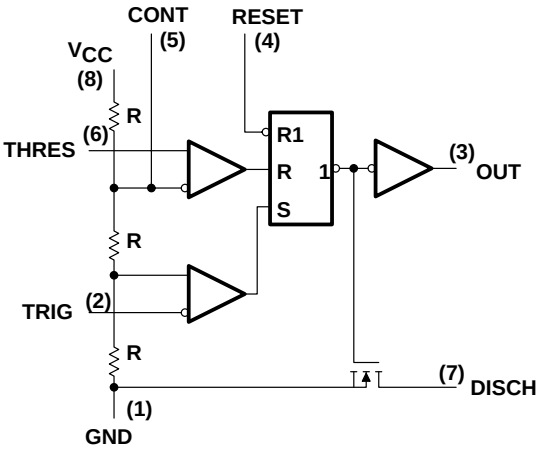
RESET can override TRIG, which can override THRES.
Pin numbers shown are for the D, JG, and P packages only.

chip information

These chips, properly assembled, display characteristics similar to the NE555 (see electrical table for NE555Y). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_J max = 150° C

TOLERANCES ARE ± 10%

ALL DIMENSIONS ARE IN MILS

PIN (1) INTERNALLY CONNECTED TO BACKSIDE OF CHIP

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1) . . . . . 18 V
Input voltage (CONT, RESET, THRES, and TRIG) . . . . . V_{CC}
Output current . . . . . ±225 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: NE555 . . . . . 0°C to 70°C
SA555 . . . . . –40°C to 85°C
SE555, SE555C . . . . . –55°C to 125°C
Storage temperature range . . . . . –65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG (SE555, SE555C)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
JG (SA555, NE555C)	825 mW	6.6 mW/°C	528 mW	429 mW	N/A
P	1000 mW	8.0 mW/°C	640 mW	520 mW	N/A

recommended operating conditions

	NE555		SA555		SE555		SE555C		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	4.5	16	4.5	16	4.5	18	4.5	16	V
Input voltage (CONT, RESET, THRES, and TRIG)		V_{CC}		V_{CC}		V_{CC}		V_{CC}	V
Output current		±200		±200		±200		±200	mA
Operating free-air temperature, T_A	0	70	–40	85	–55	125	–55	125	°C

electrical characteristics, V_{CC} = 5 V to 15 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SE555			NE555, SA555, SE555C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
THRES voltage level	V_{CC} = 15 V		9.4	10	10.6	8.8	10	11.2	V
	V_{CC} = 5 V		2.7	3.3	4	2.4	3.3	4.2	
THRES current (see Note 2)				30	250		30	250	nA
TRIG voltage level	V_{CC} = 15 V		4.8	5	5.2	4.5	5	5.6	V
	V_{CC} = 5 V		1.45	1.67	1.9	1.1	1.67	2.2	
TRIG current	TRIG at 0 V			0.5	0.9		0.5	2	µA
RESET voltage level			0.3	0.7	1	0.3	0.7	1	V
RESET current	RESET at V_{CC}			0.1	0.4		0.1	0.4	mA
	RESET at 0 V			–0.4	–1		–0.4	–1.5	
DISCH switch off-state current				20	100		20	100	nA
CONT voltage (open circuit)	V_{CC} = 15 V		9.6	10	10.4	9	10	11	V
	V_{CC} = 5 V		2.9	3.3	3.8	2.6	3.3	4	
Low-level output voltage	V_{CC} = 15 V	I_{OL} = 10 mA		0.1	0.15		0.1	0.25	V
		I_{OL} = 50 mA		0.4	0.5		0.4	0.75	
		I_{OL} = 100 mA		2	2.2		2	2.5	
		I_{OL} = 200 mA		2.5			2.5		
	V_{CC} = 5 V	I_{OL} = 5 mA		0.1	0.2		0.1	0.35	
		I_{OL} = 8 mA		0.15	0.25		0.15	0.4	
High-level output voltage	V_{CC} = 15 V	I_{OH} = –100 mA	13	13.3		12.75	13.3		V
		I_{OH} = –200 mA		12.5			12.5		
	V_{CC} = 5 V	I_{OH} = –100 mA	3	3.3		2.75	3.3		
Supply current	Output low, No load	V_{CC} = 15 V		10	12		10	15	mA
		V_{CC} = 5 V		3	5		3	6	
	Output high, No load	V_{CC} = 15 V		9	10		9	13	
		V_{CC} = 5 V		2	4		2	5	

NOTE 2: This parameter influences the maximum value of the timing resistors R_A and R_B in the circuit of Figure 12. For example, when V_{CC} = 5 V, the maximum value is R = R_A + R_B ≈ 3.4 MΩ, and for V_{CC} = 15 V, the maximum value is 10 MΩ.

operating characteristics, V_{CC} = 5 V and 15 V

PARAMETER		TEST CONDITIONS†	SE555			NE555, SA555, SE555C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Initial error of timing interval‡	Each timer, monostable§	T_A = 25°C		0.5%	1.5%		1%	3%	
	Each timer, astable¶			1.5%			2.25%		
Temperature coefficient of timing interval	Each timer, monostable§	T_A = MIN to MAX		30	100		50		ppm/°C
	Each timer, astable¶			90			150		
Supply voltage sensitivity of timing interval	Each timer, monostable§	T_A = 25°C		0.05	0.2		0.1	0.5	%/V
	Each timer, astable¶			0.15			0.3		
Output pulse rise time		C_L = 15 pF, T_A = 25°C		100	200		100	300	ns
Output pulse fall time				100	200		100	300	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.
§ Values specified are for a device in a monostable circuit similar to Figure 9, with component values as follow: R_A = 2 kΩ to 100 kΩ, C = 0.1 µF.
¶ Values specified are for a device in an astable circuit similar to Figure 12, with component values as follow: R_A = 1 kΩ to 100 kΩ, C = 0.1 µF.

electrical characteristics, V_{CC} = 5 V to 15 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
THRES voltage level	V_{CC} = 15 V		8.8	10	11.2	V
	V_{CC} = 5 V		2.4	3.3	4.2	
THRES current (see Note 2)				30	250	nA
TRIG voltage level	V_{CC} = 15 V		4.5	5	5.6	V
	V_{CC} = 5 V		1.1	1.67	2.2	
TRIG current	TRIG at 0 V			0.5	2	µA
RESET voltage level			0.3	0.7	1	V
RESET current	RESET at V_{CC}			0.1	0.4	mA
	RESET at 0 V			–0.4	–1.5	
DISCH switch off-state current				20	100	nA
CONT voltage (open circuit)	V_{CC} = 15 V		9	10	11	V
	V_{CC} = 5 V		2.6	3.3	4	
Low-level output voltage	V_{CC} = 15 V	I_{OL} = 10 mA		0.1	0.25	V
		I_{OL} = 50 mA		0.4	0.75	
		I_{OL} = 100 mA		2	2.5	
		I_{OL} = 200 mA		2.5		
	V_{CC} = 5 V	I_{OL} = 5 mA		0.1	0.35	
		I_{OL} = 8 mA		0.15	0.4	
High-level output voltage	V_{CC} = 15 V	I_{OH} = –100 mA	12.75	13.3		V
		I_{OH} = –200 mA		12.5		
	V_{CC} = 5 V	I_{OH} = –100 mA	2.75	3.3		
Supply current	Output low, No load	V_{CC} = 15 V		10	15	mA
		V_{CC} = 5 V		3	6	
	Output high, No load	V_{CC} = 15 V		9	13	
		V_{CC} = 5 V		2	5	

NOTE 2: This parameter influences the maximum value of the timing resistors R_A and R_B in the circuit of Figure 12. For example, when V_{CC} = 5 V, the maximum value is $R = R_A + R_B \approx 3.4$ MΩ, and for V_{CC} = 15 V, the maximum value is 10 MΩ

operating characteristics, V_{CC} = 5 V and 15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Initial error of timing interval†	Each timer, monostable‡			1%	3%	
	Each timer, astable§			2.25%		
Supply voltage sensitivity of timing interval	Each timer, monostable‡			0.1	0.5	%/V
	Each timer, astable§			0.3		
Output pulse rise time		C_L = 15 pF		100	300	ns
Output pulse fall time				100	300	

† Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.
‡ Values specified are for a device in a monostable circuit similar to Figure 9, with component values as follow: R_A = 2 kΩ to 100 kΩ, C = 0.1 µF.
§ Values specified are for a device in an astable circuit similar to Figure 12, with component values as follow: R_A = 1 kΩ to 100 kΩ, C = 0.1 µF.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

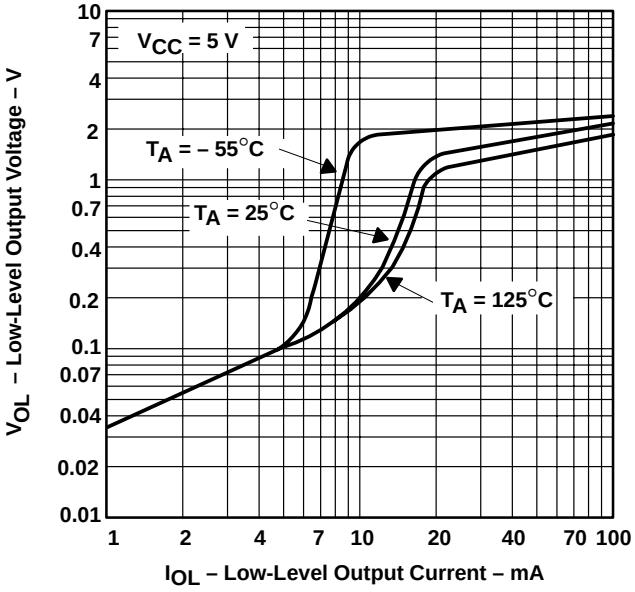


Figure 1

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

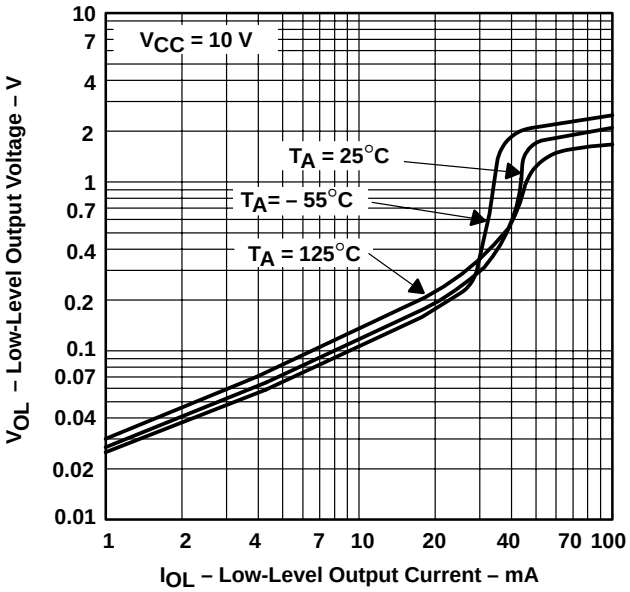


Figure 2

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

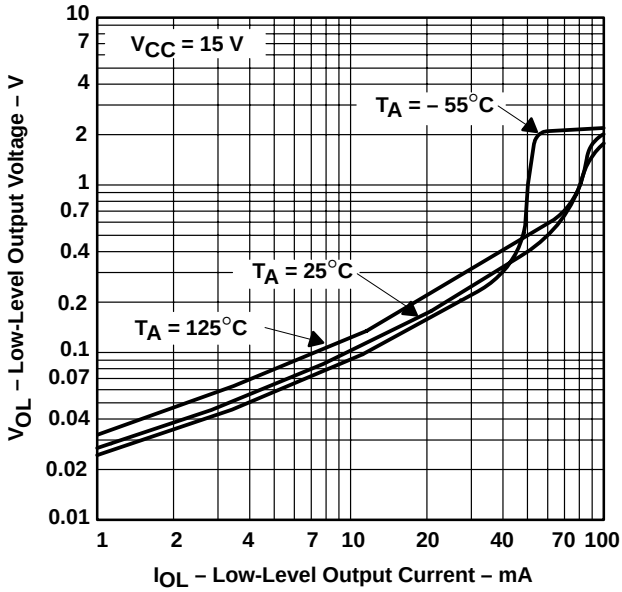


Figure 3

DROP BETWEEN SUPPLY VOLTAGE AND OUTPUT vs HIGH-LEVEL OUTPUT CURRENT

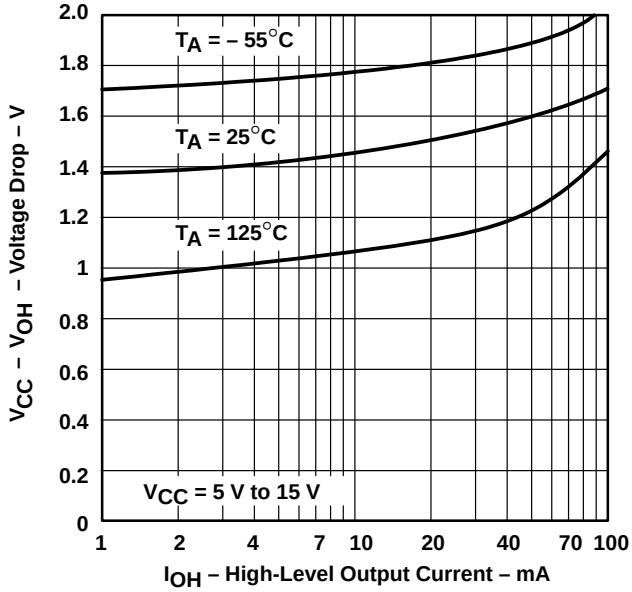


Figure 4

† Data for temperatures below 0°C and above 70°C are applicable for SE555 circuits only.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT vs SUPPLY VOLTAGE

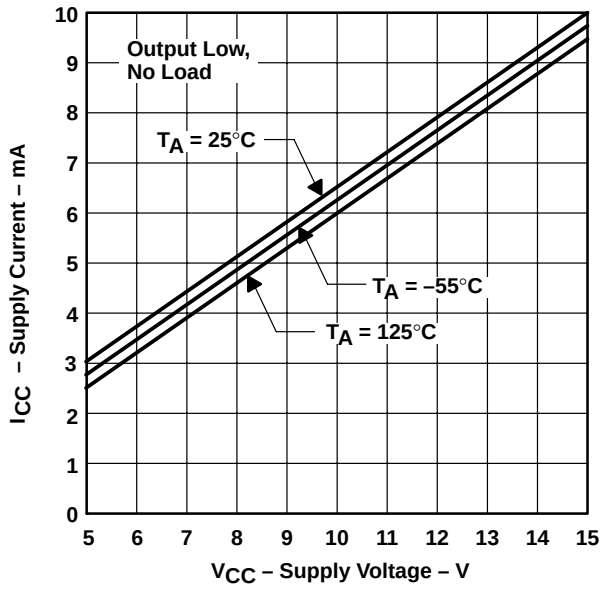


Figure 5

NORMALIZED OUTPUT PULSE DURATION (MONOSTABLE OPERATION) vs SUPPLY VOLTAGE

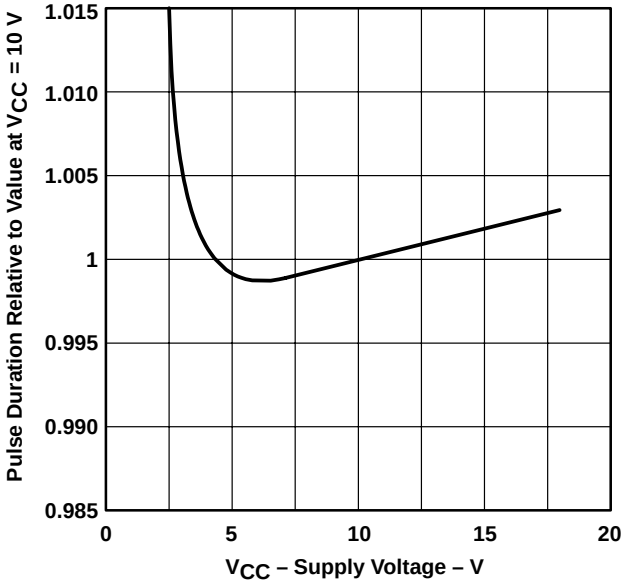


Figure 6

NORMALIZED OUTPUT PULSE DURATION (MONOSTABLE OPERATION) vs FREE-AIR TEMPERATURE

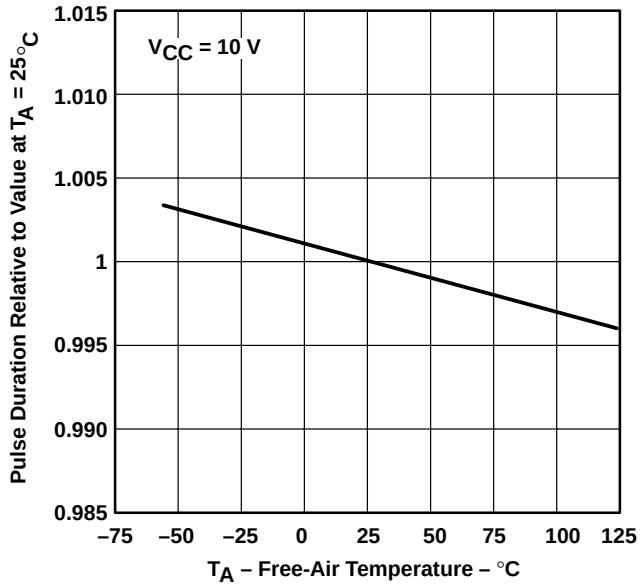


Figure 7

PROPAGATION DELAY TIME vs LOWEST VOLTAGE LEVEL OF TRIGGER PULSE

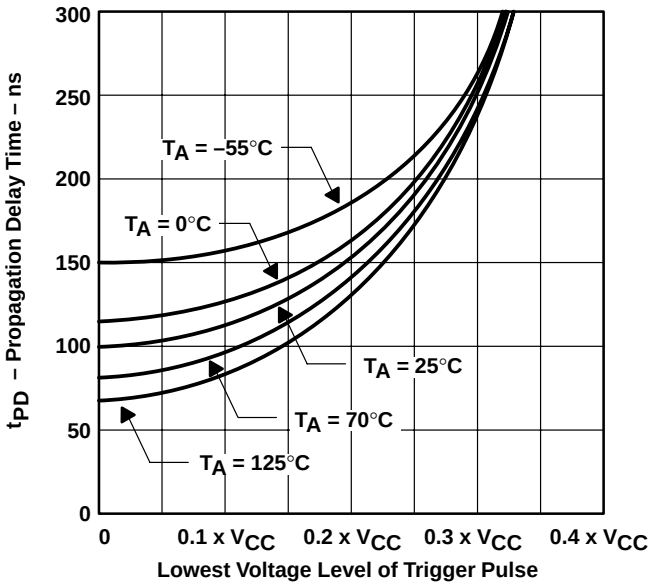


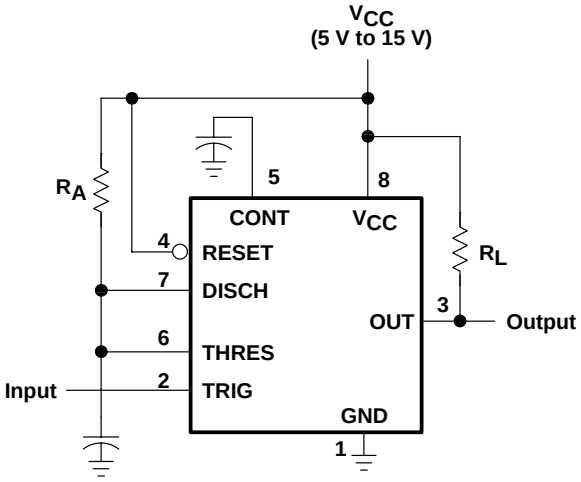
Figure 8

† Data for temperatures below 0°C and above 70°C are applicable for SE555 circuits only.

APPLICATION INFORMATION

monostable operation

For monostable operation, any of these timers may be connected as shown in Figure 9. If the output is low, application of a negative-going pulse to TRIG sets the flip-flop ($\overline{Q}$ goes low), drives the output high, and turns off Q1. Capacitor C is then charged through R_A until the voltage across the capacitor reaches the threshold voltage of THRES input. If TRIG has returned to a high level, the output of the threshold comparator will reset the flip-flop ($\overline{Q}$ goes high), drive the output low, and discharge C through Q1.



Pin numbers shown are for the D, JG, and P packages.

Figure 9. Circuit for Monostable Operation

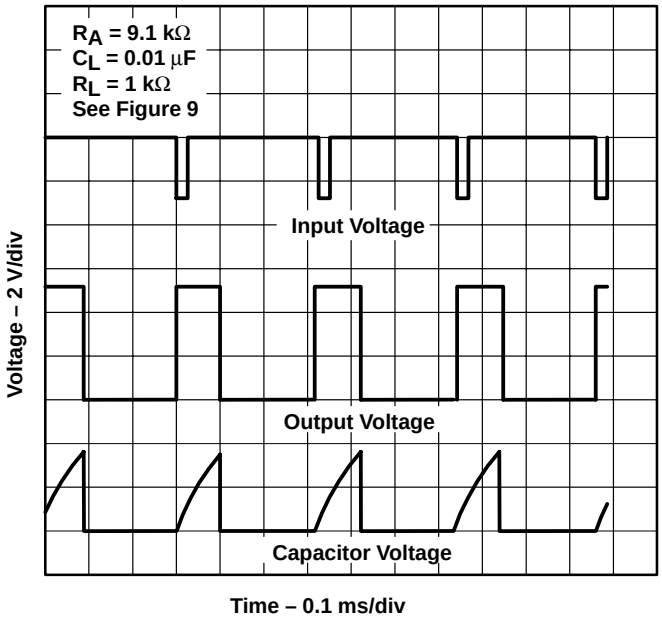


Figure 10. Typical Monostable Waveforms

Monostable operation is initiated when TRIG voltage falls below the trigger threshold. Once initiated, the sequence ends only if TRIG is high at the end of the timing interval. Because of the threshold level and saturation voltage of Q1, the output pulse duration is approximately $t_w = 1.1 R_A C$. Figure 11 is a plot of the time constant for various values of R_A and C. The threshold levels and charge rates are both directly proportional to the supply voltage, V_{CC}. The timing interval is therefore independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval discharges C and re-initiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when RESET is not used, it should be connected to V_{CC}.

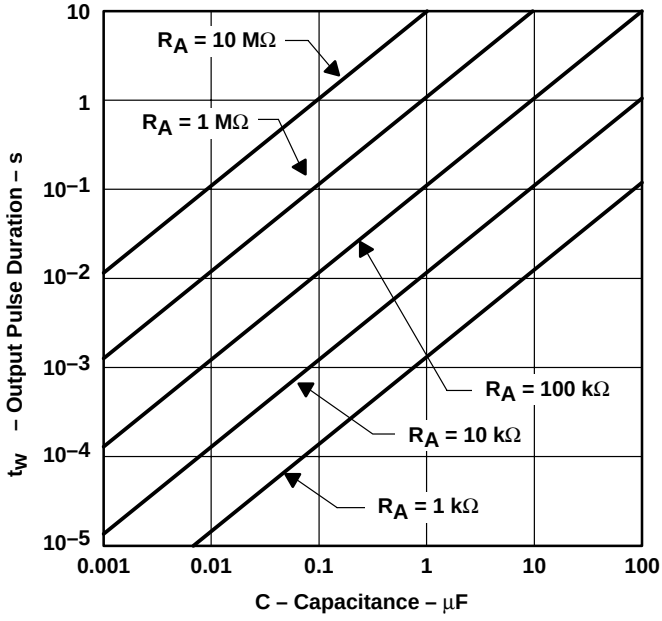


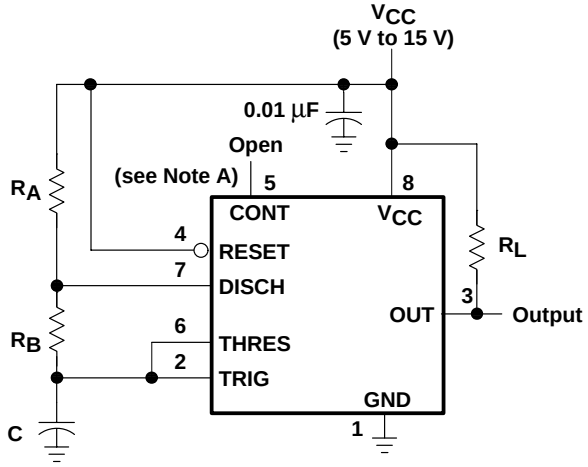
Figure 11. Output Pulse Duration vs Capacitance

APPLICATION INFORMATION

astable operation

As shown in Figure 12, adding a second resistor, R_B, to the circuit of Figure 9 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multivibrator. The capacitor C will charge through R_A and R_B and then discharge through R_B only. The duty cycle may be controlled, therefore, by the values of R_A and R_B.

This astable connection results in capacitor C charging and discharging between the threshold-voltage level ($\approx 0.67 \bullet V_{CC}$) and the trigger-voltage level ($\approx 0.33 \bullet V_{CC}$). As in the monostable circuit, charge and discharge times (and therefore the frequency and duty cycle) are independent of the supply voltage.



Pin numbrs shown are for the D, JG, and P packages.

NOTE A: Decoupling CONT voltage to ground with a capacitor may improve operation. This should be evaluated for individual applications.

Figure 12. Circuit for Astable Operation

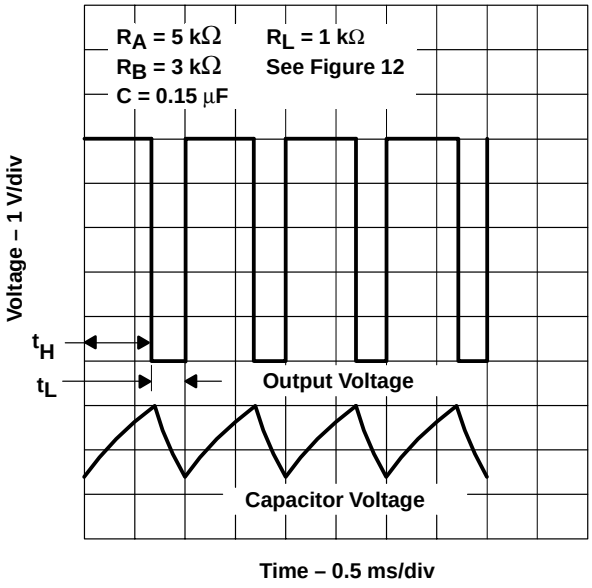


Figure 13. Typical Astable Waveforms

APPLICATION INFORMATION

Figure 13 shows typical waveforms generated during astable operation. The output high-level duration t_H and low-level duration t_L may be calculated as follows:

$$t_H = 0.693\ (R_A + R_B)\ C$$

$$t_L = 0.693\ (R_B)\ C$$

Other useful relationships are shown below.

$$\text{period} = t_H + t_L = 0.693\ (R_A + 2R_B)\ C$$

$$\text{frequency} \approx \frac{1.44}{(R_A + 2R_B)\ C}$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} = \frac{R_B}{R_A + 2R_B}$$

$$\text{Output waveform duty cycle} = \frac{t_H}{t_H + t_L} = 1 - \frac{R_B}{R_A + 2R_B}$$

$$\text{Low-to-high ratio} = \frac{t_L}{t_H} = \frac{R_B}{R_A + R_B}$$

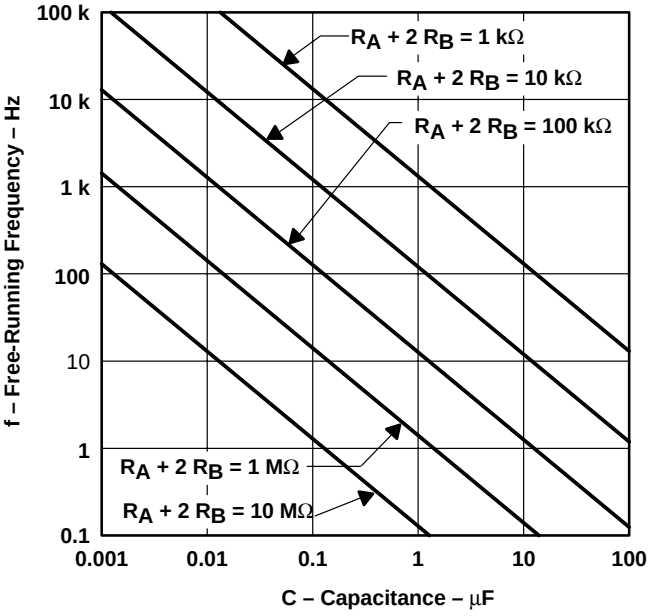
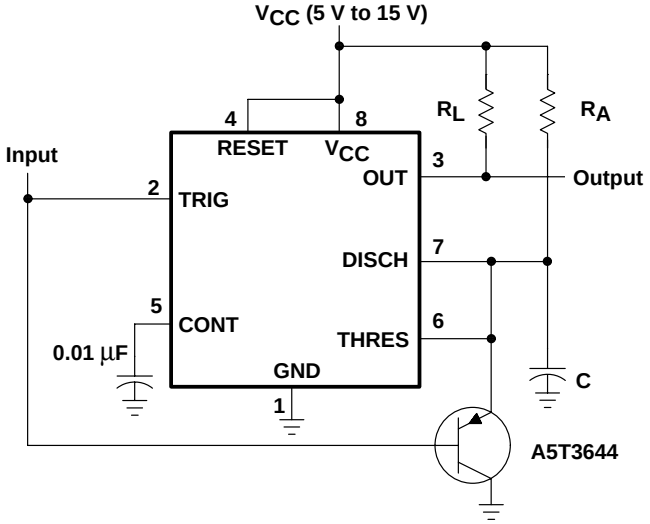


Figure 14. Free-Running Frequency

missing-pulse detector

The circuit shown in Figure 15 may be used to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is continuously retriggered by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse as illustrated in Figure 16.



Pin numbers shown are shown for the D, JG, and P packages.

Figure 15. Circuit for Missing Pulse Detector

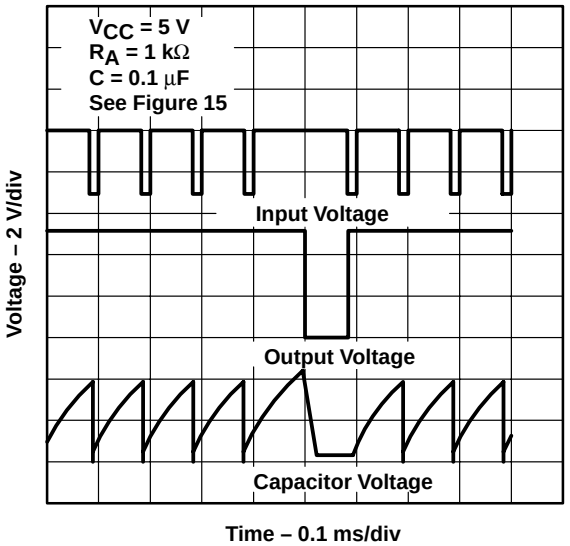


Figure 16. Circuit for Missing Pulse Detector

APPLICATION INFORMATION

frequency divider

By adjusting the length of the timing cycle, the basic circuit of Figure 9 can be made to operate as a frequency divider. Figure 17 illustrates a divide-by-three circuit that makes use of the fact that retriggering cannot occur during the timing cycle.

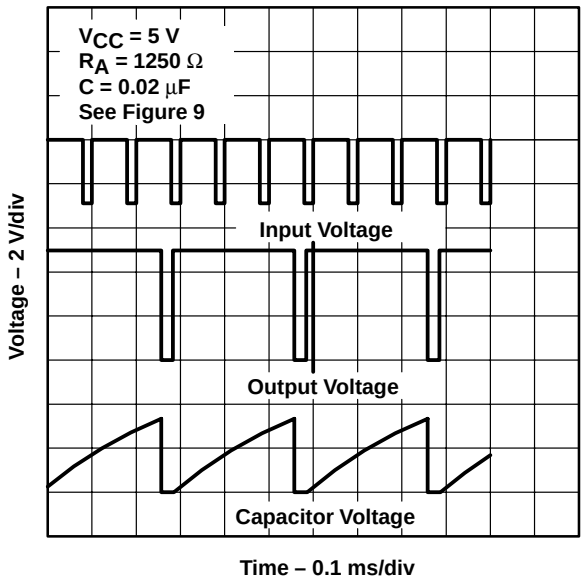
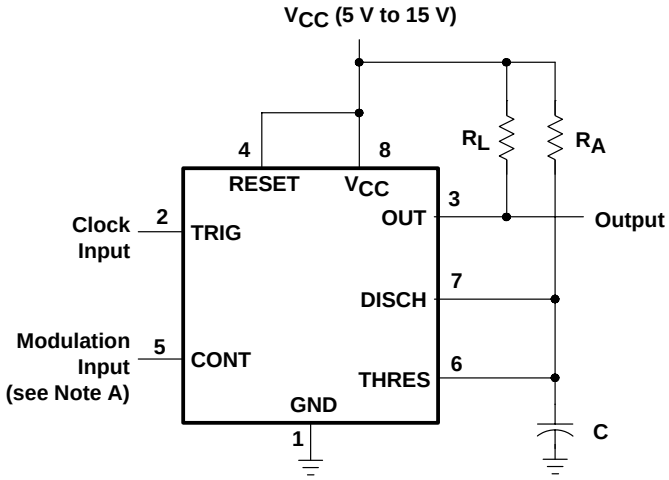


Figure 17. Divide-By-Three Circuit Waveforms

pulse-width modulation

The operation of the timer may be modified by modulating the internal threshold and trigger voltages, which is accomplished by applying an external voltage (or current) to CONT. Figure 18 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. Figure 19 illustrates the resulting output pulse-width modulation. While a sine-wave modulation signal is illustrated, any wave shape could be used.

APPLICATION INFORMATION



Pin numbers shown are for the D, JG, and P packages only.

NOTE A: The modulating signal may be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 18. Circuit for Pulse-Width Modulation

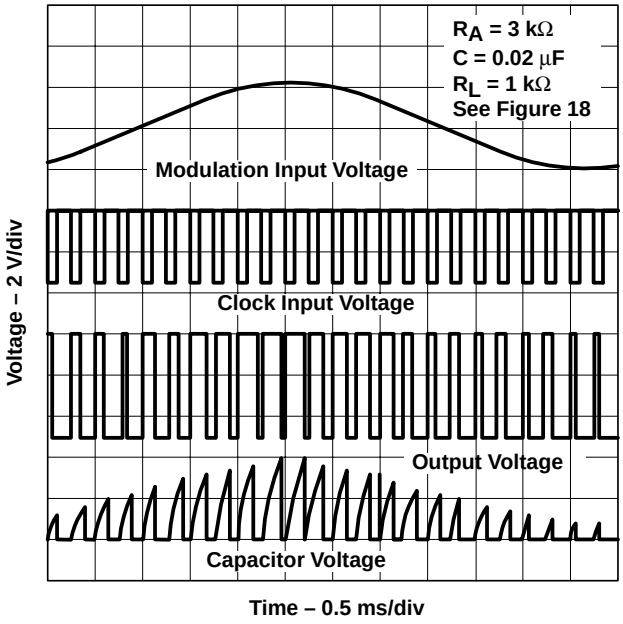
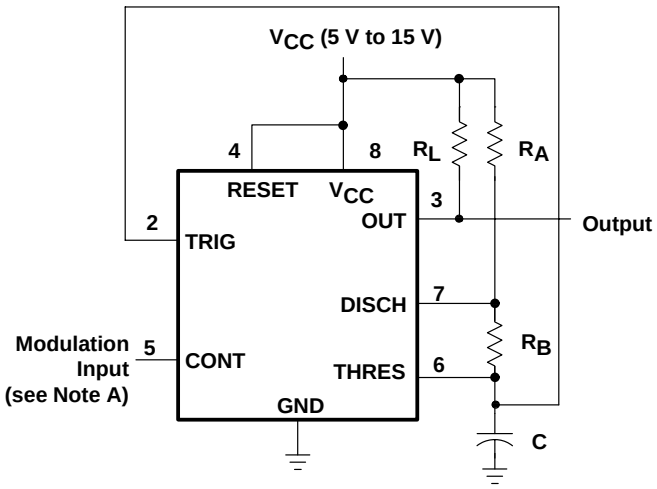


Figure 19. Pulse-Width Modulation Waveforms

pulse-position modulation

As shown in Figure 20, any of these timers may be used as a pulse-position modulator. This application modulates the threshold voltage, and thereby the time delay, of a free-running oscillator. Figure 21 illustrates a triangular-wave modulation signal for such a circuit; however, any wave shape could be used.



Pin numbers shown are for the D, JG, and P packages only.

NOTE A: The modulating signal may be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 20. Circuit for Pulse-Position Modulation

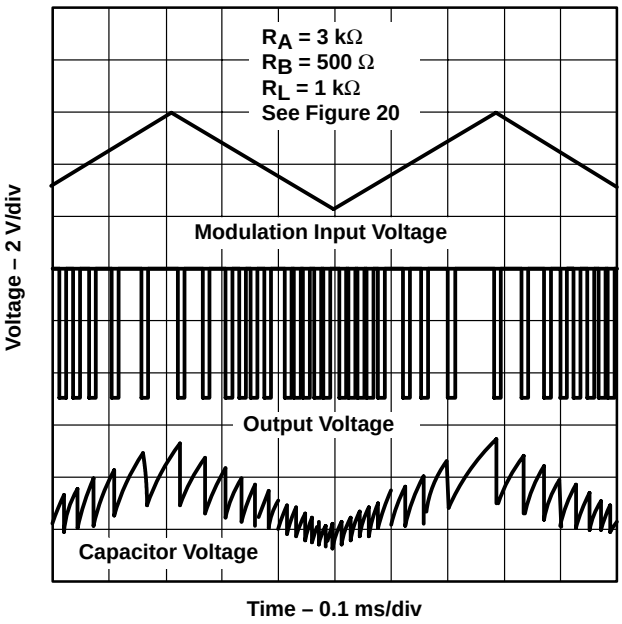
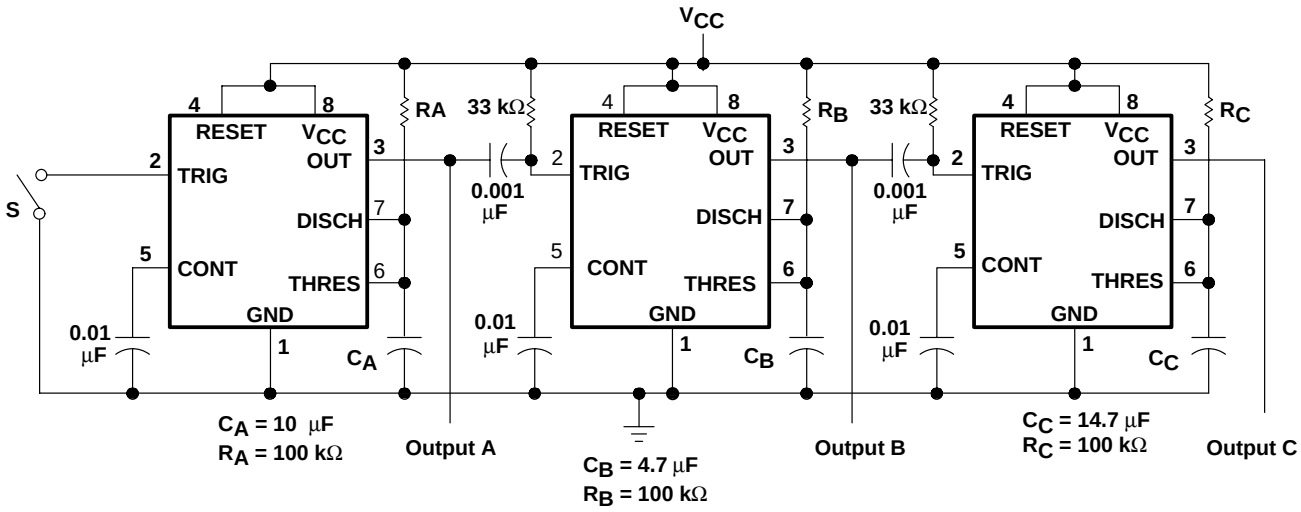


Figure 21. Pulse-Position-Modulation Waveforms

APPLICATION INFORMATION

sequential timer



S closes momentarily at t = 0.
Pin numbers shown are for the D, JG, and P packages only.

Figure 22. Sequential Timer Circuit

Many applications, such as computers, require signals for initializing conditions during start-up. Other applications, such as test equipment, require activation of test signals in sequence. These timing circuits may be connected to provide such sequential control. The timers may be used in various combinations of astable or monostable circuit connections, with or without modulation, for extremely flexible waveform control. Figure 22 illustrates a sequencer circuit with possible applications in many systems, and Figure 23 shows the output waveforms.

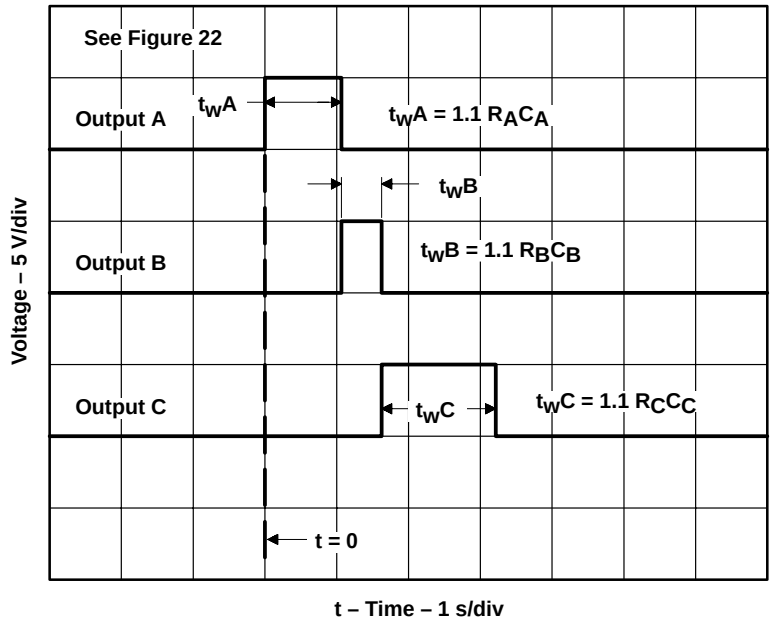


Figure 23. Sequential Timer Waveforms

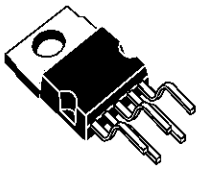
SGS-THOMSON MICROELECTRONICS

TDA2040

20W Hi-Fi AUDIO POWER AMPLIFIER

DESCRIPTION

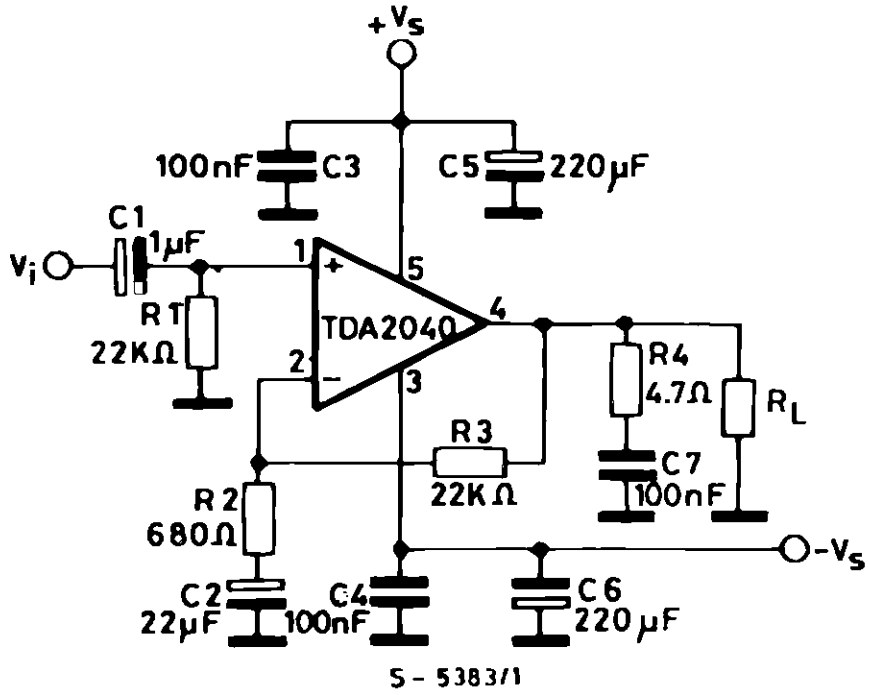
The TDA2040 is a monolithic integrated circuit in Pentawatt® package, intended for use as an audio class AB amplifier. Typically it provides 22W output power (d = 0.5%) at V_S = 32V/4Ω . The TDA2040 provides high output current and has very low harmonic and cross-over distortion. Further the device incorporates a patented short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A thermal shut-down system is also included.



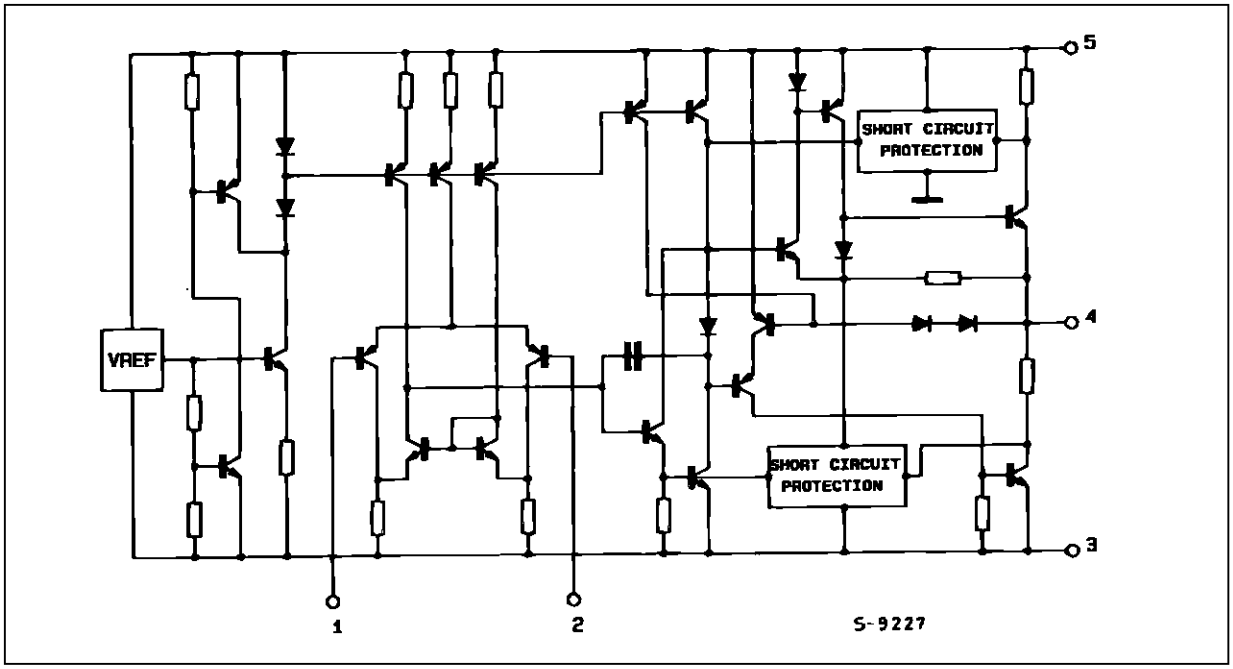
PENTAWATT

ORDERING NUMBER : TDA2040V

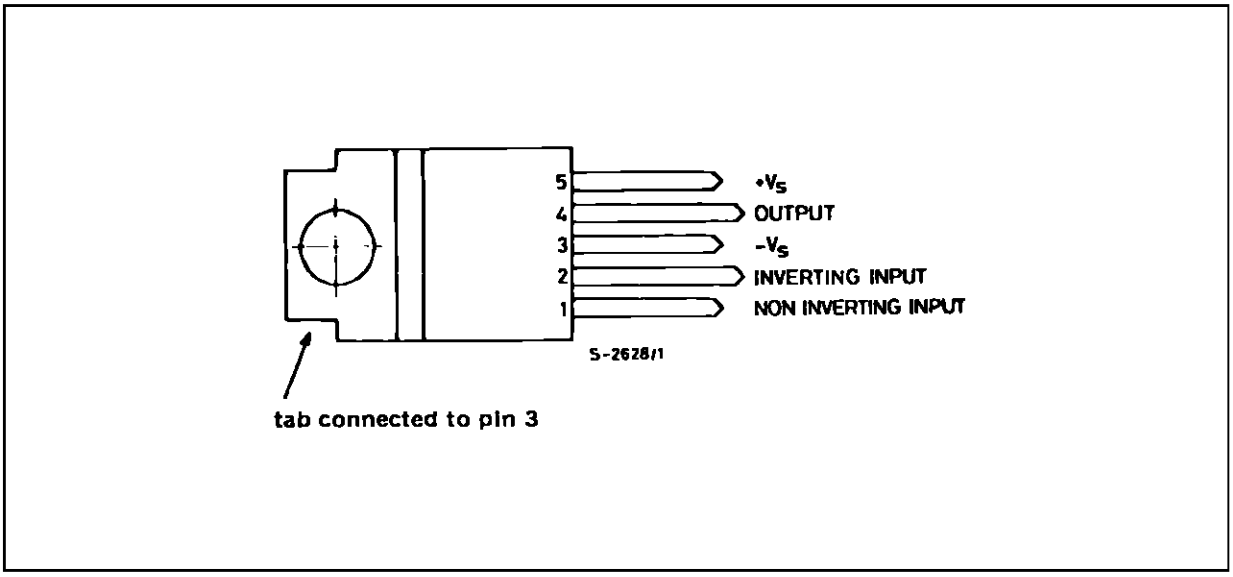
TEST CIRCUIT



SCHEMATIC DIAGRAM



PIN CONNECTION



THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max.	3	°C/W

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	± 20	V
V_i	Input Voltage	V_s	
V_i	Differential Input Voltage	± 15	V
I_o	Output Peak Current (internally limited)	4	A
P_{tot}	Power Dissipation at T_{case} = 75 °C	25	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to + 150	°C

ELECTRICAL CHARACTERISTICS
(refer to the test circuit, V_S = ± 16V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		± 2.5		± 20	V
I_d	Quiescent Drain Current	V_s = ± 4.5V V_s = ± 20V		 45	30 100	mA mA
I_b	Input Bias Current	V_s = ± 20V		0.3	1	µA
V_{os}	Input Offset Voltage	V_s = ± 20V		± 2	± 20	mV
I_{os}	Input Offset Current				± 200	nA
P_o	Output Power	d = 0.5%, T_{case} = 60°C f = 1kHz R_L = 4Ω R_L = 8Ω f = 15kHz R_L = 4Ω	 20 15	 22 12 18		W
BW	Power Bandwidth	P_o = 1W, R_L = 4Ω		100		kHz
G_v	Open Loop Voltage Gain	f = 1kHz		80		dB
G_v	Closed Loop Voltage Gain	f = 1kHz	29.5	30	30.5	dB
d	Total Harmonic Distortion	P_o = 0.1 to 10W, R_L = 4Ω f = 40 to 15000Hz f = 1kHz		 0.08 0.03		%
e_N	Input Noise Voltage	B = Curve A B = 22Hz to 22kHz		2 3	 10	µV µV
i_N	Input Noise Current	B = Curve A B = 22Hz to 22kHz		50 80	 200	pA
R_i	Input Resistance (pin 1)		0.5	5		MΩ
SVR	Supply Voltage Rejection	R_L = 4Ω, R_g = 22kΩ, G_v = 30dB f = 100Hz, V_{ripple} = 0.5V_{RMS}	40	50		dB
η	Efficiency	f = 1kHz P_o = 12W R_L = 8 Ω P_o = 22W R_L = 4 Ω		 66 63		%
T_j	Thermal Shut-down Junction Temperature			145		°C

Figure 1 : Output Power versus Supply Voltage

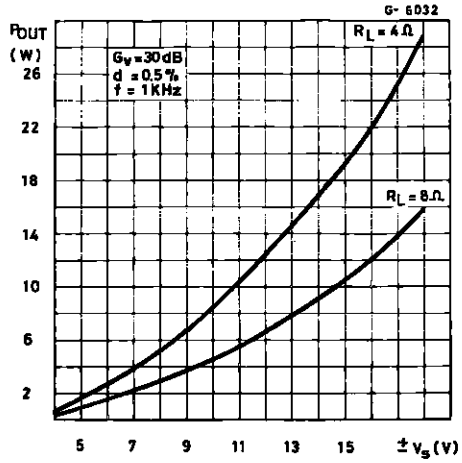


Figure 2 : Output Power versus Supply Voltage

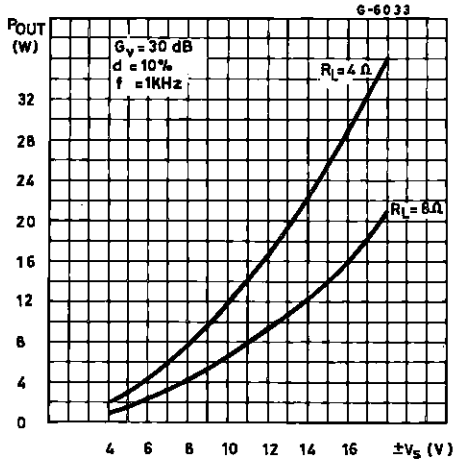


Figure 3 : Output Power versus Supply Voltage

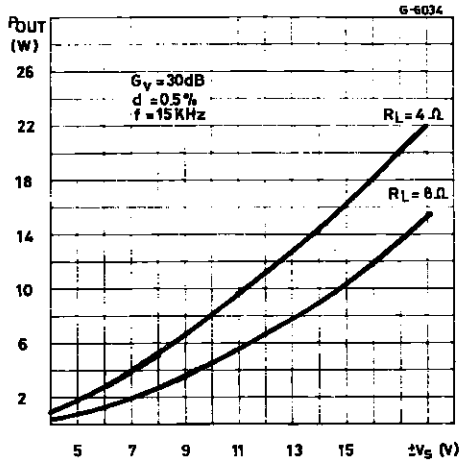


Figure 4 : Distortion versus Frequency

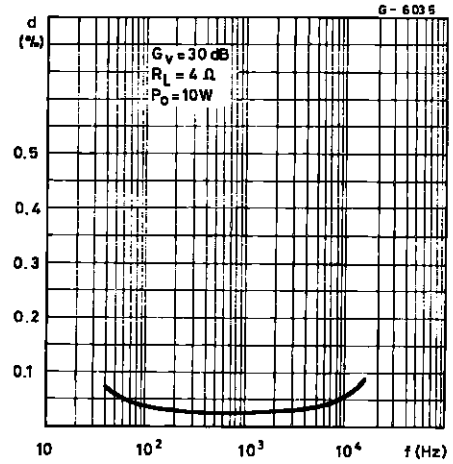


Figure 5 : Supply Voltage Rejection versus Frequency

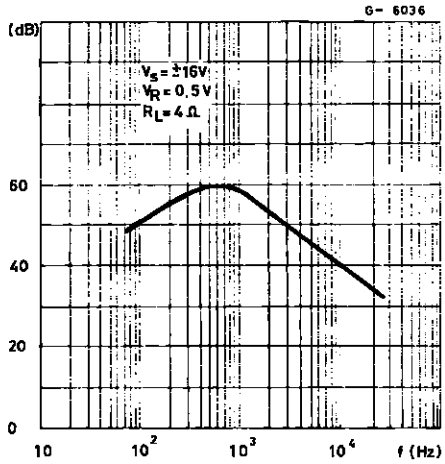


Figure 6 : Supply Voltage Rejection versus Voltage Gain

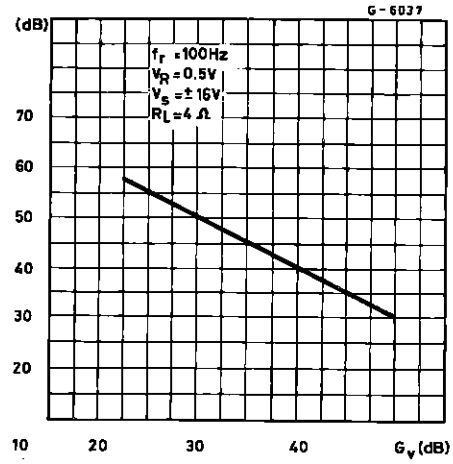


Figure 7 : Quiescent Drain Current versus Supply Voltage

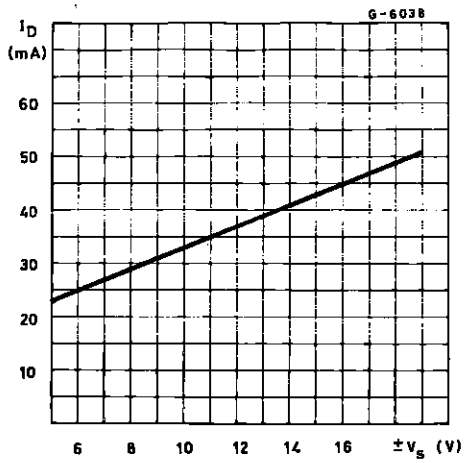


Figure 8 : Open Loop Gain versus Frequency

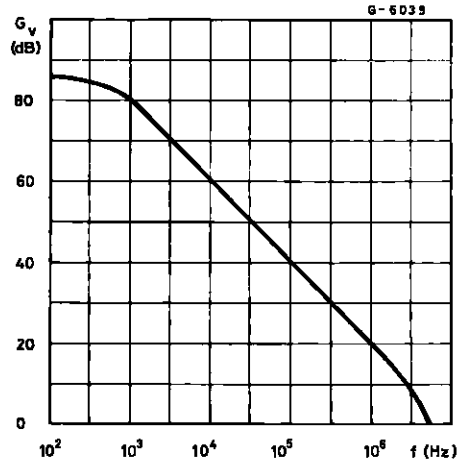


Figure 9 : Power Dissipation versus Output Power

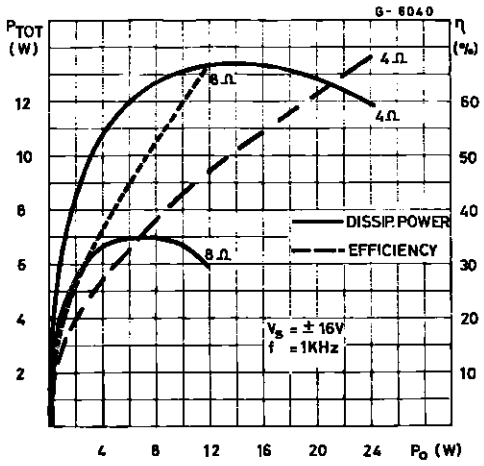


Figure 10 : Amplifier with Split Power Supply

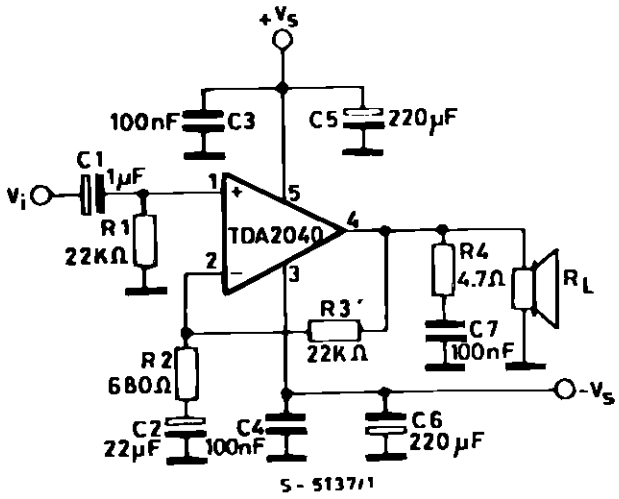


Figure 11 : P.C. Board and Components Layout for the Circuit of Figure 10 (1:1 scale)

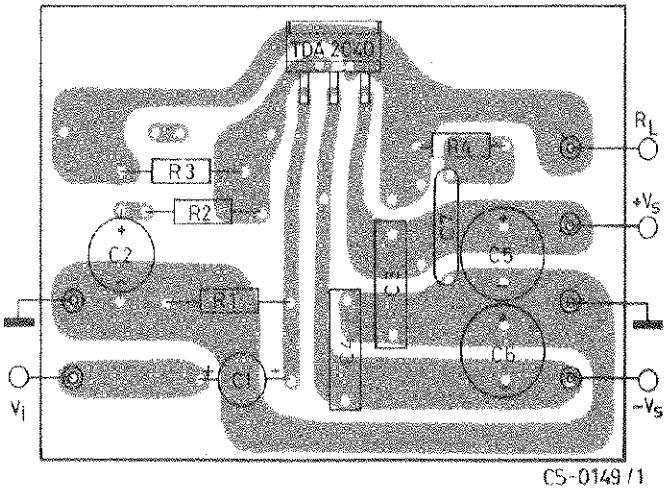
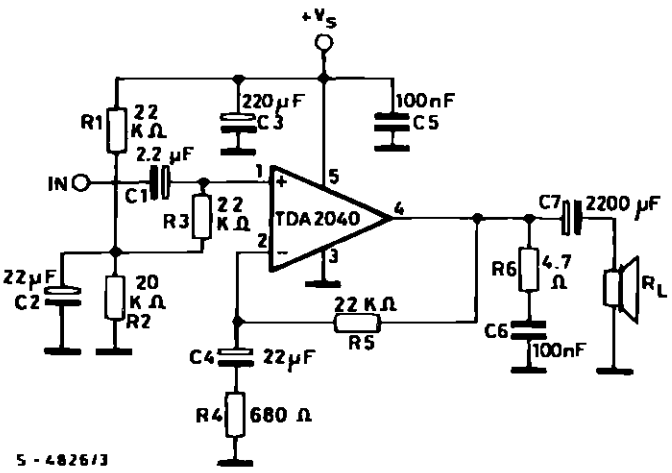


Figure 12 : Amplifier with Split Power Supply (see Note)



Note : In this case of highly inductive loads protection diodes may be necessary.

Figure 13 : P.C. Board and Components Layout for the Circuit of Figure 12 (1:1 scale)

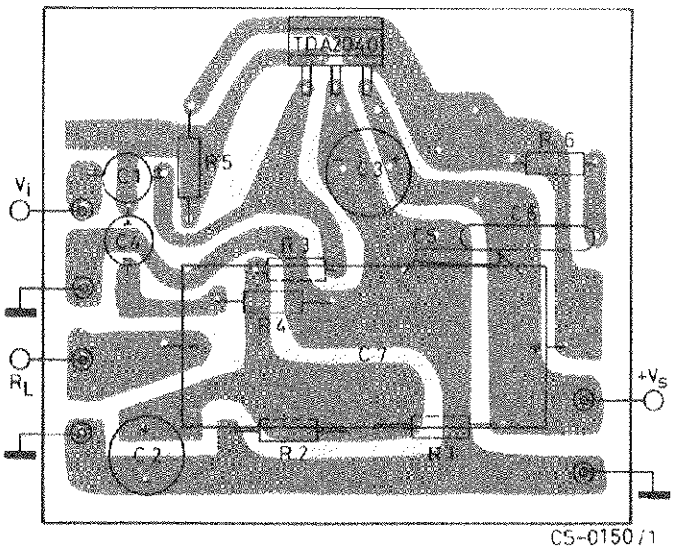


Figure 14 : 30W Bridge Amplifier with Split Power Supply

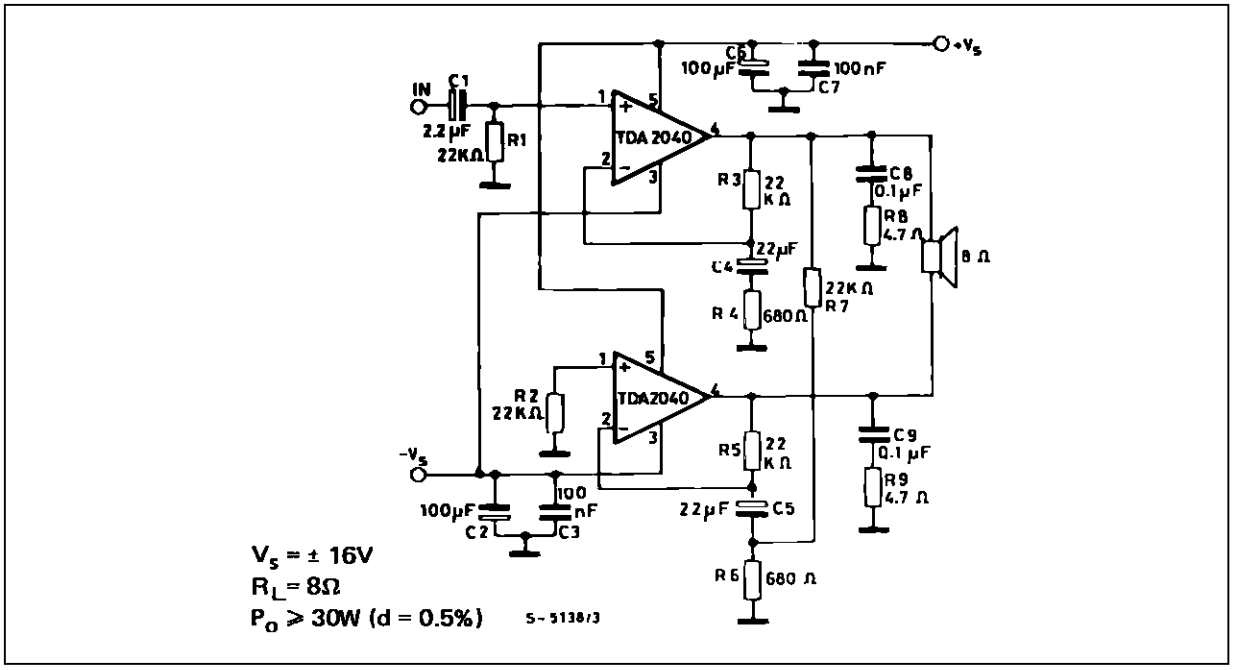


Figure 15 : P.C. Board and Components Layout for the Circuit of Figure 14 (1:1 scale)

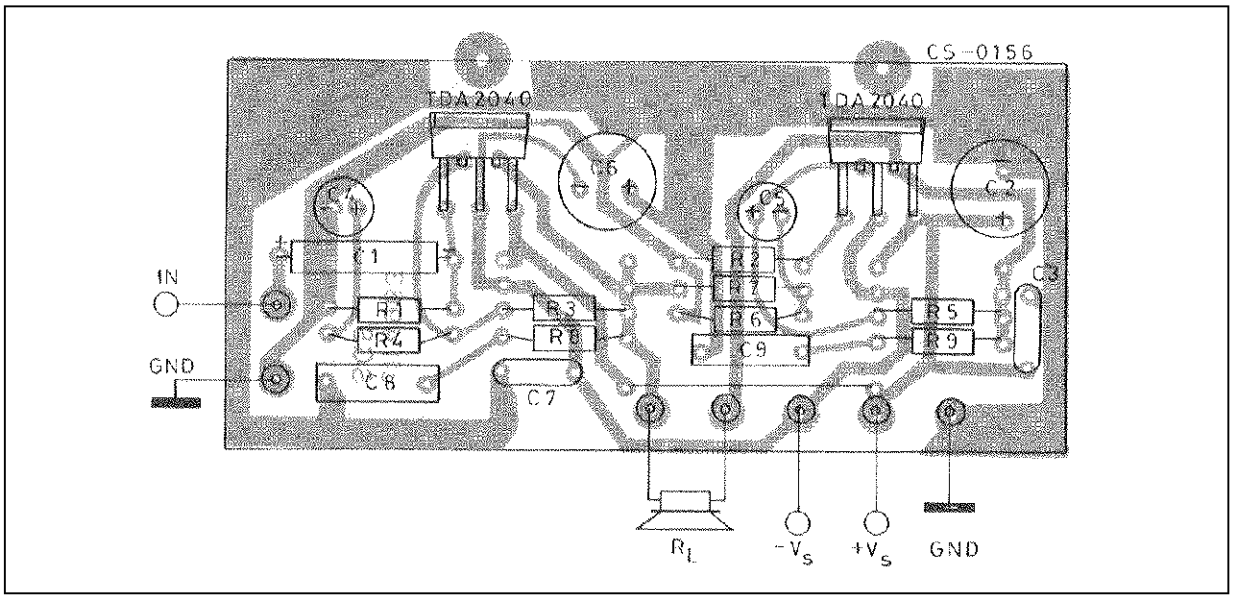


Figure 16 : Two Way Hi-Fi System with Active Crossover

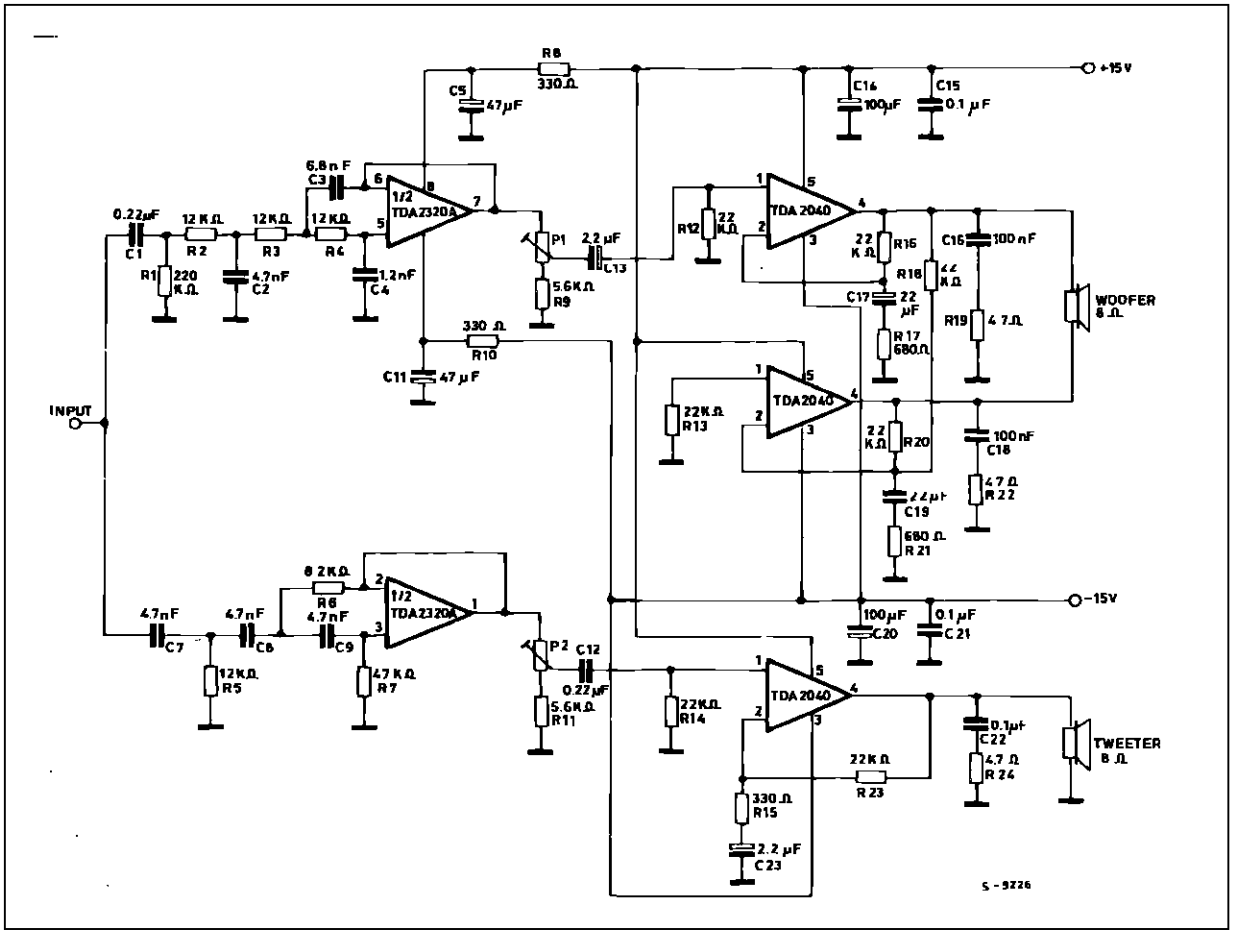


Figure 17 : P.C. Board and Components Layout for the Circuit of Figure 16 (1:1 scale)

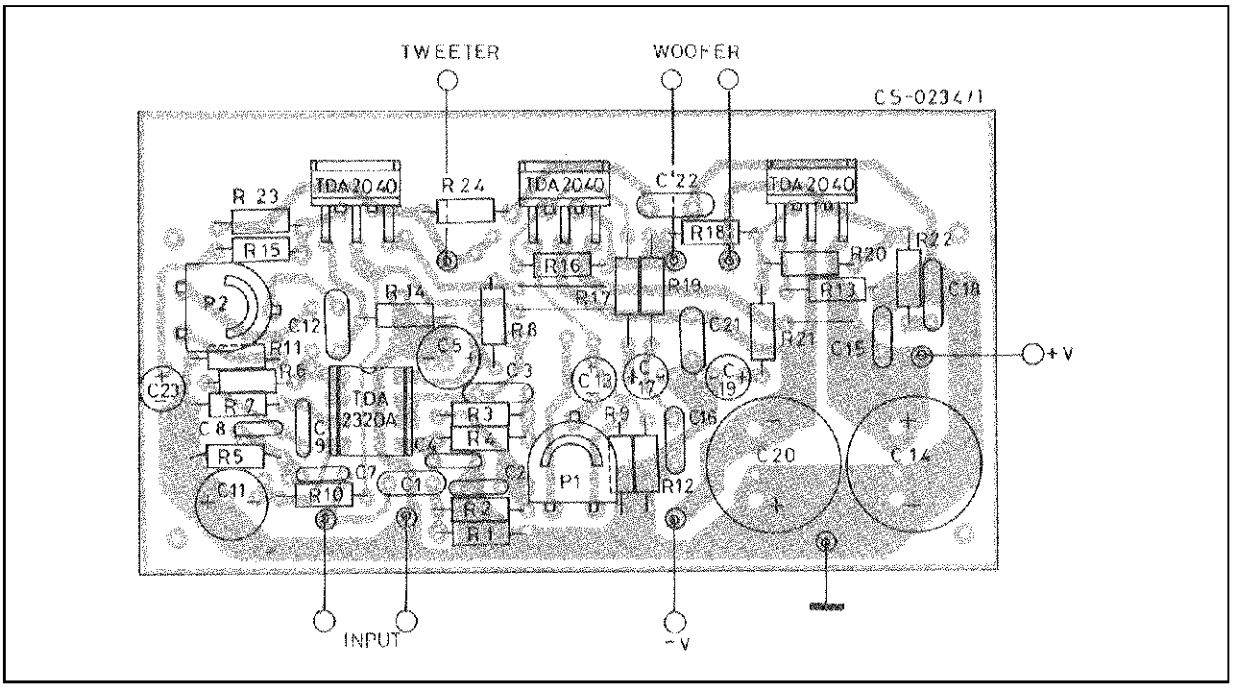


Figure 18 : Frequency Response

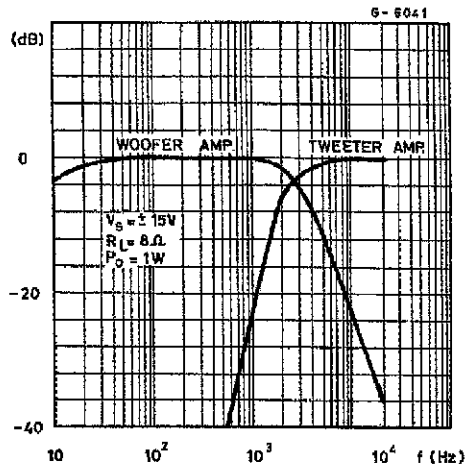
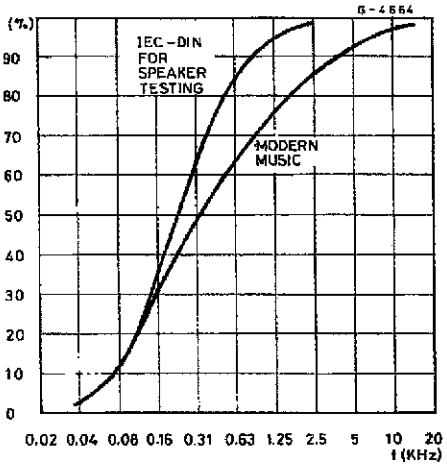


Figure 19 : Power Distribution versus Frequency



MULTIWAY SPEAKER SYSTEMS AND ACTIVE BOXES

Multiway loudspeaker systems provide the best possible acoustic performance since each loudspeaker is specially designed and optimized to handle a limited range of frequencies. Commonly, these loudspeaker systems divide the audio spectrum into two, three or four bands.

To maintain a flat frequency response over the Hi-Fi audio range the bands covered by each loudspeaker must overlap slightly. Imbalance between the loudspeakers produces unacceptable results therefore it is important to ensure that each unit generates the correct amount of acoustic energy for its segment of the audio spectrum. In this respect it is also important to know the energy distribution of the music spectrum determine the cutoff frequencies of the crossover filters (see Figure 19). As an example, a 100W three-way system with crossover frequencies of 400Hz and 3kHz would require 50W for the woofer, 35W for the midrange unit and 15W for the tweeter.

Both active and passive filters can be used for crossovers but today active filters cost significantly less than a good passive filter using air-cored inductors and non-electrolytic capacitors. In addition, active filters do not suffer from the typical defects of passive filters :

- power loss
- increased impedance seen by the loudspeaker (lower damping)
- difficulty of precise design due to variable loudspeaker impedance

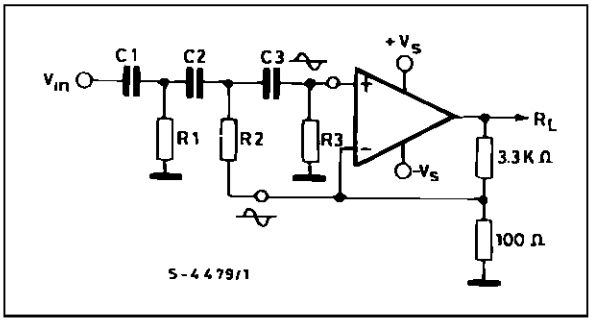
Obviously, active crossovers can only be used if a power amplifier is provided for each drive unit. This makes it particularly interesting and economically sound to use monolithic power amplifiers. In some applications, complex filters are not really necessary and simple RC low-pass and high-pass networks (6dB/octave) can be recommended.

The results obtained are excellent because this is the best type of audio filter and the only one free from phase and transient distortion.

The rather poor out of band attenuation of single RC filters means that the loudspeaker must operate linearly well beyond the crossover frequency to avoid distortion.

A more effective solution, named "Active Power Filter" by SGS is shown in Figure 20.

Figure 20 : Active Power Filter



The proposed circuit can realize combined power amplifiers and 12dB/octave or 18dB/octave high-pass or low-pass filters.

In practice, at the input pins of the amplifier two equal and in-phase voltages are available, as required for the active filter operation.

The impedance at the pin (-) is of the order of 100Ω, while that of the pin (+) is very high, which is also what was wanted.

C1 = C2 = C3	R1	R2	R3
22 nF	8.2 kΩ	5.6 kΩ	33 kΩ

The component values calculated for f_c = 900Hz using a Bessel 3rd order Sallen and Key structure are :

In the block diagram of Figure 21 is represented an active loudspeaker system completely realized using power integrated circuit, rather than the traditional discrete transistors on hybrids, very high quality is obtained by driving the audio spectrum into three bands using active crossovers (TDA2320A) and a separate amplifier and loudspeakers for each band.

A modern subwoofer/midrange/tweeter solution is used.

PRATICAL CONSIDERATION

Printed Circuit Board

The layout shown in Figure 11 should be adopted by the designers. If different layouts are used, the ground points of input 1 and input 2 must be well decoupled from the gorund return of the output in which a high current flows.

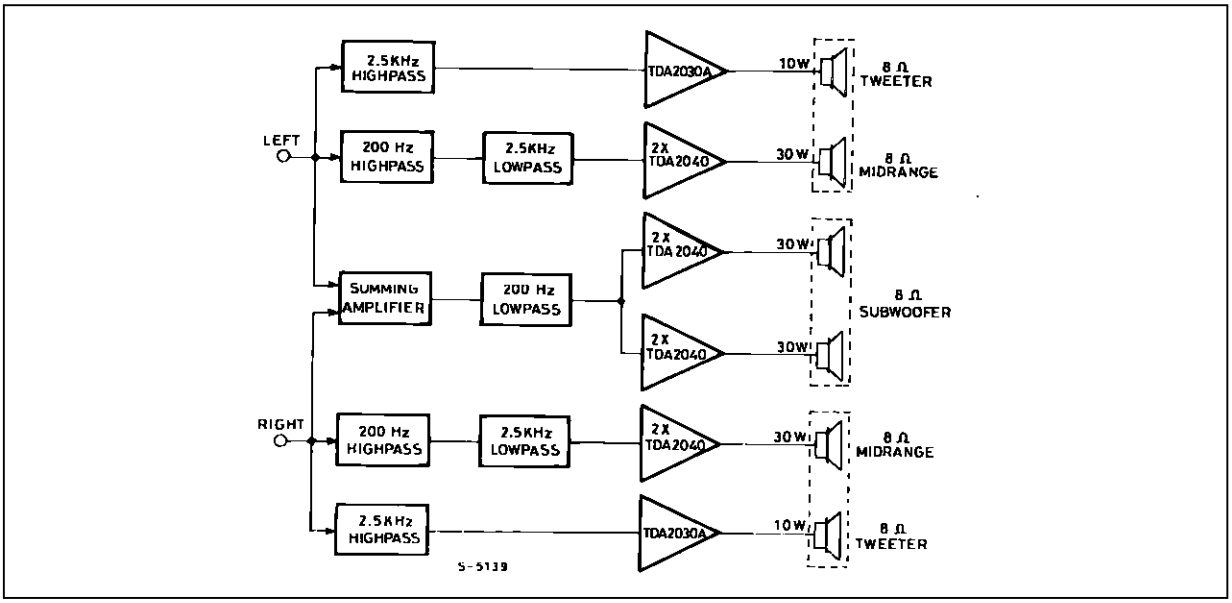
Assembly Suggestion

No electrical isolation is needed between the package and the heatsink with single supply voltage configuration.

Application Suggestions

The recommended values of the components are those shown on application circuit of Fig. 10. Different values can be used. The following table can help the designer.

Figure 21 : High Power Active Loudspeaker System using TDA2030A and TDA2040

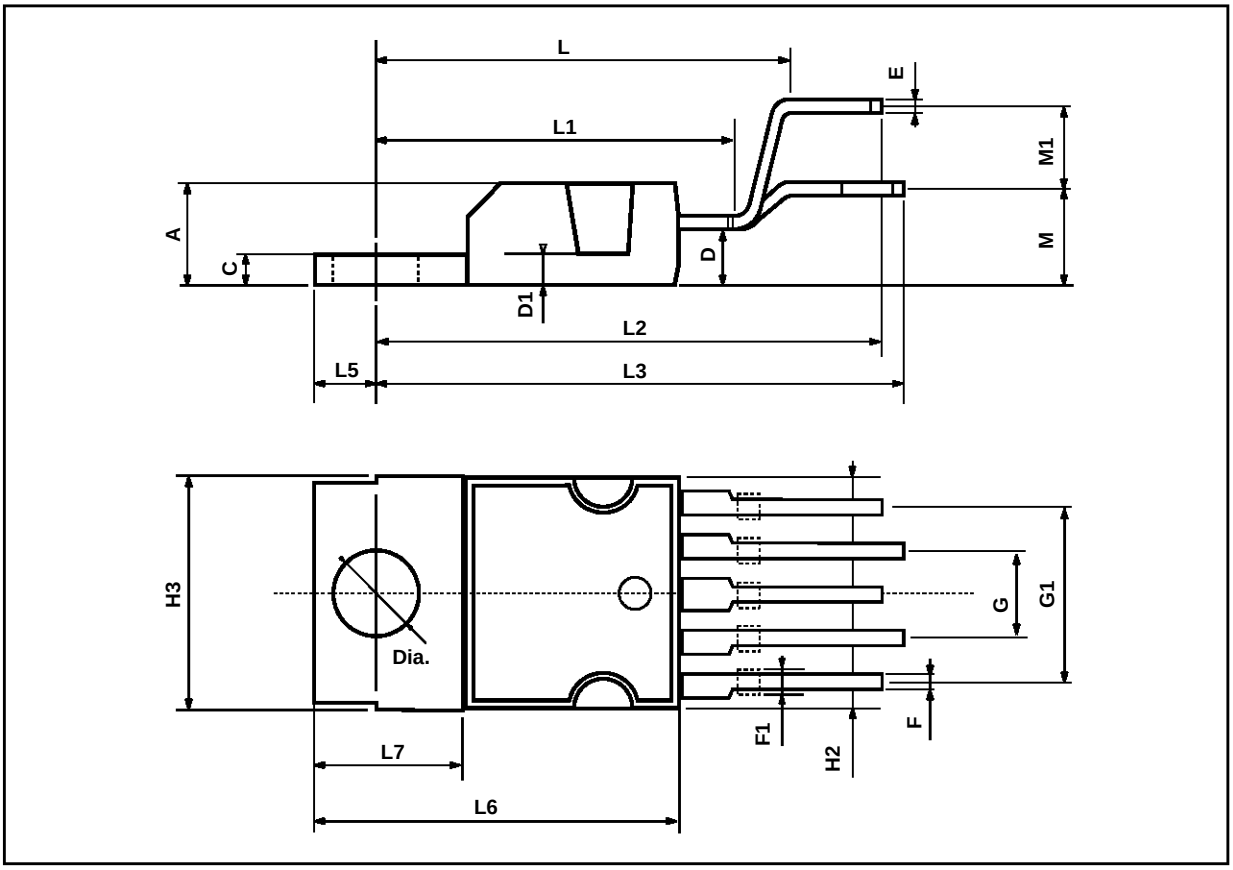


Comp.	Recom. Value	Purpose	Larger than Recommended Value	Smaller than Recommended Value
R1	22kΩ	Non inverting input biasing	Increase of input impedance	Decrease of input impedance
R2	680Ω	Closed loop gain setting	Decrease of gain (*)	Increase of gain
R3	22kΩ	Closed loop gain setting	Increase of gain	Decrease of gain (*)
R4	4.7Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads	
C1	1µF	Input DC decoupling		Increase of low frequencies cut-off
C2	22µF	Inverting DC decoupling		Increase of low frequencies cut-off
C3, C4	0.1µF	Supply voltage bypass		Danger of oscillation
C5, C6	220µF	Supply voltage bypass		Danger of oscillation
C7	0.1µF	Frequency stability		Danger of oscillation

(*) The value of closed loop gain must be higher than 24dB

PENTAWATT PACKAGE MECHANICAL DATA

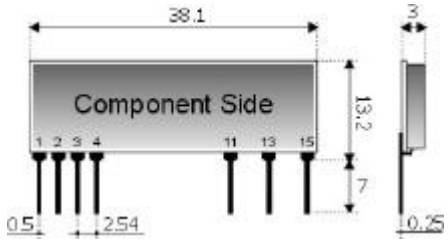
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.8		1.05	0.031		0.041
F1	1		1.4	0.039		0.055
G		3.4		0.126	0.134	0.142
G1		6.8		0.260	0.268	0.276
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		17.85			0.703	
L1		15.75			0.620	
L2		21.4			0.843	
L3		22.5			0.886	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		4.5			0.177	
M1		4			0.157	
Dia	3.65		3.85	0.144		0.152

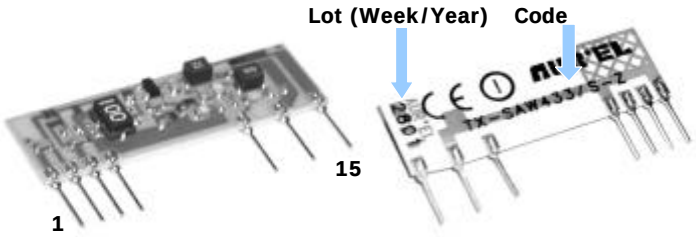


TX-SAW / 433 s-Z Transmitter

SAW Transmitter module with external antenna, for utilisations with ON-OFF modulation of a RF carrier with digital data.

Pin-out





Connections

Pin 1-4-13	**Ground**	GND Connections. To be externally connected to a single ground plate. (see fig. 3)
Pin 2	**Input Mod.**	TTL 0÷5V type data input with a minimum 5KΩ resistance. Connection utilized only if the supply to pin 15 is +12V ±10% (see fig. 2)
Pin 3	**Input Mod.**	TTL 0÷5V type data input with a minimum 5KΩ resistance. Connection utilized only if the supply to pin 15 is +5V ±10% (see fig. 2)
Pin 11	**RF output**	RF output with a characteristic impedence of 50Ω
Pin 15	**+V**	Connection to the positive pole of the +5V ±10% supply

Max voltage values allowed

Description	Max	Unity	Remarks
Voltage supply (Vs) to pin 15	13,5	V	

Technical features [ETS 300 200]

Description	Min	Typical	Max	Unity	Remarks
Working frequency centre	433.82	433.92	434.02	MHz	See notes 1 and 2
Voltage supply (Vs)	4.5	5	5.5	V	
Absorbed current		4		mA	
RF output power (E.R.P.)			+10	dBm	See note 1
Output impedance pin 11		50		Ω	
RF spurious emissions		-50		dBm	See note 1
Modulation frequency			4	kHz	
Input high logic level	4.5	5	5.5	V	
Input low logic level	0		0.2	V	
Working temperature	-20		+80	°C	See fig. 5
Working temperature [ETS 300 200]	-20		+55	°C	See fig. 5
Dimensions	38.1 x 13.2 x 3 mm				See Pin-out

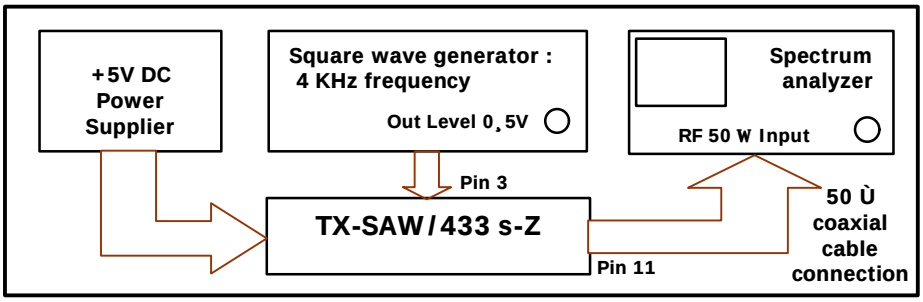
Note1: *Values have been obtained by applying the test system shown in Fig. 1 and maximum 5,5 V power supply.*
Note2: *The minimum and maximum showed values are determined by the device's construction tolerance.*
To define the working frequency of the device, add to these values the deviation caused by the thermal variations (see fig. 3).
Note3: *To keep the parameters within the limits established by the rules in force, (see para. "Reference Rules"), it is recommended to supply the circuit with not more than 5,5V and to comply with all the recommendations specified in para "Device usage".*

Messrs AUR°EL declines all responsibilities in case the a.m. recommendations are disregarded.

Technical features are subject to change without notice. AUR°EL S.p.A does not feel responsible for any damage caused by the device's misuse.

The declared technical features have been obtained by applying the following testing system:

Fig. 1



Device usage

In order to obtain the performances described in the technical specifications and to comply with the operating conditions, which characterize the Certification, the transmitter has to be mounted on a printed circuit, and keep into consideration what follows:

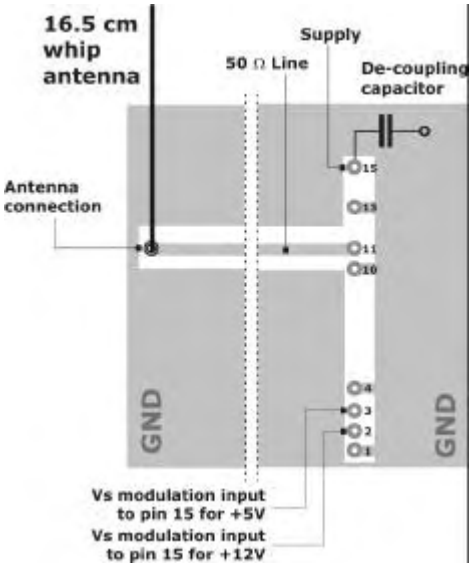
5V dc supply

1. The transmitter must be supplied by a very low voltage source, safely protected against short circuits.
2. Maximum voltage variations allowed: ± 0,5 V.
3. De-coupling, next to the transmitter, by means of a minimum 100.000 pF ceramic capacitor.

Ground

1. It must surround at the best the welding area of the transmitter. The circuit must be double layer, with throughout vias to the ground planes, approximately each 15 mm.
2. It must be properly dimensioned, especially in the antenna connection area, in case a radiating whip antenna is fitted in it (an area of approximately 50 mm radius is suggested).

Fig. 2



50 Ohm line

1. It must be the shortest as possible.
2. 1,8 mm wide for 1 mm thick FR4 printed circuits and 2,9 mm wide for 1,6 mm thick FR4 printed circuits. It must be kept 2 mm away from the ground circuit on the same side.
3. On the opposite side a ground circuit area must be present.

Antenna connection

1. It may be utilized as the direct connection point for the radiating whip antenna.
2. It can bear the connection of the central wire of a 50 Ω coaxial cable. Be sure that the braid is welded to the ground in a close point.

Antenna

1. A **whip** antenna, 16,5 mm long and approximately 1 mm dia, brass or copper wire made, must be connected to the RF output of the transmitter (pin 11), (see fig. 2).
2. The antenna body must be keep straight as much as possible and it must be free from other circuits or metal parts (5 cm minimum suggested distance.)
3. It can be utilized either vertically or horizontally, provided that a good ground plane surrounds the connection point between antenna and transmitter output.

N.B: As an alternative to the a.m. antenna it is possible to fit the whip model manufactured by **AUR°EL** (see related Data Sheet and Application Notes).
By fitting whips too different from the described ones, the EEC Certification is not assured.

Other components

1. Keep the transmitter separate from all other components of the circuit (more than 5 mm).

2. Keep particularly far away and shielded all microprocessors and their clock circuits.
3. Do not fit components around the 50 Ohm line. Keep them at least at 5 mm distance.
4. If the Antenna Connection is directly used for a radiating whip connection, keep at least 5 cm radius free area. In case a 50 Ω impedance coaxial cable is connected, then 5 mm radius will suffice.

Reference Rules

The **TX-SAW/433 s-Z** transmitter complies with the EU Rules **ETS 300-220,** with a 5,5V max. supply. The equipment has been tested according to rule **EN 60950** and it can be utilized inside a special insulated housing that assures its compliance with the above mentioned rule. The transmitter must be supplied by a very low voltage source, safely protected against short circuits.

The use of the transmitter module is foreseen inside housings that assure the overcoming of the rules **EN 61000** not directly applicable to the module itself. In particular, it is left at the User's care, the insulation of the external antenna connection, and of the antenna itself, since the RF output of the transmitter is not built to directly bear the electrostatic charges foreseen by the **EN 61000-4-2** rules.

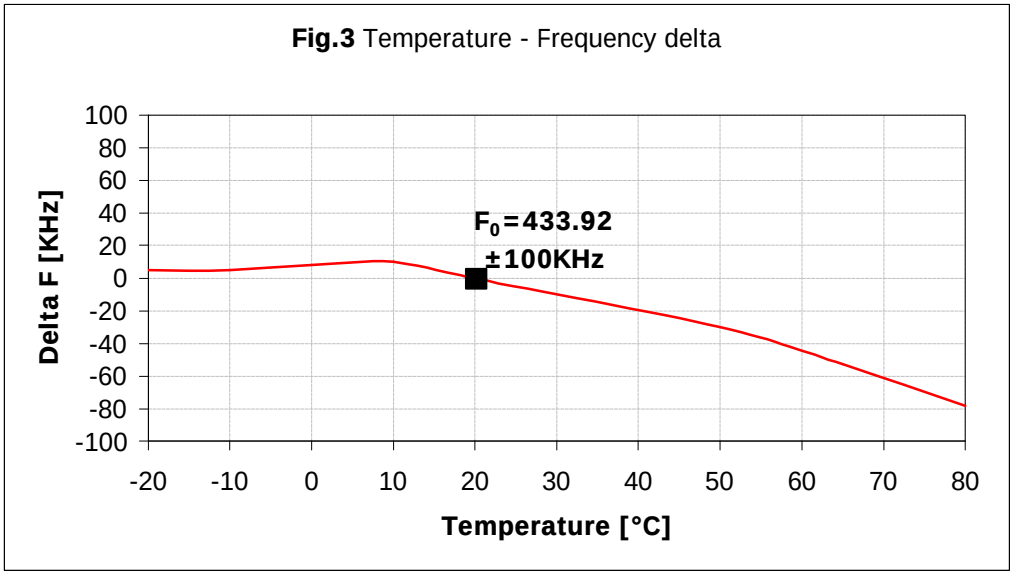
CEPT 70-03 Recommendation

In order to comply with such rule, the device must be used only for a 10% of an hourly duty-cycle, (that means 6 minutes of utilisation over 60). The device utilisation inside the italian territory is governed by the *Codice Postale* and *Telecomunicazioni* rules in force (art. no. 334 and subsequents).

BTX-SAW/433 s-Z module was previously BZT approved by mean of Test Report obtained c/o the laboratory: **SENTON GmbH** - Äussere Frühlingstrasse 45 D – 94315 STRAUBIN

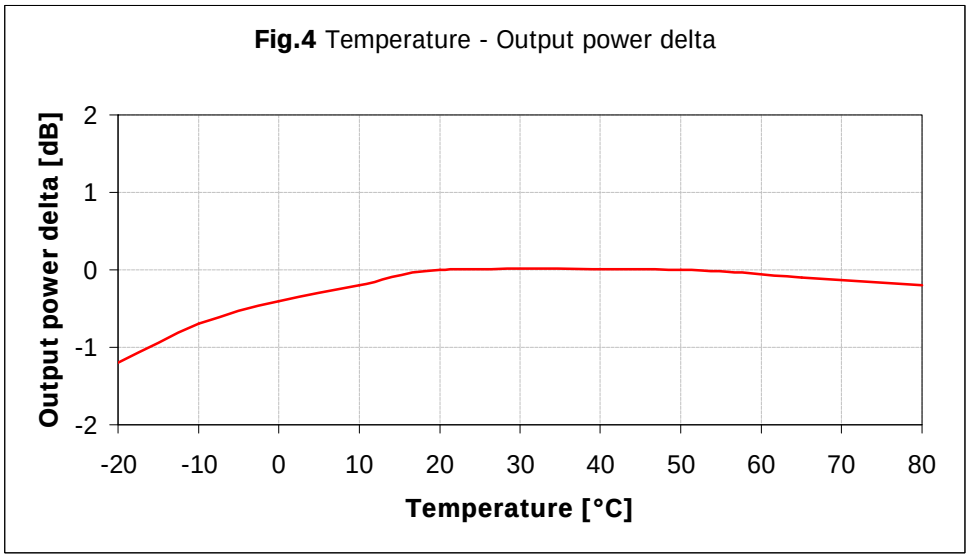
Reference curves

Fig.3 Temperature - Frequency delta



The curve has been obtained by the testing system shown in Fig.1.
5V Power supply

Fig.4 Temperature - Output power delta



The curve has been obtained by the testing system shown in Fig.1
5V supply, RF output 433,92MHz, ±100 kHz, output power 8dBm ±2dB